SONET/SDH/ATM OC-3/OC-12 TRANSCEIVER S3033

FEATURES

- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLL for clock generation
- Supports 155.52 Mbps (OC-3) and 622.08 Mbps (OC-12)
- Selectable reference frequencies of 19.44, 38.88, 51.84 or 77.76 MHz
- Interface to both LVPECL and TTL logic
- 8-bit TTL data path
- Compact 10 mm 64 PQFP/TEP package
- Diagnostic loopback mode
- Low jitter LVPECL interface
- Single 3.3V supply

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

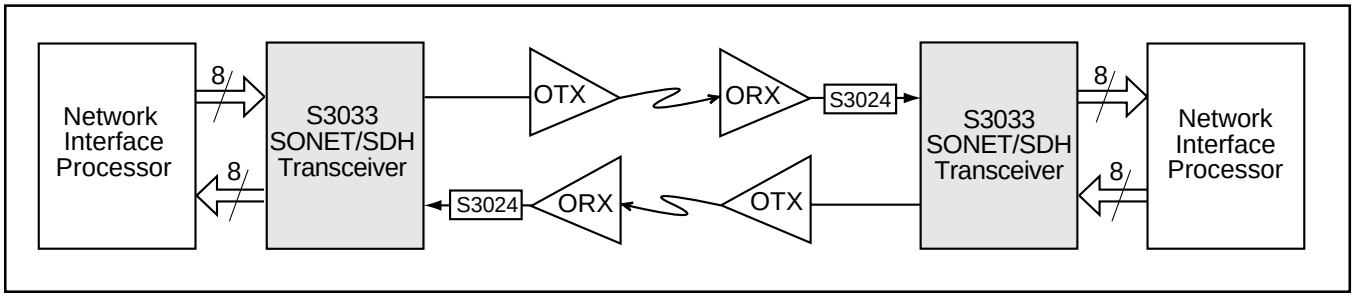
GENERAL DESCRIPTION

The S3033 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-12 (622.08 Mbps) and OC-3 (155.52 Mbps) interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3033 transceiver chip allowing the use of a slower external transmit clock reference. The S3033 performs SONET/SDH frame detection. The chip can be used with 19.44, 38.88, 51.84 or 77.76 MHz reference clocks, in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3033 is packaged in a 10 mm 64 PQFP/TEP, offering designers a small package outline.

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3033 chip supports OC-3 and OC-12 rates (155.52 and 622.08 Mbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-12 consists of 36 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 36 overhead and 1044 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

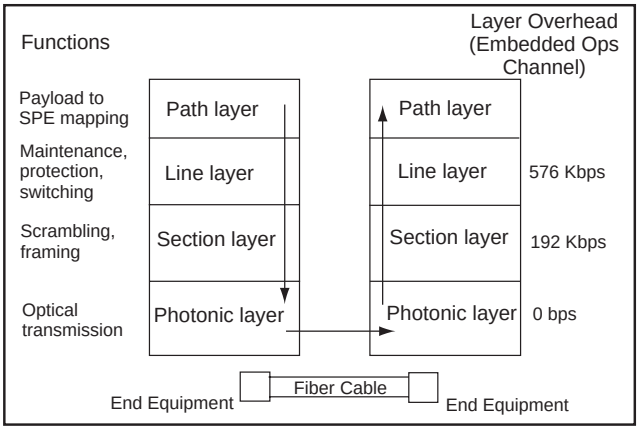


Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 3. STS–12/OC–12 Frame Format

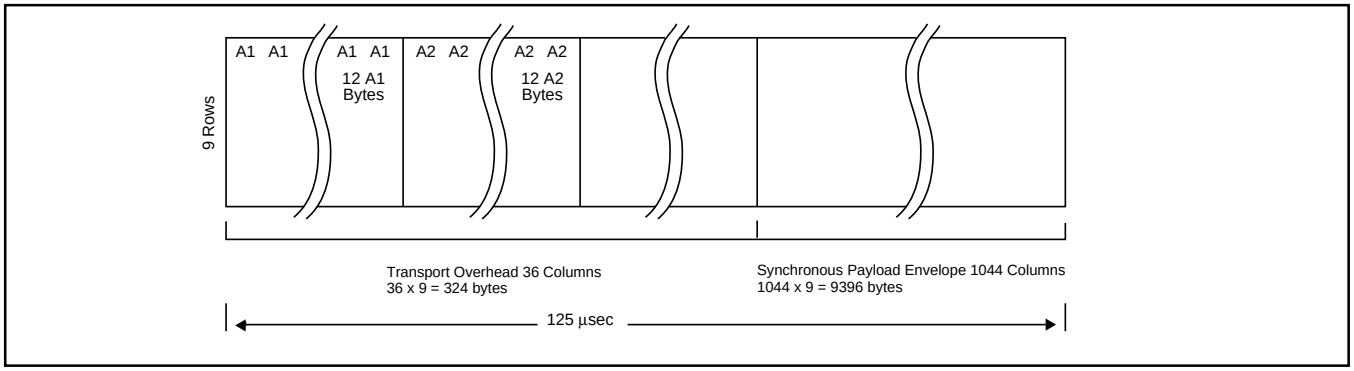
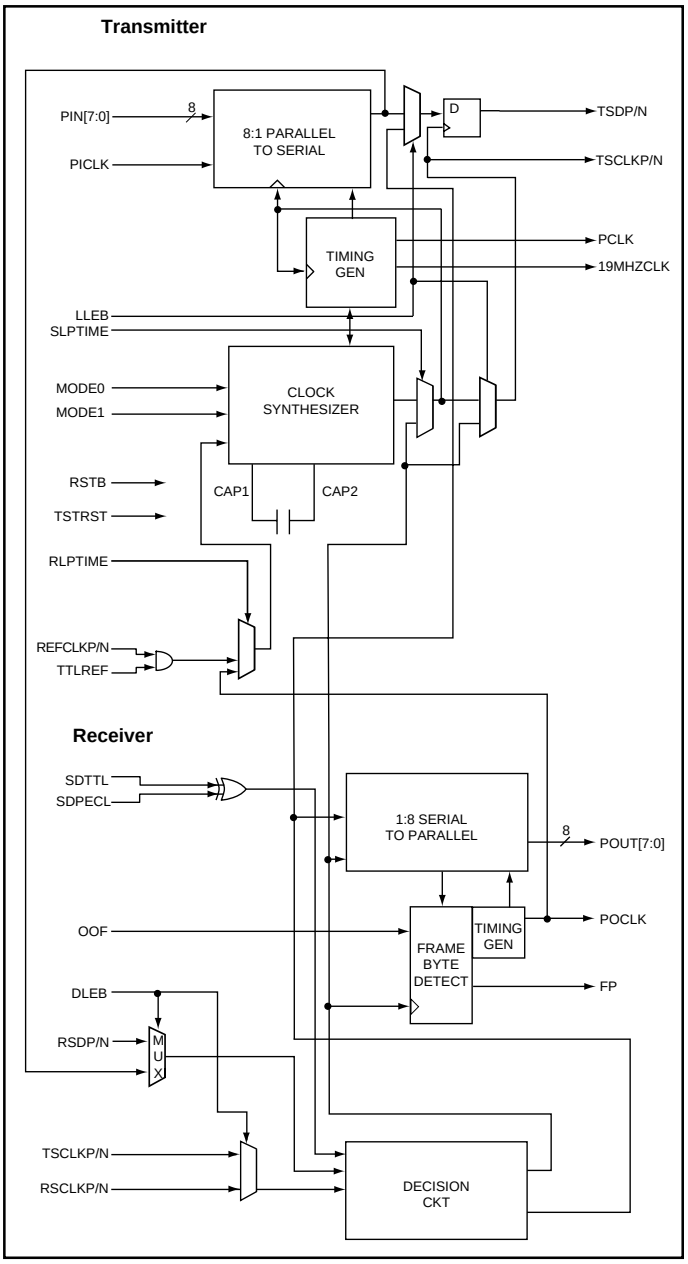


Figure 4. S3033 Transceiver Functional Block Diagram



S3033 OVERVIEW

The S3033 transceiver implements SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagram in Figure 4 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream, framing, and clock distribution throughout the front end.

The S3033 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Frame detection
2. Serial-to-parallel conversion
3. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 through 10.

Suggested Interface Devices

AMCC	S3024	155/622 Mbps Clock Recovery Device
AMCC	CONGO (S1201)	POS/ATM SONET Mapper
AMCC	NILE (S1202)	ATM SONET Mapper

S3033 TRANSCEIVER FUNCTIONAL DESCRIPTION

TRANSMITTER OPERATION

The S3033 transceiver chip performs the serializing stage in the processing of a transmit SONET STS-3 or STS-12 bit serial data stream. It converts the 8-bit parallel 19.44 or 77.76 Mbyte/sec data stream into bit serial format at 155.52 or 622.08 Mbps.

A high-frequency bit clock can be generated from a 19.44 or 77.76 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback is provided (transmitter to receiver). See Other Operating Modes.

Clock Synthesizer

The clock synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCLKP/N or TTLREF).

The REFCLKP/N or TTLREF input must be generated from a crystal oscillator which has a frequency accuracy that meets the value stated in Table 8 in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLKP/N or TTLREF input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generator

The timing generation function, seen in Figure 4, provides an 8-bit parallel rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PIN[7:0] data from the parallel input register to the serial shift register.

The PCLK output is an 8-bit parallel rate version of the transmit serial clock at 19.44 or 77.76 MHz. PCLK is intended for use as an 8-bit parallel speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3033 device.

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 4 is comprised of two 8-bit registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

The load signal, which latches the data from the parallel to the serial shift register, has a fixed relationship to PCLK. If PICLK is tied to PCLK, the PIN[7:0] data latched into the parallel register will meet the timing specifications with respect to the load signal. If PICLK is not tied to PCLK, the delay must meet the timing requirements shown in Figure 8.

Table 2. Reference Frequency Options

MODE [1:0]	REFERENCE CLOCK FREQUENCY	OPERATING MODE
00	19.44 MHz	STS-12
01	38.88 MHz	STS-12
10	51.84 MHz	STS-12
11	77.76 MHz	STS-12
0 NC	19.44 MHz	STS-3
1 NC	38.88 MHz	STS-3
NC 0	51.84 MHz	STS-3
NC 1	77.76 MHz	STS-3[1]
NC NC	Not Allowed	

1. Only valid in SLP Mode

Table 3. Reference Jitter Limits

Frequency Band	Maximum Reference Clock Jitter	Operating Mode
12 kHz to 5 MHz	14 ps rms	STS–12
12 kHz to 1 MHz	56 ps rms	STS–3

RECEIVER OPERATION

The S3033 transceiver chip provides the first stage of the digital processing of a receive SONET STS-3 or STS-12 bit-serial stream. It converts the bit-serial 155.52 or 622.08 Mbps data stream into a 19.44 or 77.76 Mbyte/sec 8-bit parallel data format.

A loopback mode is provided for diagnostic loopback (transmitter to receiver).

Frame and Byte Boundary Detection

The frame and byte boundary detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the Out-Of-Frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is active. It is disabled when a framing pattern is detected and OOF is inactive. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or looped transmitter data). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the Frame Pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 or STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 µs, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that the frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern

Serial-to-Parallel Converter

The serial-to-parallel converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial-to-parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the serial-to-parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

(See Figure 11.)

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the serial-to-parallel block in place of the normal data stream (RSD). DLEB takes precedence over SDPECL and SDTTL.

Line Loopback

The line loopback circuitry consists of alternate clock and data output drivers. For the S3033, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable (LLEB) input is inactive, it selects data and clock from the parallel to serial converter block. When LLEB is active, it forces the output data multiplexer to select data and clock from the RSD and RSCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. Diagnostic loopback and line loopback can be active at the same time.

Serial Loop Timing

In Serial Loop Timing (SLPTIME) mode, the clock synthesizer PLL of the S3033 is bypassed, and the timing of the entire transmitter section is controlled by the Receive Serial Clock (RSCLKP/N). This mode is entered using the SLPTIME input.

In this mode the REFCLKP/N input is not used, and the MODE[1:0] inputs are ignored for all transmit functions. It should be carefully noted that the internal PLL continues as the source for the 19MHZCLK, and if this signal is being used (e.g. as the reference for an external clock recovery device), the REFCLKP/N and MODE[1:0] inputs must be properly driven.

Reference Loop Timing

In Reference Loop Timing (RLPTIME) mode, the clock synthesizer PLL is still used as the clock source for the transmit section. However, the parallel receive clock is used as the reference clock for the clock synthesizer PLL. The MODE[1:0] inputs must be in the logic High state (1,1) for STS-12 operation or (0,NC) state for STS-3 operation.

Forward Clocking

For both 77.78 MHz and 38.88 MHz reference operation, the S3033 operates in the forward clocking mode. The PLL locks the PCLK output of the transmitter section to the REFCLK with a fixed and repeatable phase relation. This allows the transmitter data source to also be the timing source for the serial clock synthesis.

The rising edge of PCLK is locked to the rising edge of REFCLKP, with a maximum delay of 8 to 10 ns due to the PCLK TTL output driver.

For operation at 19.44 MHz and 51.84 MHz references, separate timing paths are used for PLL control and PCLK generation, and forward clocking is not recommended.

Table 4. Transmitter Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PIN7 PIN6 PIN5 PIN4 PIN3 PIN2 PIN1 PIN0	LVTTL	I	59 58 57 56 55 54 53 52	Parallel data input, a 77.76 Mbyte/s or 19.44 Mbyte/s word, aligned to the PICLK parallel input clock. PIN7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PICLK.
PICLK	LVTTL	I	60	Parallel Input Clock, a 77.76 or 19.44 MHz, nominally 50% duty cycle input clock, to which PIN[7:0] is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN[7:0]. After a master reset, two rising edges of PICLK are required to fully initialize the internal data path.
CAP1 CAP2	Analog	I	9 8	The loop filter capacitor is connected to these pins. The capacitor value should be 0.01µF ±10% tolerance, X7R dielectric. 50 volt is recommended (16 volt is acceptable).
TSDP TSDN	Diff. LVPECL	O	17 18	Transmit Serial Data. Serial data stream signals, normally connected to an optical transmitter module.
TSCLKP TSCLKN	Diff. LVPECL	O	21 20	Transmit Serial Clock that can be used to retime the TSD signal. This clock will be 622.08 MHz or 155.52 MHz, depending on the operating mode.
PCLK	LVTTL	O	62	A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3033 device.
19MHZCLK	TTL	O	64	19 MHz Clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function (such as the S3024).

Table 5. Receiver Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Diff. LVPECL	I	24 25	Receive Serial Data stream signals normally connected to an optical receiver module. A clock is recovered from transitions on the RSD inputs.
OOF	LVTTL	I	34	Out-Of-Frame indicator. Active High. Used to enable framing pattern detection logic in the S3033. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set Low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 12 and 13.)
SDPECL	LVPECL	I	23	LVPECL Signal Detect. LVPECL with internal 1 kΩ pull-down. Active High when SDTTL is held at logic 0. A single-ended 10K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDPECL is inactive, the data on the Serial Data (RSDP/N) pins will be internally forced to a constant zero. When SDPECL is active, data on the RSDP/N pins will be processed normally. When SDTTL is to be connected to the optical receiver module instead of SDPECL, then SDPECL should be tied High to implement an active Low signal detect, or left unconnected to implement an active High signal detect.
SDTTL	LVTTL	I	22	LVTTL Signal Detect. Active High when SDPECL is unconnected (logic 0). Active Low when SDPECL is held at logic 1. A single-ended LVTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDTTL is inactive, the data on the RSDP/N pins will be internally forced to a constant zero. When SDTTL is active, data on the RSDP/N pins will be processed normally.
POUT7 POUT6 POUT5 POUT4 POUT3 POUT2 POUT1 POUT0	LVTTL	O	46 45 44 42 41 40 38 37	Parallel Output data bus. A 77.76 Mbyte/s or 19.44 Mbyte/s word, aligned to the POCLK parallel output clock. POUT7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT[7:0] is updated on the falling edge of POCLK.
FP	LVTTL	O	36	Frame Pulse. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48-bit sequence matching the framing is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.
RSCLKP RSCLKN	LVPECL	I	28 29	Receive Serial Clock. Used to supply a clock input for the RSDP/N inputs.
POCLK	LVTTL	O	48	Parallel Output Clock. A 77.76 or 19.44 MHz, nominally 50% duty cycle, byte rate output clock that is aligned to POUT[7:0] 8-bit parallel output data. POUT[7:0] and FP are updated on the falling edge of POCLK.

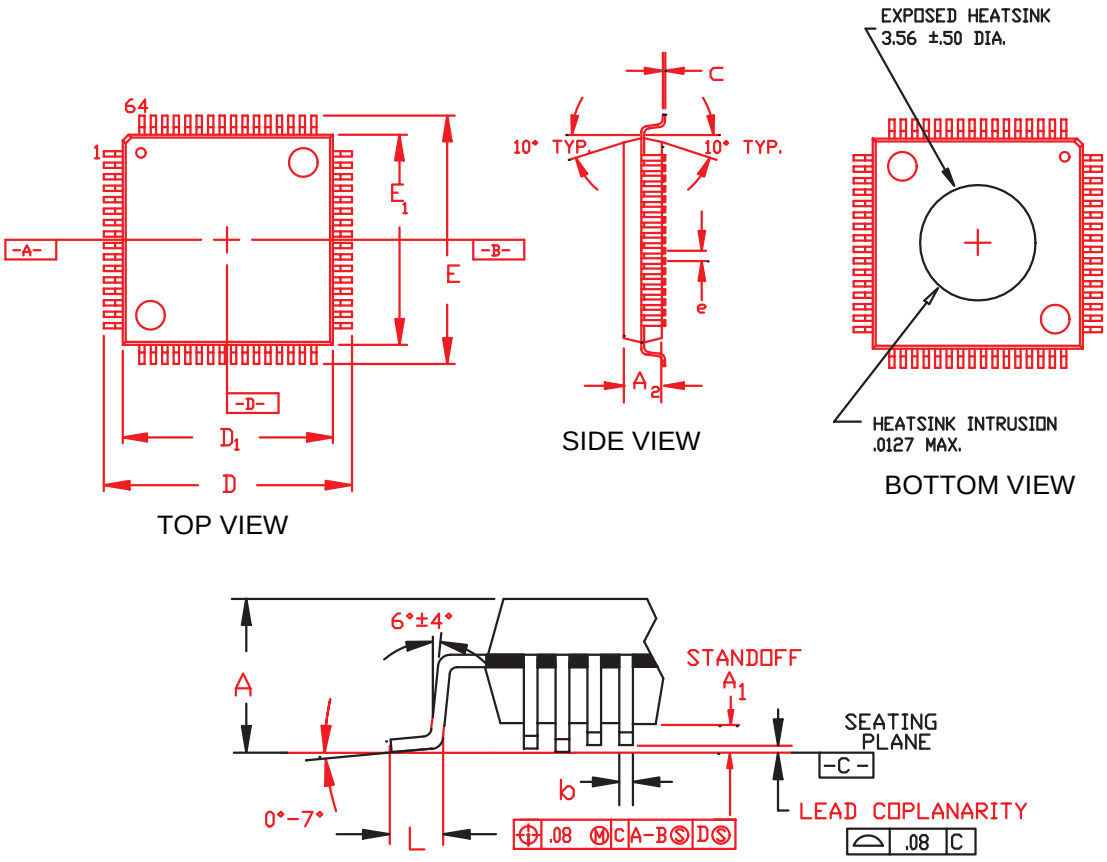
Table 6. Common Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
REFCLKP REFCLKN	Diff. LVPECL	I	5 4	Reference Clock input. Used as the reference for the internal bit clock frequency synthesizer. (Must be connected to a logic one state if TTLREF is used).
TTLREF	LVTTL	I	3	TTL Reference clock input. Can be used as the reference for the internal bit clock frequency synthesizer. (Must be tied High if REFCLKP/N is used).
DLEB	LVTTL	I	32	Diagnostic Loopback Enable. Active Low. Selects diagnostic loopback. When DLEB is inactive, the S3033 device uses the primary data (RSD) and clock (RSCLK) inputs. When active, the S3033 device uses the diagnostic loopback clock and data from the transmitter.
RSTB	LVTTL	I	33	Master Reset. Active Low. Reset input for the device. Initializes the device to a known state.
LLEB	LVTTL	I	13	Line Loopback Enable. Active Low. Selects line loopback. When LLEB is active, the S3033 will route the data from the RSD/RSCLK inputs to the TSD/TSCLK outputs.
MODE1 MODE0	LVTTL	I	49 50	Operating Mode select inputs. Used to select the reference clock frequency and the operating speed. (See Table 2).
SLPTIME	LVTTL	I	51	Serial Clock Loop Time select input. Used to enable the recovered clock from the receive section to be used in place of the synthesized transmit clock.
RLPTIME	LVTTL	I	14	Reference Clock Loop Time select input. Used to enable the parallel recovered clock from the receiver to be used as the reference clock input to the transmitter.
TSTRST	LVTTL	I	12	Test Pin.
TTLINGND	GND		63	Ground (0V).
TTLINVCC	+3.3V		61	Power Supply.
TXCOREVCC	+3.3V		2	Power Supply.
TXCOREGND	GND		1	Ground (0V).

Table 6. Common Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
AGND0 AGND1	GND		10 7	Ground (0V)
AVCC0 AVCC1	+3.3V		11 6	Power Supply
TXOUTVCC	+3.3V		16	Power Supply
TTLVCC	+3.3V		47 39	Power Supply
TTLGND	GND		35 43	Ground (0V)
RXCOREVCC	+3.3V		30	Power Supply
RXCOREGND	GND		31	Ground (0V)
RSCLKVCC	+3.3V		27	Power Supply
RSCLKGND	GND		26	Ground (0V)
TXOUTGND	GND		19	Ground (0V)
NC			15	Not connected.

Figure 5. 64 PQFP/TEP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	1.95	13.00	9.90	13.00	9.90	0.78	0.50 BSC.	0.17	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.22	
MAX	2.45	0.50	2.10	13.40	10.10	13.40	10.10	1.03		0.27	0.17

Table 7. Thermal Management

Max Package Power	Max Θja	Θjc
1.18 W	39° C/W	2.5° C/W

Figure 6. Pinout Assignments

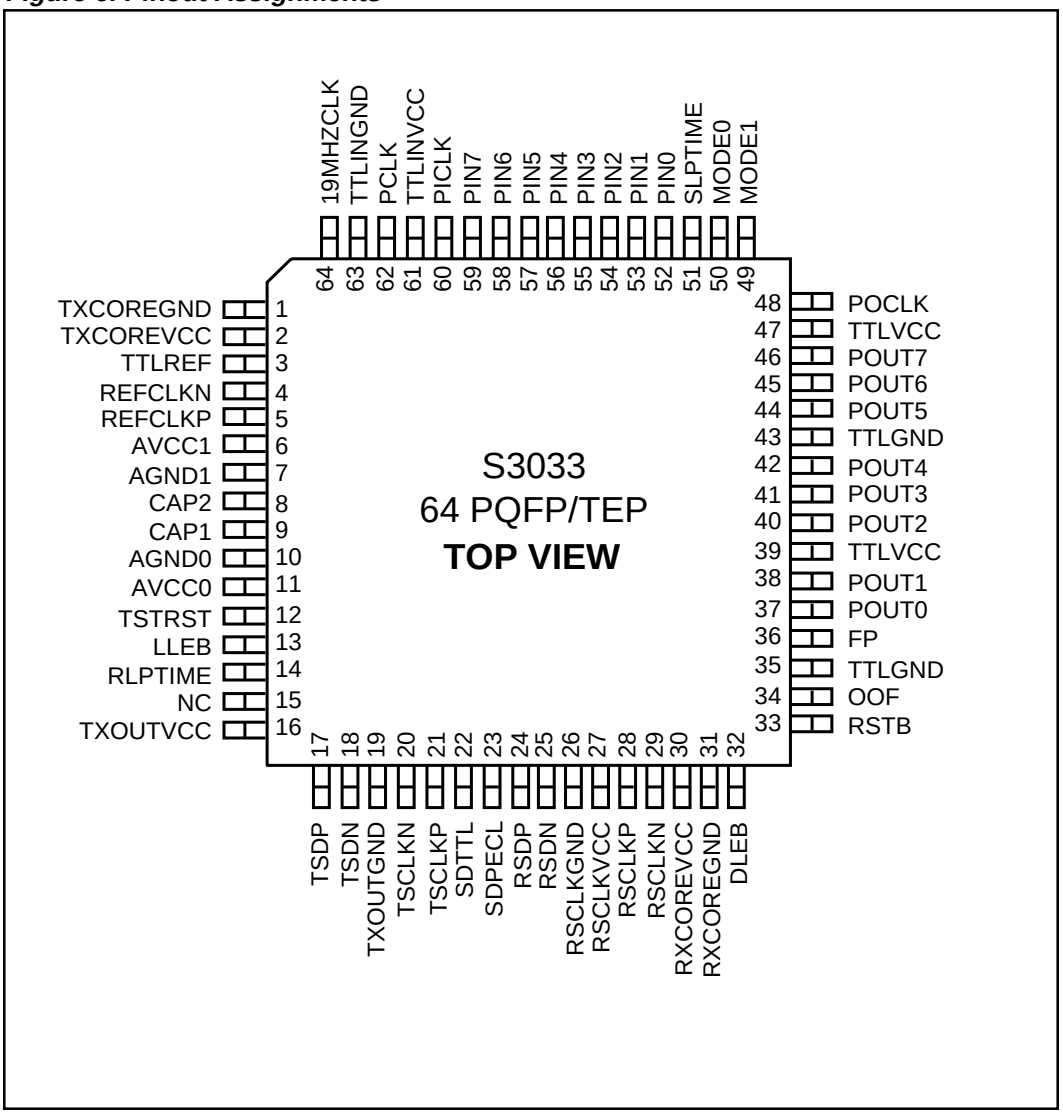


Table 8. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08 ±12%		MHz	
TSCLK Clock Output Jitter OC-3/STS-3 OC-12/STS-12			 32 8	 ps(rms) ps(rms)	Given the jitter on REFCLKP/N (12 kHz to 1 MHz band for OC-3 and 12 kHz to 5 MHz band for OC-12) is less than: 56 ps rms (OC-3) 14 ps rms (OC-12)
Data Output Jitter **STS-12** -19.44 MHz Ref Clk -38.88 MHz Ref Clk -51.84 MHz Ref Clk -77.76 MHz Ref Clk **STS-3** -19.44 MHz Ref Clk -38.88 MHz Ref Clk -51.84 MHz Ref Clk			 0.009 0.008 0.007 0.006 0.004 0.003 0.003	UI (rms)	rms jitter, in lock
Reference Clock Frequency Tolerance*	-20		+20	ppm	Required to meet SONET output frequency specification
Reference Clock Input Duty Cycle	30		70	% of UI	
Reference Clock Rise & Fall Times			2.0	ns	20% to 80% of amplitude
LVPECL Output Rise & Fall Times			450	ps	20% to 80%, 50Ω load, 5 pF cap
TSCLK Duty Cycle	40		60	%	

* Noise on REFCLKP/N should be less than 14 ps rms in a jitter frequency band from 12 kHz to 5 MHz for OC-12 operating rate.

Table 9. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with Respect to GND	-0.5		+7.0	V
Voltage on any LVTTL Input Pin	-0.5		+5.5	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
LVTTL Output Sink Current			8	mA
LVTTL Output Source Current			8	mA
High Speed LVPECL Output Source Current			24	mA

ESD Ratings

The S3033 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500 V except pin 8, pin 9, and pin 21.

Table 10. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Conditions
Ambient Temperature Under Bias	-40		85	˚C	
Junction Temperature Under Bias	-40		+125	˚C	
Voltage on V_{CC} with Respect to GND 3.3V Operation	3.135	3.3	3.465	V	
Voltage on any LVTTL Input Pin	0		5.5	V	
Voltage on any LVPECL Input Pin	0		4.0	V	
Icc Supply Current		290	340	mA	Outputs open, V_{CC} = V_{CC} max
P_D Power Dissipation		0.96	1.18	W	Outputs open, V_{CC} = V_{CC} max

Table 11. LVTTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.1 2.2			V V	V_{CC} = min, I_{OH} = -2.4 mA V_{CC} = min, I_{OH} = -0.1 mA
V_{OL}	Output Low Voltage (TTL)			0.5	V	V_{CC} = min, I_{OL} = -2.4 mA
V_{IH}	Input High Voltage (TTL)	2.0		5.5	V	$I_H \leq 1$ mA at V_{IH} = 5.5 V
V_{IL}	Input Low Voltage (TTL)	0		0.8	V	
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V

Table 12. LVPECL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} -2.000		V_{CC} -1.441	V	Guaranteed input Low voltage for single ended inputs
V_{IH}	Input High Voltage	V_{CC} -1.225		V_{CC} -0.570	V	Guaranteed input High voltage for single ended inputs
V_{IL}	Input Low Voltage	V_{CC} -2.000		V_{CC} -0.700	V	Guaranteed input Low voltage for differential inputs
V_{IH}	Input High Voltage	V_{CC} -1.750		V_{CC} -0.450	V	Guaranteed input High voltage for differential inputs
V_{ID}	Input Differential Voltage	0.200	0.500	1.400	V	Differential input voltage
I_{IHD}	Differential Input High Current	-0.500		20.000	µA	V_{ID} = 500 mV
I_{ILD}	Differential Input Low Current	-0.500		20.000	µA	V_{ID} = 500 mV
I_{IH}	Input High Current Single Ended			100	µA	SD inputs have internal 24 kΩ to 1.8V load resistor
I_{IL}	Input Low Current Single Ended			100	µA	SD inputs have internal 24 kΩ to 1.8V load resistor
V_{OL}	Output Low Voltage	V_{CC} -2.000		V_{CC} -1.500	V	50 Ω termination to V_{CC} -2V
V_{OH}	Output High Voltage	V_{CC} -1.210		V_{CC} -0.670	V	50 Ω termination to V_{CC} -2V
V_{OS}	Single Ended Output Voltage Swing	0.390		1.330	V	
V_{OD}	Differential Output Voltage Swing	0.780		2.660	V	

Table 13. Transmitter AC Timing Characteristics

Parameter	Description	Min	Max	Units
tD_{PICLK}	PICLK Delay from PCLK	0	5.5	ns
tS_{PIN}	PIN[7.0] Set-up Time w.r.t. PICLK	1.5		ns
tH_{PIN}	PIN[7.0] Hold Time w.r.t. PICLK	1.0		ns
tP_{TSD}	TSCLK Low to TSD Valid Propagation Delay	-200	600	ps
tS_{TSD}	TSDP/N Set-up Time w.r.t. TSCLK	200		ps
tH_{TSD}	TSDP/N Hold Time w.r.t. TSCLK	200		ps

Figure 7. Transmitter Output Timing

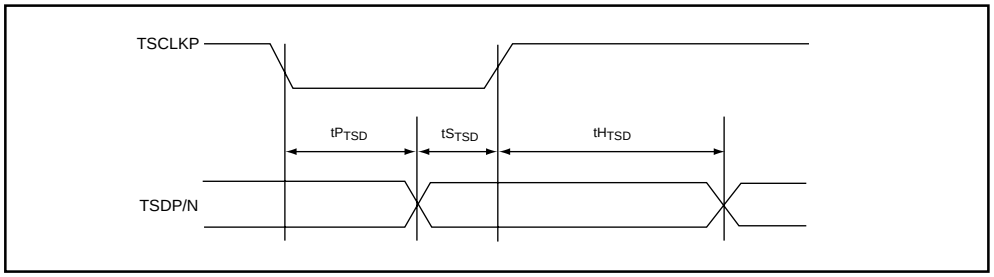
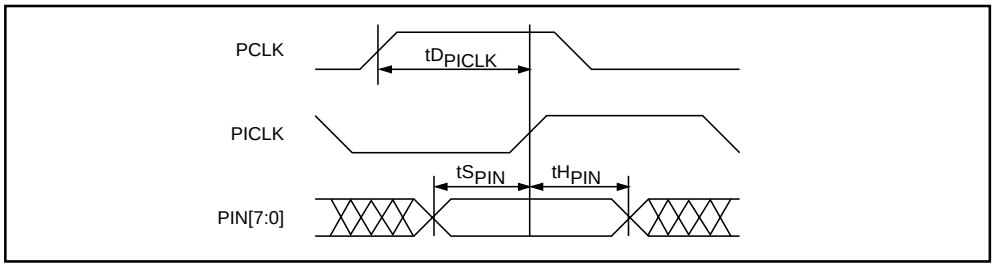


Figure 8. Transmitter Input Timing



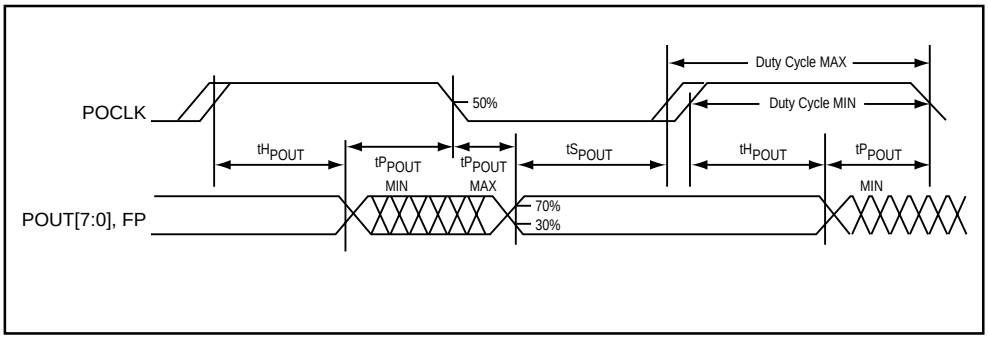
1. When a set-up time is specified on LVTTL signals between an input and a clock, the set-up time is the time in nano seconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVTTL signals between an input and a clock, the hold time is the time in nano seconds from the 50% point of the clock to the 50% point of the input.
3. When a set-up time is specified on differential LVPECL signals between an input and a clock, the set-up time is the time in nano seconds from the cross-over point of the input to the cross-over point of the clock.
4. When a hold time is specified on differential LVPECL signals between an input and a clock, the hold time is the time in nano seconds from the cross-over point of the clock to the cross-over point of the input.

Table 14. Receiver AC Timing Characteristics

Parameter	Description	Min	Max	Units
	POCLK Duty Cycle	40	60	%
tP_{POUT}	POCLK Low to POUT [7:0] Valid prop. delay at STS-3 POCLK Low to POUT [7:0] Valid prop. delay at STS-12	-8 -3	0 1	ns ns
tS_{POUT}	POUT[7:0] and FP Set-up Time w.r.t. POCLK[1]	4		ns
tH_{POUT}	POUT[7:0] and FP Hold Time w.r.t. POCLK[1]	3		ns
tS_{RSD}	RSDP/N Set-up Time w.r.t. RSCLKP/N	400		ps
tH_{RSD}	RSDP/N Hold Time w.r.t. RSCLKP/N	400		ps

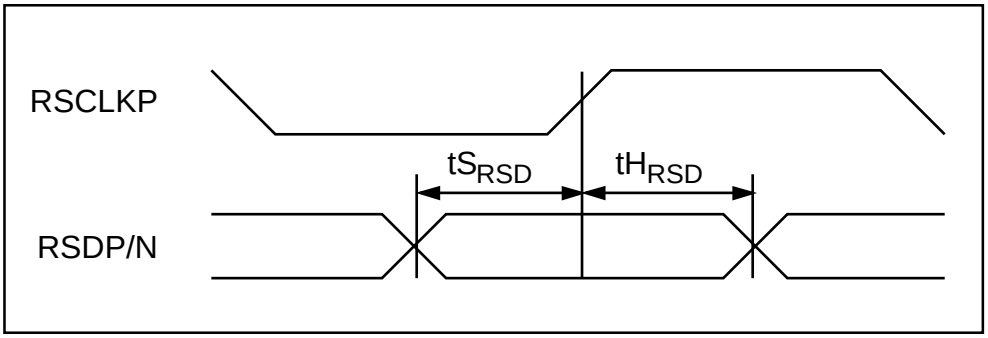
1. Set-up and hold times are specified for an interface which directly connects the S3033 receiver parallel outputs to the data and clock inputs on an external register.

Figure 9. Receiver Output Timing Diagram



Notes on Output Timing:
1. Output propagation delay time of LVTTL outputs is the time in nano seconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays of LVTTL outputs are measured with a 15 pF load on the outputs.

Figure 10. Receiver Input Timing



RECEIVER FRAMING

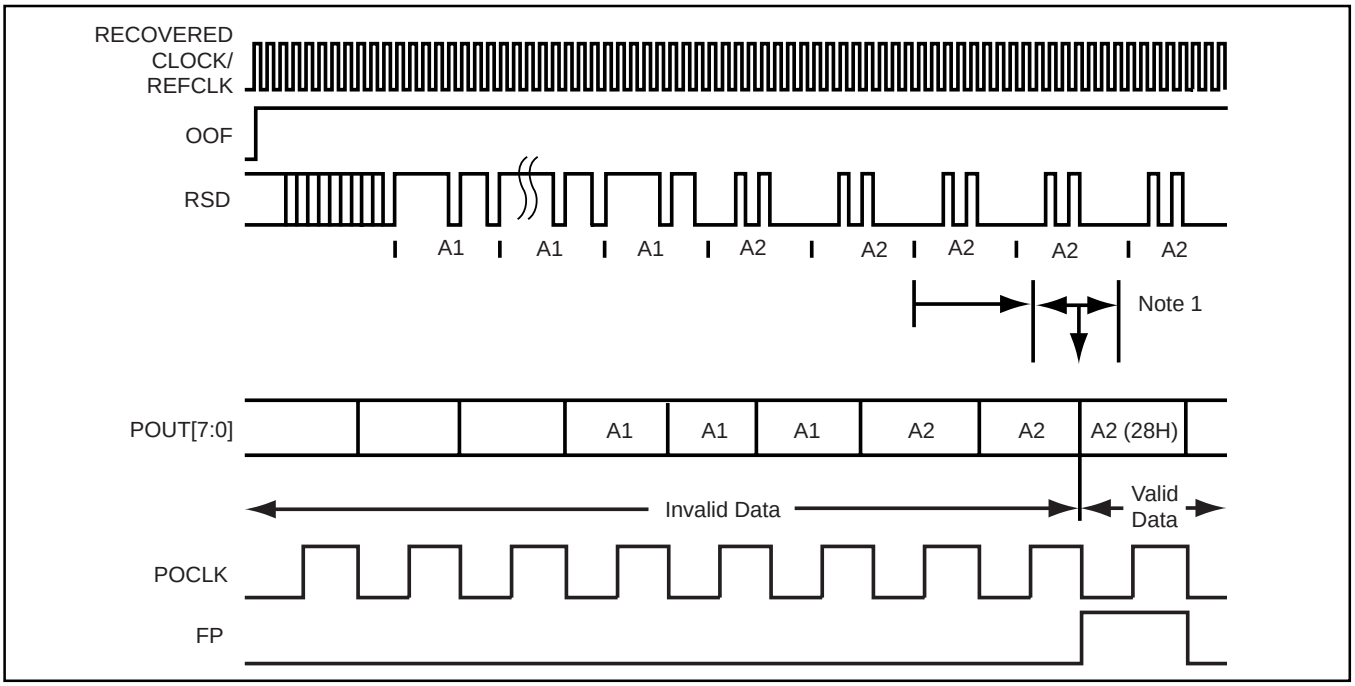
Figure 11 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is High. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the Frame Pulse (FP) is set High for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains High for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 12. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set Low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP or until OOF goes Low, whichever occurs last. Figure 12 shows a typical OOF timing pattern which occurs when the S3033 is connected to a down stream section terminating device. OOF remains High for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes Low.

Figure 13 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP.

Figure 11. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 12. OOF Operation Timing with PM5312 STTX or PM5355 SUNI-622

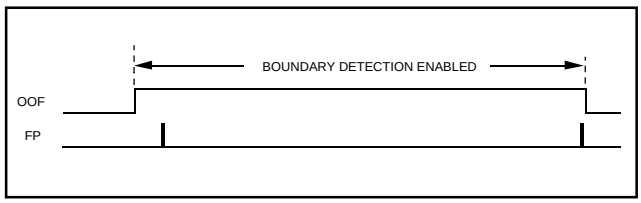
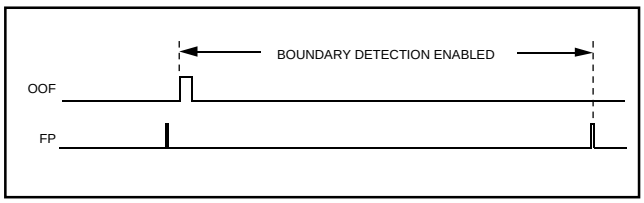


Figure 13. Alternate OOF Timing



S3033 WITH DATA CLOCK SYNCHRONOUS TO REFERENCE CLOCK

In some applications it is necessary to "forward clock" the data in a SONET/SDH system. In this application the reference clock from which the high speed serial clock is synthesized and the parallel data clock both originate from the same (usually TTL/CMOS) clock source. This application note explains how the AMCC S3033 can be configured to operate in this mode.

Clock Control Logic Description

The timing control logic in the S3033 automatically generates an internal load signal which has a fixed relationship to the reference clock. The logic takes in to account the variation of the reference clock to the internal load signal over temperature and voltage.

The connections required to implement the design are shown in Figure 14. The set up and hold times for the PICLK to the data must be met by the controller ASIC. We recommend latching the data on the falling edge of the output reference clock in order to meet the required specifications.

Possible Problems

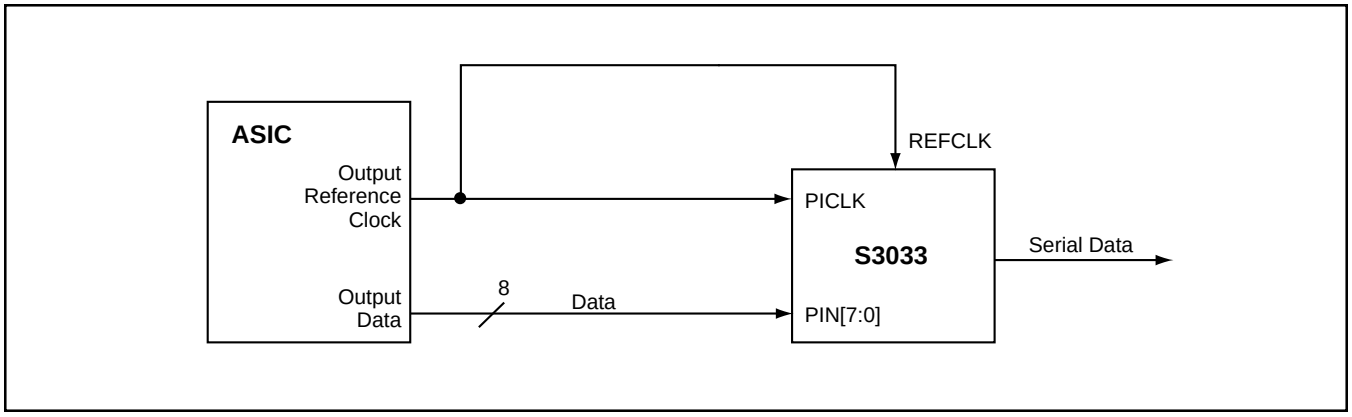
In order to meet the jitter generation specifications required by SONET, the jitter of the reference clock must be minimized. It may be difficult to meet the SONET jitter generation specifications using a reference clock input with a TTL reference source.

Power Sequencing

When the S3033 is operated with a 5 Volt controller such as the PMC 5355 SUNI, it is recommended that power be applied to the S3033 before or simultaneously (Time difference less than 1 ms) with the application of power to the 5 Volt controller. If this condition cannot be met, series resistance of at least 33 Ω is required on all TTL inputs driven from the 5 Volt environment.

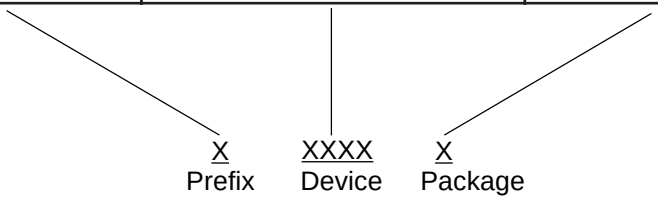
Please note that 33 Ω is already recommended on dynamically switching input signals such as PIN[7:0], OOF, PICLK, and TTLREF to limit overshoot and ringing. Static control lines such as LLEB, DLEB, RLPTIME, SLPTIME, MODE[1:0], SDTTL and RSTB should also be provided with series resistors of at least 33 Ω (100 Ω recommended) to limit input current if the 5 Volt environment is powered while the 3.3 Volt V_{CC} of the S3033 is off.

Figure 14. S3033 with Data Clocked by Reference Clock



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3033	A – 64 PQFP/TEP



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