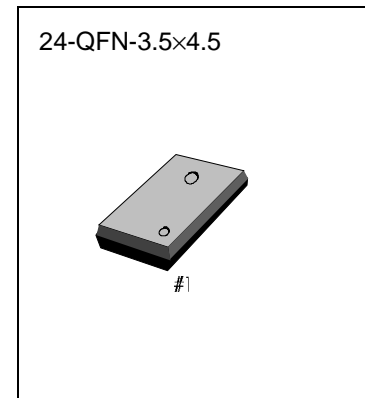


INTRODUCTION

The S1M8836/37 is a Fractional-N frequency synthesizer with integrated prescalers, designed for RF operation up to **1.0GHz/2.5GHz** and for IF operation up to 520MHz. The fractional-N synthesizer allows fast-locking, low phase noise phase-locked loops to be built easily, thus having rapid channel switching and reducing standby time for extended battery life. The S1M8836/37 based on $\Sigma - \Delta$ fractional-N techniques solves the fractional spur problems in other fractional-N synthesizers based on charge pump compensation. The synthesizer also has an additional feature that the PCS/CDMA channel frequency in steps of 10kHz can be accurately programmed.

The S1M8836/37 contains quadruple-modulus prescalers. The S1M8836 RF synthesizer adopts an 8/9/12/13 prescaler(16/17/20/21 for the S1M8837) and the IF synthesizer adopts an 8/9 prescaler. Phase detector gain is user-programmable for maximum flexibility to address IS-95 CDMA and IMT2000. Various program-controlled power down options as well as low supply voltage help the design of wireless cell phones having minimum power consumption.

Using the Samsung's proprietary digital phase-locked-loop technique, the S1M8836/37 has a linear phase detector characteristic and can be used for very stable, low noise PLL's. Supply voltage can range from 2.7V to 4.0V. The S1M8836/37 is available in a 24-QFN package.



FEATURES

- High operating frequency dual synthesizer
- Operating voltage range : 2.7 to 4.0V
- Low current consumption(S1M8836: 5.5mA, S1M8837: 7.5mA)
- Selectable power saving mode (Icc = 1uA typical @3V)
- Quadruple-modulus prescaler and Fractional-N/Integer-N:
 - S1M8836 (RF) 8/9/12/13 Fractional-N
 - S1M8837 (RF) 16/17/20/21 Fractional-N
 - S1M8836/37 (IF) 8/9 Integer-N
- S1M8836: 250MHz to **1.0GHz**(RF) / 45MHz to 520MHz(IF)
- S1M8837: 500MHz to 2.5GHz(RF) / 45MHz to 520MHz(IF)
- Excellent in-band phase noise (- 85dBc/Hz @ PCS, - 90dBc/Hz @ CDMA)
- Improved fractional spurious performance (< 80dBc)
- Frequency resolution (= 10kHz/64 @ f_{ref} = 9.84MHz)
- Fast channel switching time: <500us
- Programmable charge pump output current: from 50μA to 800μA in 50μA steps
- Programmability via on-chip serial bus interface

APPLICATIONS

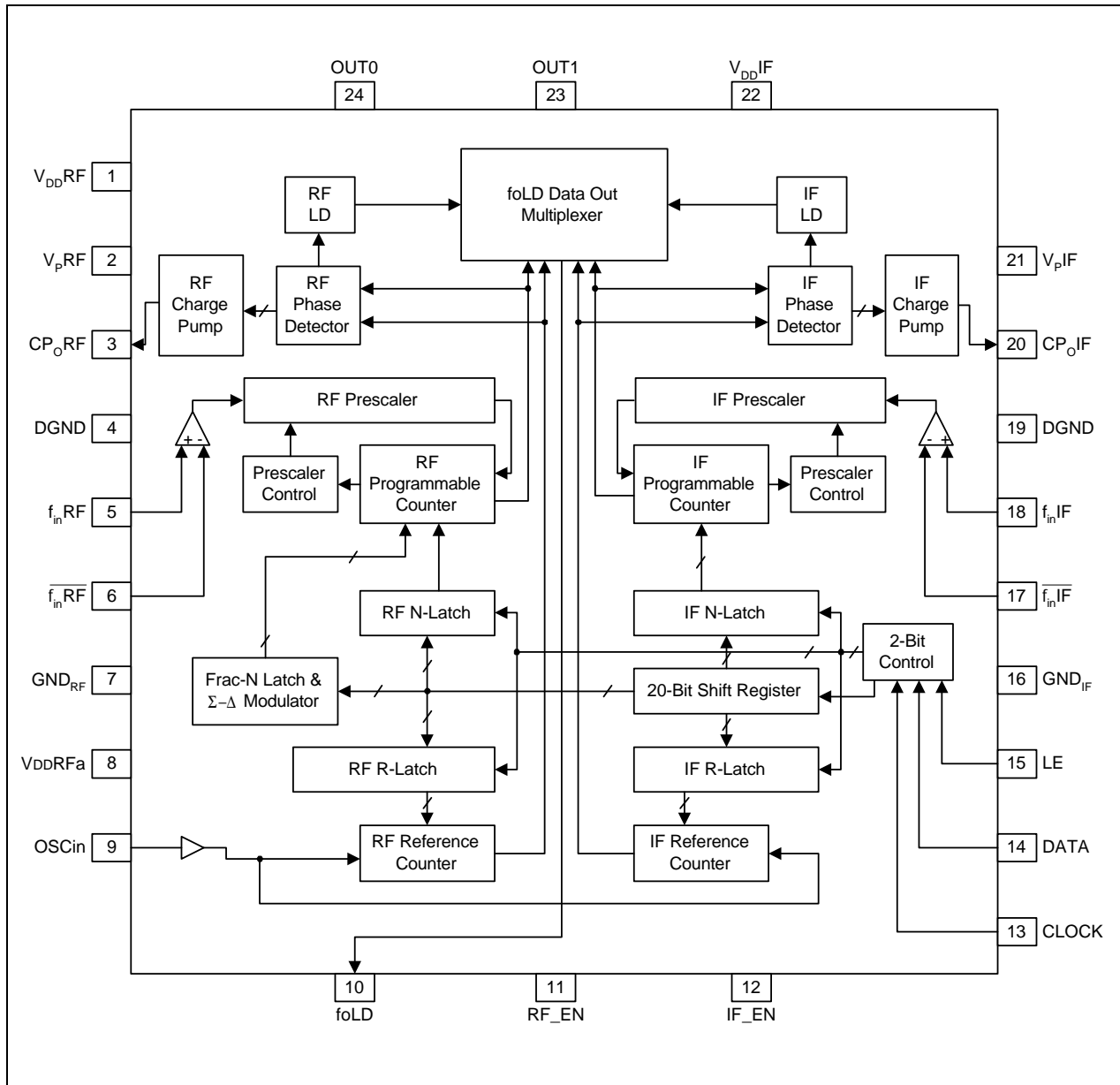
- High-rate data-service cellular telephones (for CDMA) : S1M8836, S1M8837
- High-rate data-service portable wireless communications : S1M8837
- Other wireless communications systems

ORDERING INFORMATION

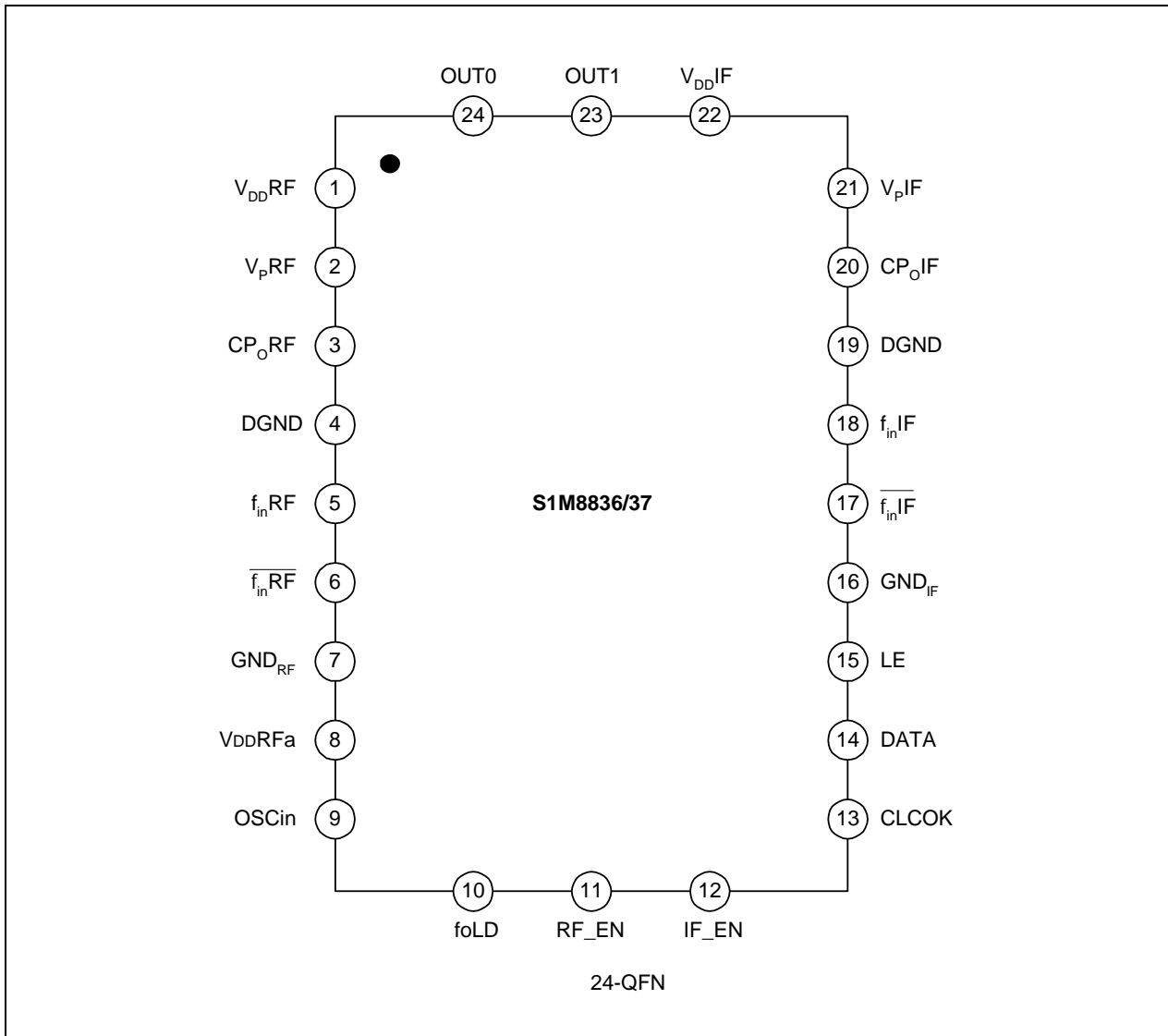
Device	Package	Operating Temperature
+ S1M8836X01-G0T0	24-QFN-3.5×4.5	-40 to +85C
+ S1M8837X01-G0T0		

+: New Product

BLOCK DIAGRAM



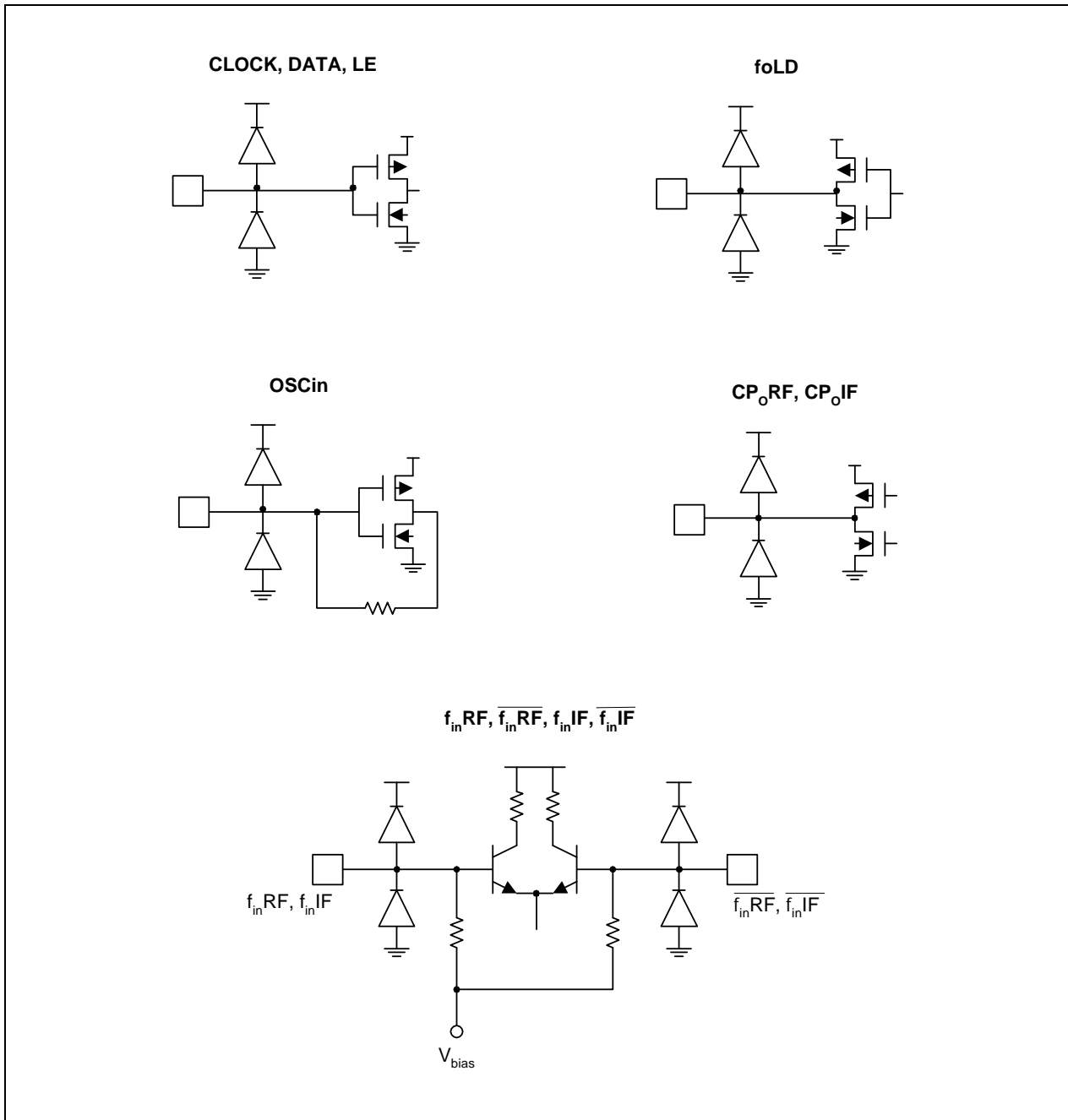
PIN DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Descriptions
1	V_{DDRF}	–	RF PLL power supply (2.7V to 4.0V). Must be equal to V_{DDIF} .
2	V_{pRF}	–	Power supply for RF charge pump. Must be $\geq V_{DDRF}$ and V_{DDIF} .
3	CPoRF	O	RF charge pump output. Connected to an external loop filter.
4	DGND	–	Ground for RF PLL digital circuitry.
5	finRF	I	RF prescaler input. Small signal input from the external VCO.
6	$\overline{\text{finRF}}$	I	RF prescaler complementary input. For a single-ended output RF VCO, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
7	GNDRF	–	Ground for RF PLL analog circuitry.
8	V_{DDRFa}	–	PLL power supply (2.7V to 4.0V) for RF analog (prescaler). Must be equal to V_{DDRF}
9	OSCIin	I	Oscillator input to drive both the IF and RF R counter inputs.
10	foLD	O	Multiplexed output of N or R divider and RF/IF lock detect.
11	RF_EN	I	RF PLL Enable (Enable when HIGH, Power down when LOW). Controls the RF PLL to power down directly, not depending on a program control. Also sets the charge pump output to be in TRI-STATE when LOW. Powers up when HIGH depends on the state of RF_CTL_WORD.
12	IF_EN	I	IF PLL Enable (Enable when HIGH, Power-down when LOW). Controls the IF PLL to power down directly. The same as RF_EN except that power-up depends on the state of IF_CTL_WORD.
13	CLOCK	I	CMOS clock input. Data for the various counters is clocked into the 22-bit shift register on the rising edge.
14	DATA	I	Binary serial data input. Data entered MSB (Most Significant Bit) first.
15	LE	I	Load enable when LE goes HIGH. High impedance CMOS input.
16	GNDIF	–	Ground for IF analog circuitry.
17	$\overline{\text{finIF}}$	I	IF prescaler complementary input. For a single-ended output IF VCO, a bypass capacitor should be placed as close as possible to this pin.
18	finIF	I	IF prescaler input. Small signal input from the VCO.
19	DGND	–	Ground for IF PLL digital circuitry.
20	CPoIF	O	IF charge pump output. Connected to an external loop filter.
21	V_{pIF}	–	Power supply for IF charge pump. Must be $\geq V_{DDRF}$ and V_{DDIF} .
22	V_{DDIF}	–	IF PLL power supply (2.7V to 4.0V). Must be equal to V_{DDRF} .
23	OUT1	O	Programmable CMOS output. Level of the output is controlled by W2[19] bit.
24	OUT0	O	Programmable CMOS output. Level of the output is controlled by W2[18] bit. In the Speedy Lock mode, the OUT0 and OUT1 pins can be utilized as synchronous switches between active low and tri-state.

EQUIVALENT CIRCUIT DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power supply voltage	V_{DD}	0.0 to 4.0	V
Voltage on any pin with GND = 0 volts	V_I	-0.3 to $V_{DD} + 0.3$	V
Power dissipation	P_D	600	mW
Operating temperature	T_a	-40 to +85	°C
Storage temperature	T_{STG}	-65 to +150	°C

ELECTROSTATIC CHARACTERISTICS

Characteristics	Pin No.	ESD level	Unit
Human Body Model	All	$<\pm 2000$	V
Machine Model	All	$<\pm 300$	V
Charge Device Model	All	$<\pm 800$	V

NOTE: These devices are ESD sensitive. These devices must be handled in an ESD protected environment.

ELECTRICAL CHARACTERISTICS(V_{DD}=3.0V, V_p=3.0V, T_a = 25°C, unless otherwise specified.)

Characteristic		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V _{DD}		2.7	3.0	4.0	V
		V _P		V _{DD}	3.0	4.0	
Power supply current	S1M8836 RF+IF	I _{DD}	Fractional-N mode (f _{osc} =19.68MHz, RF R=2)		5.5		mA
	S1M8837 RF+IF				7.5		
	Quiescent State			4.0			
	S1M8836 RF+IF			6.0			
	S1M8837 RF+IF			1.5			
IF only							
Power down current		I _{PWDN}	V _{DD} =3.0V		1	10	μA
Digital Inputs: CLOCK, DATA and LE							
High Level Input Voltage		V _{IH}	V _{DD} =2.7V to 4.0V	0.7V _D			V
Low Level Input Voltage		V _{IL}	V _{DD} =2.7V to 4.0V			0.3V _D	V
High Level Input Current		I _{IH}	V _{IH} =V _{DD} =4.0V	-1.0		+1.0	μA
Low Level Input Current		I _{IL}	V _{IL} =0V, V _{DD} =4.0V	-1.0		+1.0	μA
Reference Oscillator Input: OSC_{in}							
Input Current		I _{IHR}	V _{IH} =V _{DD} =4.0V			+100	μA
		I _{IILR}	V _{IL} =0V, V _{DD} =4.0V	-100			μA
Digital Output: foLD							
High Level Output Voltage		V _{OH}	I _{out} =-500μA	V _{DD} -0.4			V
Low Level Output Voltage		V _{OL}	I _{out} =+500μA			0.4	V

ELECTRICAL CHARACTERISTICS (Continued)

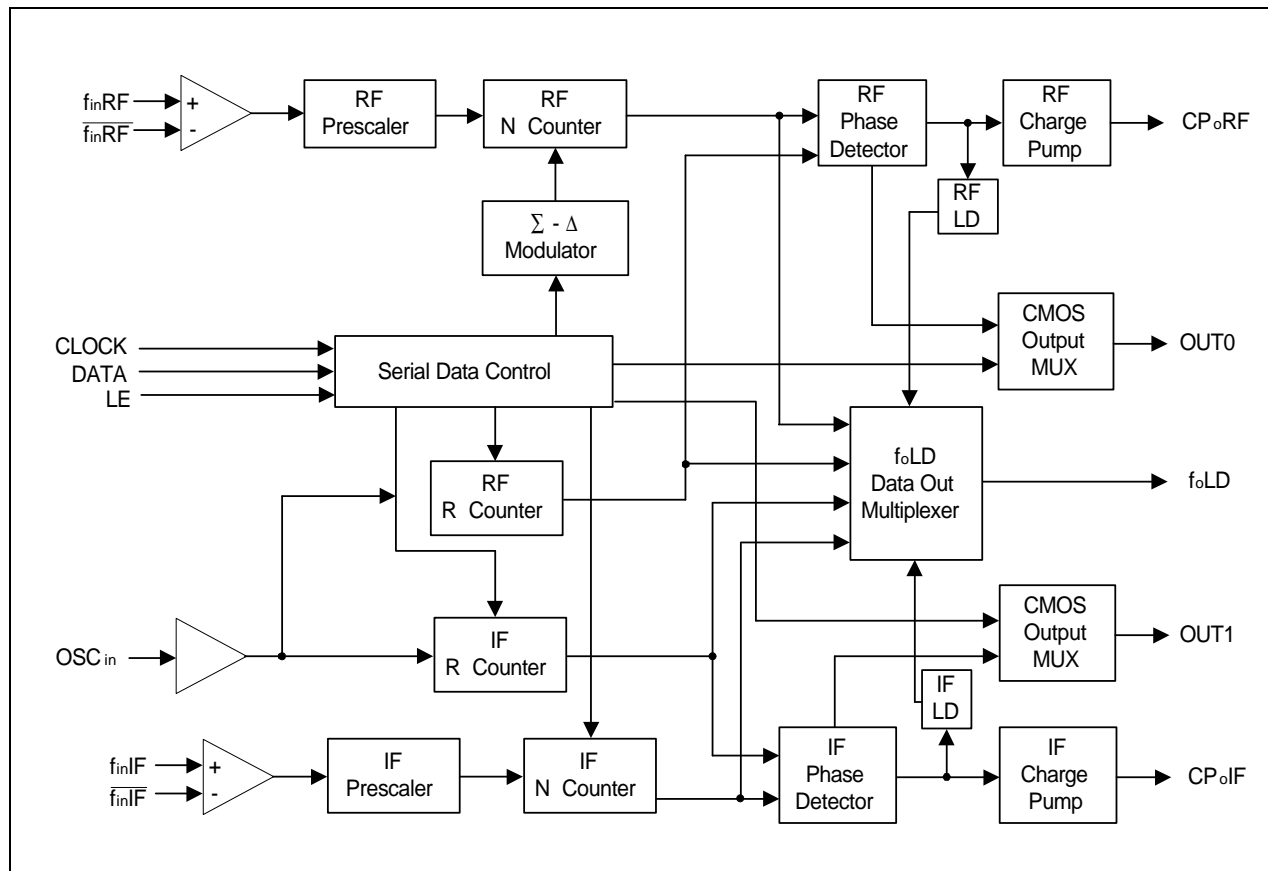
($V_{DD}=3.0V$, $V_p=3.0V$, $T_a = 25^\circ C$, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Charge Pump Outputs: CP_oRF, CP_oIF							
RF Charge Pump Output Current	I_{CPRF} SOURCE _{min}	$V_{CP}=V_p/2$, RF_CP_WORD=0000		-50		μA	
	I_{CPRF} SINK _{min}	$V_{CP}=V_p/2$, RF_CP_WORD=0000		+50		μA	
	I_{CPRF} SOURCE _{max}	$V_{CP}=V_p/2$, RF_CP_WORD=1111		-800		μA	
	I_{CPRF} SINK _{max}	$V_{CP}=V_p/2$, RF_CP_WORD=1111		+800		μA	
IF Charge Pump Output Current	I_{CPRF} SOURCE _{min}	$V_{CP}=V_p/2$, CP_GAIN_8=0		-100		μA	
	I_{CPRF} SINK _{min}	$V_{CP}=V_p/2$, CP_GAIN_8=0		+100		μA	
	I_{CPRF} SOURCE _{max}	$V_{CP}=V_p/2$, CP_GAIN_8=1		-800		μA	
	I_{CPRF} SINK _{max}	$V_{CP}=V_p/2$, CP_GAIN_8=1		+800		μA	
Charge Pump Leakage Current	I_{CPL}	$0.5V \leq V_{CP} \leq V_p - 0.5V$	-2.5		+2.5	nA	
Sink vs. Source Mismatch	$I_{CP-SINK}$ vs $I_{CP-SOURCE}$	$V_{CP}=V_p/2$		3	10	%	
Output Current Magnitude Variations. Voltage	I_{CP} vs V_{CP}	$0.5V \leq V_{CP} \leq V_p - 0.5V$		10	15	%	
Output Current vs. Temperature	I_{CP} vs T_a	$V_{CP}=V_p/2$		10		%	
Operating Frequency, Input Sensitivity (Programmable Divider, PFD)							
RF Operating Frequency	S1M8837	f_{inRF}	Fractional-N mode ($f_{osc}=19.68MHz$, RF R=2)	0.5		2.5	GHz
	S1M8836		Fractional-N mode ($f_{osc}=19.68MHz$, RF R=2)	0.25		1.0	GHz
IF Operating Frequency	f_{inIF}	$V_{DD}=3.0V$		45		520	MHz
Reference Oscillator Input Frequency	OSC _{in}			2		40	MHz
Phase Detector Operating Frequency	f_{PD}					10	MHz
RF Input Sensitivity	P_{finRF}	$V_{DD}=3.0V$		-15		0	dBm
		$V_{DD}=4.0V$		-10		0	dBm
IF Input Sensitivity	P_{finIF}	$V_{DD}=2.7V$ to $4.0V$		-10		0	dBm
Reference Oscillator Input Sensitivity	V_{OScin}			0.5		V_{DD}	V_{PP}

ELECTRICAL CHARACTERISTICS (Continued)(V_{DD}=3.0V, V_p=3.0V, T_a = 25°C, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Serial Data Control						
CLOCK Frequency	f _{CLOCK}				10	MHz
CLOCK Pulse Width High	t _{CWH}		50			ns
CLOCK Pulse Width Low	t _{CWL}		50			ns
DATA Set Up Time to CLOCK Rising Edge	t _{DS}		50			ns
DATA Hold Time after CLOCK Rising Edge	t _{DH}		10			ns
LE Pulse Width	t _{LEW}		50			ns
CLOCK Rising Edge to LE Rising Edge	t _{CLE}		50			ns

FUNCTIONAL DESCRIPTION



The Samsung S1M8836/37 is RF/IF dual frequency synthesizer IC which supports Fractional-N mode for RF PLL and Integer-N mode for IF PLL depending on a program control. S1M8836/37 combined with an external LPF and an external VCO forms PLL frequency synthesizer. The frequency synthesizer consists of prescalers, pulse-swallowed programmable N counters, programmable reference R counters, phase detectors, programmable charge pumps, analog LD(lock detector), serial data control, etc.

An input buffer in the prescaler amplifies the RF input power of -10dBm from the external RF/IF VCO to the sufficient ECL switching level to drive the following ECL divider so that it can be normally operated even in a smaller input power less than -10dBm. The amplified VCO output signal is divided by the prescaler with a pre-determined divide ratio (div. 8/9/12/13 for S1M8836, div. 16/17/20/21 for S1M8837, div. 8/9 for IF), the N counter and the Fractional-N circuitry ($\Sigma - \Delta$ modulator). External reference signal is divided by the R counter to set the comparison frequency of the PFD. The divide ratios of the programmable counters can be programmed via the serial bus interface. These two signals drive the both inputs of the phase detector. The phase detector drives the charge pump by comparing frequencies and phases of the above two signals. The charge pump and the external LPF make the control voltage for the external VCO and finally the VCO generates the appropriate frequency signal.

When the PLL is in the locked state, the RF VCO's frequency will be $N_{INT} + N_{FRAC}$ times the comparison frequency, where N_{INT} is the integer divide ratio and N_{FRAC} is the fractional component.

The S1M8836/37 has new improved features compared to conventional Integer-N PLLs.

The fractional-N PLL is available for the RF. The fractional synthesis frequency as is AMPS and IS-95A/B/C. This makes it possible to widen the loop bandwidth as wide as 20kHz or wider for a faster lock-up time and to improve the in-band phase noise performance due to the reduced divide ratio N. Such S1M8836/37 in the fractional-N mode is suitable for CDMA, GSM and PCS band applications.

Also, from the programmability of the charge pump, the users can easily design a stable loop by free selection of loop components and reach to the low spurious, the low power PLL by an optimized current selection.

Prescaler

The RF/IF prescaler consists of a differential input buffer and ECL frequency dividers. The input buffer amplifies the input signal from the external VCO to the required level set by sensitivity requirements. The output of the amplifier delivers a differential signal to the divider with the correct DC level. The buffer may be either single-ended or differentially driven. The single-ended operation is preferred in typical applications due to external VCO. In this case, we recommend that the complementary input /fin of the input buffer be AC coupled to ground through external capacitors, even though it is internally coupled to ground via an internal 10pF capacitor. The other input pin fin of the buffer also needs external capacitor for decoupling the DC component and controlling the input power level.

The RF prescalers of S1M8836 and S1M8837 provide 8/9/12/13 and 16/17/20/21 prescaler ratio, respectively. The IF prescaler of S1M8836/37 contains 8/9 dual modulus prescaler.

Reference Oscillator Inputs

The reference oscillator frequency is provided by an external reference such as TCXO through the OSC_{in} . It drives both the IF R and RF R counters.

Programmable Dividers (RF/IF N Counters)

The RF N counter can be configured as a fractional counter. The fractional-N counter is selected when the $Frac-N_SEL$ bit becomes HIGH.

In the fractional mode, the S1M8836 is capable of offering a continuous integer divide range from 25 to 1023 and the S1M8837 offering a continuous integer divide range from 49 to 2047.

The S1M8836/37 IF N counter supports an integer counter mode only, not including fractional counter, and is capable of operating from 45MHz to 520MHz offering a continuous integer divide range from 72 to 32767.

Σ - Δ modulator

The RF part of S1M8836/37 adopts the Σ - Δ modulator as a core of the fractional counter that makes it possible to obtain divide ratio N to be a fractional number between two contiguous integers. The Σ - Δ modulator effectively randomizes the quantization noise generated from digitizing process and results in extreme suppression of in-band noise power by pushing it out to out-of-band as in conventional Σ - Δ data converter. This technique eliminates the need for compensation current injection into the loop filter and improves fractional spurious performance, suitable for high-tier applications.

The Σ - Δ modulator operates only for fractional-N mode, when the Frac-N_SEL is HIGH.

For proper use of the fractional mode, the user should be kept in mind that

1. A fractional number should be set in the range from -0.5 to 0.5 in step of 1/62976.
2. For S1M8836/7, R can be selected 1-3. The clock frequency fixed at 9.84MHz (=19.68MHz/2, R=2) is recommended for the Σ - Δ modulator which is an optimum condition for achieving good electrical performances related to the fractional noise and power consumption. Only when using this clock frequency, the S1M8836/37 guarantees the exact frequency resolutions: 10kHz for CDMA PCS and 30kHz for CDMA cellular.

Note that the clock frequency much lower than 9.84MHz can deteriorate the fractional noise performance.

Users can use R=1 or R=3, too. For the case of R=1 or R=3, users must ask SAMSUNG for details.

Fractional noise performance may become better for R=1 (clock frequency=19.68MHz/1=19.68MHz). But the RF operating frequency range may be shrunk for that case of R=1.

Phase-Frequency Detector (PFD) and Charge Pump (CP)

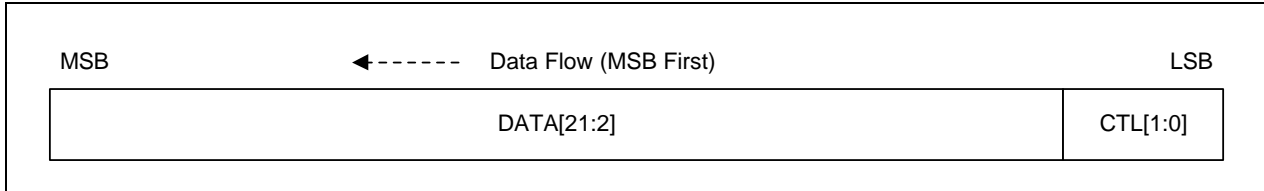
The RF/IF phase detector composed of PFD and CP outputs pump current into an external loop filter in proportional to the phase difference between outputs of N and R counter. The phase detector has a better linear transfer characteristic due to a feedback loop to eliminate dead zone. The polarity of the PFD can be programmed using RF_PFD_POL/IF_PFD_POL depending on whether RF/IF VCO characteristics are positive or negative. (Programmable descriptions for phase detection polarity)

Power-Down(or Power-Save) Control

Each PLL is individually power controlled by the enable pins (RF_EN and IF_EN pins) or program control bits (PWDN, PWDN_RF/IF). The enable pins override the program control bits. When both enable pins are HIGH, the program control bits determine the state of power control. Power down forces all the internal blocks to be deactivated and the charge pump output to be in the TRISTATE. The control register, however, remains active for serial programming and is capable of loading and latching in data during the power down.

Programming Description

The S1M8836/37 can be programmed via the serial bus interface. The interface is made of 3 functional signals: clock, data, and latch enable(LE). Serial data is moved into the 22-bit shift register on the rising edge of the clock. These data enters MSB first. When LE goes HIGH, data in the shift register is moved into one of the 4 latches (by the 2-bit control).



Control Bit Map (CTL[1:0])

Control Bits		DATA Location
CTL2(CTL[1])	CTL1(CTL[0])	
0	0	WORD1
0	1	WORD2
1	0	WORD3
1	1	WORD4

Data Bit Map (DATA[21:2])

	REGISTER BIT LOCATION																				Last Bit		
	First Bit		21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4			3
WORD1(W1)	IF_CTL_WORD		RF_R (2Bit)		IF_R_CNTR(15Bit)															0 0			
WORD2(W2)	CMOS		IF_CP_WORD		IF_NB_CNTR(12Bit)												IF_NA_CNTR(3Bit)			0 1			
WORD3(W3)	FoLD(4Bit)				RF_CP_WORD				RF_NB_CNTR(7Bit)					RF_NA_CNTR (36:3Bit)				RF_NA_CNTR (37:4Bit)				1 0	
WORD4(W4)	RF_CTL_WORD		FRAC_CNTR(17Bit)																	1 1			

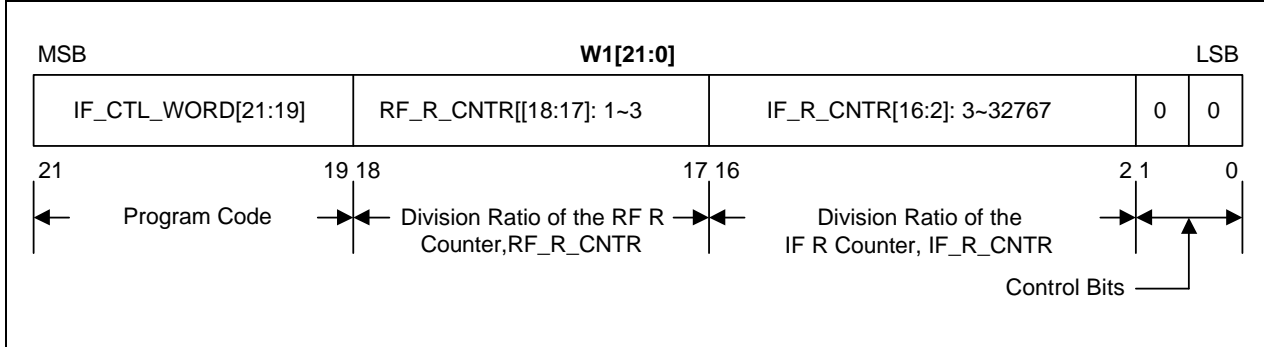
Data Bit Map (DATA[21:2]) (Continued)

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
IF_CTL_WORD	W1[21]	IF_CNT_RST	normal operation	IF counter reset	IF
	W1[20]	PWDN_IF	power up	power down	IF
	W1[19]	PWDN	asynchronous power down	synchronous power down	RF and IF
CMOS	W2[21]	Speedy_Lock	CMOS output	Speedy_Lock mode	
	W2[20]	OUT1	voltage LOW	voltage HIGH	pin #23
	W2[19]	OUT0	voltage LOW	voltage HIGH	pin #24
IF_CP_WORD	W2[18]	IF_CP_GAIN	1X	8X	IF charge pump
	W2[17]	IF_PFD_POL	negative slope	positive slope	IF PFD
foLD	W3[21:18]	foLD	select LDs and monitoring mode of internal counters. (FoLD control for control codes in detail)		Lock Detector(LD), Test mode
RF_CP_WORD	W3[17:14]	RF_CP_LVL	select 16-level charge pump current (RF charge pump gain for control codes in detail)		RF charge pump
	W3[13]	RF_PFD_POL	negative slope	positive slope	RF PFD
RF_CTL_WORD	W4[21]	RF_CNT_RST	normal operation	RF counter reset	RF
	W4[20]	PWDN_RF	power up	power down	RF
	W4[19]	Frac-N_SEL	Integer-N mode	Fractional-N mode	RF; PLL mode selection

- Counter Reset mode resets R & N counters.
- IF charge pump current can be selected to high current(8X) or low current(1X) mode.
- In the Speedy_Lock mode, the OUT0 and OUT1 pins can be utilized as synchronous switches between active low and tri-state. The Speedy_Lock mode activates the OUT0 and OUT1 pins to be connected to GROUND with a low impedance(< 150Ω) while a high charge pump gain(≥ 8X) is selected and otherwise to the TRISTATE.
- For using a programmable CMOS output, the CMOS output bit(W2[21]=L) should be activated and then the desired logic level should be programmed with the control bits W2[19] for OUT0 and W2[20] for OUT1.

Programmable Reference Counter(W1[18:2])

If the Control Bit is 00, data is moved from the 22-bit shift register into the R-latch which sets the IF reference counter. Serial data format is shown in the table below.



• **15-Bit IF R Counter Division Ratio**

Division ratio : 3 to 32767(The divide ratios less than 3 are prohibited)
Data are shifted in MSB first.

Division Ratio	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

• **RF R Counter Division Ratio**

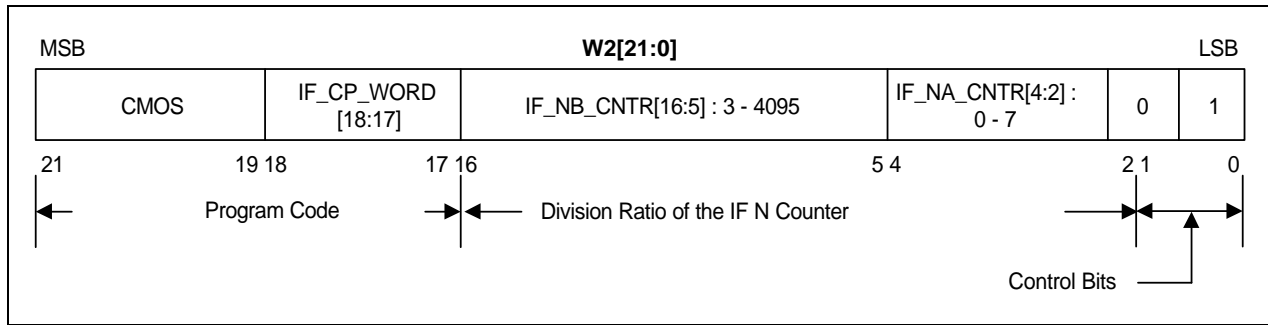
Division ratio : 1 to 3

Division Ratio	1	0
1	0	0
1	0	1
2	1	0
3	1	1

Programmable Counter(N Counter)

If the Control Bits are 01(IF), 10, and 11(RF), data is transferred from the 22-bit shift register into the N/Frac-latch. N Counter consists of swallow counter(A counter; 3-bit for IF & S1M8836RF and 4-bit for S1M8837RF), main counter(B counter; 7-bit for S1M8836/37 RF and 12-bit for IF), and fractional counter(F counter; 17-bit for S1M8836/37 RF). Serial data format is shown below.

IF N Counter



• **IF Main Counter Division Ratio(B Counter)**

IF_NB_CNTR[16:5] ; for S1M8836/37

Division Ratio(B)	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Division ratio: 3 to 4095 (The division ratios less than 3 are prohibited)

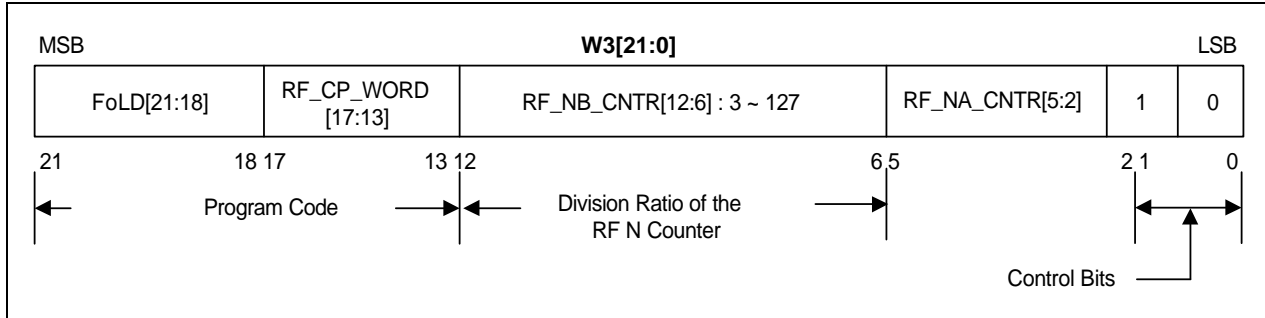
• **Swallow Counter Division Ratio (A Counter)**

IF_NA_CNTR[4:2] ; for S1M8836/37

Division Ratio(A)	2	1	0
0	0	0	0
1	0	0	1
•	•	•	•
7	1	1	1

Division Ratio: 0 to 7, B>A

RF N Counter



- RF Main Counter Division Ratio (B Counter)**

RF_NB_CNTR[12:6] ; for S1M8836/37

Division Ratio(B)	6	5	4	3	2	1	0
3	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•
7	1	1	1	1	1	1	1

Division ratio : 3 to 127 (The division ratios less than 3 are prohibited)

- RF Swallow Counter Division Ratio (A Counter)**

RF_NA_CNTR[5:2] ; for S1M8836

Division Ratio(A)	3	2	1	0
0	X	0	0	0
1	X	0	0	1
•	•	•	•	•
7	X	1	1	1

Division Ratio : 0 to 7

X = Don't care condition

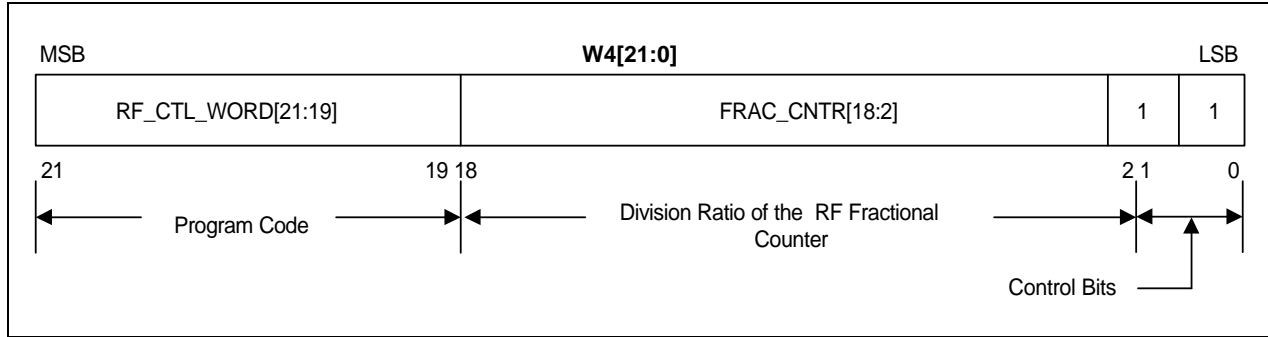
RF_NA_CNTR[5:2] ; for S1M8837

Division Ratio(A)	3	2	1	0
0	0	0	0	0
1	0	0	0	1
•	•	•	•	•
15	1	1	1	1

NOTE: Division Ratio: 0 to 15

X = Don't care condition

RF Fractional Counter



• **RF Fractional Counter Value (F Counter)**

FRAC_CNTR[18:2] ; for S1M8836/37 RF

Counter Value (F)	F 16	F 15	F 14	F 13	F 12	F 11	F 10	F 9	F 8	F 7	F 6	F 5	F 4	F 3	F 2	F 1	F 0
31488	0	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
-31488	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

F Counter Value: -31488(2's complementary) to 31488

NOTE: For a negative integer, the counter value should be inputted as the corresponding 2's complementary binary code.

For instance, the 2's complementary binary code of -2 is 1 1111 1111 1111 1110.

Programmable PFD and Charge Pump**IF Charge Pump Gain (IF_CP_WORD; W2[18])**

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
IF_CP_WORD	W2[18]	IF_CP_GAIN	1x (100 μ A)	8x (800 μ A)	IF charge pump

RF Charge Pump Gain (RF_CP_WORD; W3[17:14])

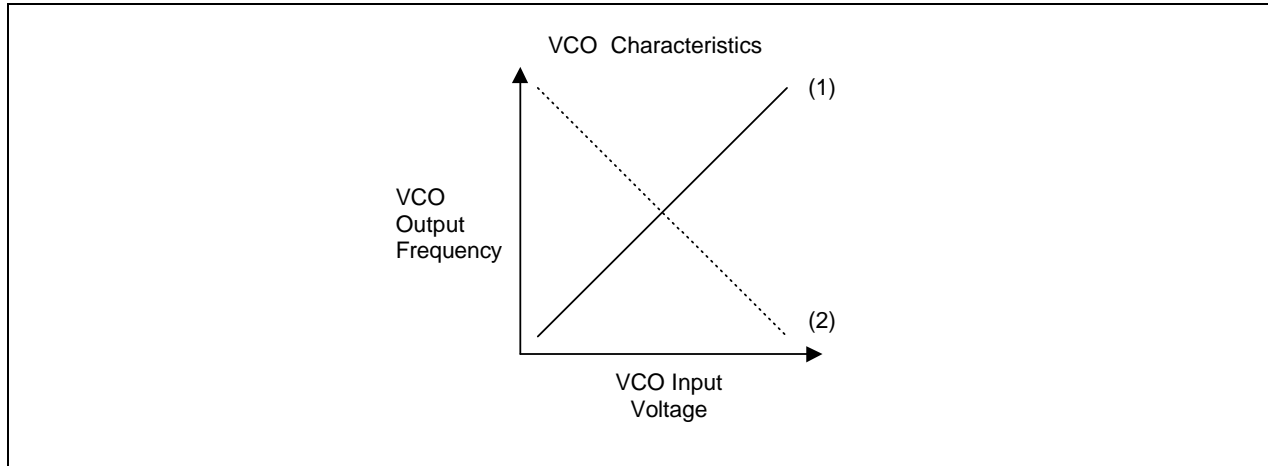
Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
RF_CP_WORD	W3[17:14]	RF_CP_LVL	select 16-level charge pump current		RF charge pump

Ic _{po} (μ A)	8X	4X	2X	1X
	W3[17]	W3[16]	W3[15]	W3[14]
50	0	0	0	0
100	0	0	0	1
•	•	•	•	•
200	0	0	1	1
250	0	1	0	0
•	•	•	•	•
400	0	1	1	1
450	1	0	0	0
•	•	•	•	•
800	1	1	1	1

Phase Detector Polarity (RF_CP_WORD/IF_CP_WORD; W3[13]/W2[17])

Depending on VCO characteristics, W2[17] and W3[13] bits should be set as follows :

Control bits	LOW (0)	HIGH (1)	Comments
W2[17]	Negative Slope	Positive Slope	IF PFD
W3[13]	Negative Slope	Positive Slope	RF PFD



Program Mode Control

Power down mode operation

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
IF_CTL_WORD	W1[20]	PWDN_IF	power up	power down	IF
	W1[19]	PWDN	asynchronous power down	synchronous power down	RF and IF
RF_CTL_WORD	W4[20]	PWDN_RF	power up	power down	RF

Each PLL is individually power controlled by the enable pins (RF_EN and IF_EN pins) or program control bits (PWDN, PWDN_RF/IF). The enable pins override the program control bits. When both enable pins are HIGH, the program control bits determine the state of power control. Power down forces all the internal analog blocks to be deactivated and the charge pump output to be in a TRISTATE. The oscillator buffer is powered down when the power down bits (W4[20] and W1[20]) become HIGH. The control register and R/N counters, however, remains active for permitting serial programming and is capable of loading and latching in data during the power down.

There are synchronous and asynchronous power-down modes for S1M8836/37. The power-down bit W1[19] is used to select between synchronous and asynchronous power-down. Synchronous power-down mode occurs if W1[19] bit is HIGH and then the power down bit (W4[20] or W1[20]) becomes HIGH. In the synchronous power down mode, the power-down function will go into power-down mode upon the completion of a charge pump pulse event because it is synchronized with the charge pump and thus can diminish undesired frequency jumps. Asynchronous power down mode occurs if W1[19] bit is LOW and then the power down bit (W4[20] or W1[20]) becomes HIGH. Activation of the asynchronous function will go into power-down mode immediately.

RF Power down mode table

W4[20]	W1[19]	Power down mode status
0	0	RF PLL active
0	1	RF PLL active, only charge pump to TRISTATE
1	1	Asynchronous power down
1	0	Synchronous power down



IF Power down mode table

W1[20]	W1[19]	Power down mode status
0	0	IF PLL active
0	1	IF PLL active, only charge pump to TRISTATE
1	0	Asynchronous power down
1	1	Synchronous power down

Programmable Counter Reset Control

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
IF_CTL_WORD	W1[21]	IF_CNT_RST	normal operation	IF counter reset	IF
RF_CTL_WORD	W4[21]	RF_CNT_RST	normal operation	RF counter reset	RF

Counter Reset mode resets R & N counters.

RF Fractional-N selection

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
RF_CTL_WORD	W4[19]	Frac_N_SEL	reserved	Fractional-N mode	RF;PLL mode selection

CMOS Output Control

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
CMOS	W2[21]	Speedy Lock	CMOS output	Speedy Lock mode	
	W2[20]	OUT1	voltage LOW	voltage HIGH	pin #23
	W2[19]	OUT0	voltage LOW	voltage HIGH	pin #24

In the Speedy Lock mode, the OUT0 and OUT1 pins can be utilized as synchronous switches between active low and a tri-state. The Speedy Lock mode activates the OUT0 and OUT1 pins to be connected to GROUND with a low impedance (< 150Ω) while a high charge pump gain (≥ 8X) is selected and otherwise to a tri-state. For using a programmable CMOS output, the CMOS output bit (W2[21]= LOW) should be activated and then the desired logic level should be programmed with the control bits W2[19] for OUT0 and W2[20] for OUT1.

foLD Control

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
foLD	W3[21:18]	foLD	select LDs monitoring mode of internal counters.		Lock Detector (LD), Test mode

foLD[3]	foLD[2]	foLD[1]	foLD[0]	foLD Output State
0	0	0	0	Disabled(default LOW)
0	0	0	1	RF and IF Analog Lock Detect
0	0	1	0	Reserved Test Mode
0	0	1	1	Reserved Test Mode
X	1	0	0	Reserved Test Mode
X	1	0	1	IF R Counter Output
X	1	1	0	IF N Counter Output
X	1	1	1	RF R Counter Output
1	0	0	0	RF N Counter Output
1	0	0	1	Reserved Test Mode
1	0	1	0	Reserved Test Mode
1	0	1	1	Reserved Test Mode

- When the PLL is locked and the analog lock detect mode is selected, the foLD output is HIGH, with narrow pulses LOW.

Lock Detector(LD)

There is analog mode for S1M8836/37. The foLD bits, W3[21:18], are used to select the lock detection mode and to output the selected lock signal through the foLD pin.

The foLD output becomes HIGH with narrow pulsed LOW while both RF and IF PLLs are locked and thereby the output should be low-pass filtered for a DC locked voltage HIGH.

PULSE SWALLOW FUNCTION

The RF VCO' frequency f_{VCO} becomes $N_{INT} + N_{FRAC}$ times the comparison frequency(f_{OSC}/R) where N_{INT} is the integer divide ratio and N_{FRAC} is the fractional component;

$$f_{VCO} = (N_{INT} + N_{FRAC}) \times f_{OSC}/R = N \times f_{OSC}/R$$

$$\text{where } N_{INT} = P \times B + A$$

RF PLL: $N_{FRAC} = F/62976$, $-31488 \leq F \leq 31488$, and $R = 1, 2, 3$ (typically 2)

IF PLL: $N_{FRAC} = 0$, $B > A$ and $3 \leq R \leq 32767$

f_{VCO} : External VCO output frequency

f_{OSC} : External reference frequency(From external oscillator)

R: Preset divide ratio of programmable R counter (RF: 1, 2, 3(typically 2), IF: 3 to 32767);

P: Preset modulus of quadruple modulus prescaler (S1M8836 RF:P=8, S1M8837 RF:P=16, IF:P=8)

B: Preset value of main counter (S1M8836/37 RF: 3 to 127, IF: 3 to 4095)

A: Preset value of swallow counter division ratio
(S1M8836 RF: $0 \leq A \leq 7$, S1M8837 RF: $0 \leq A \leq 15$. IF: $0 \leq A \leq 7$, $A < B$)

N_{FRAC} : Fractional component of Pulse-swallowed division ratio N (for IF: $N_{FRAC} = 0$)

F: Preset value of fractional register($-31488 \leq F \leq 31488$); For a negative integer, F should be inputted as its 2's complementary binary code.

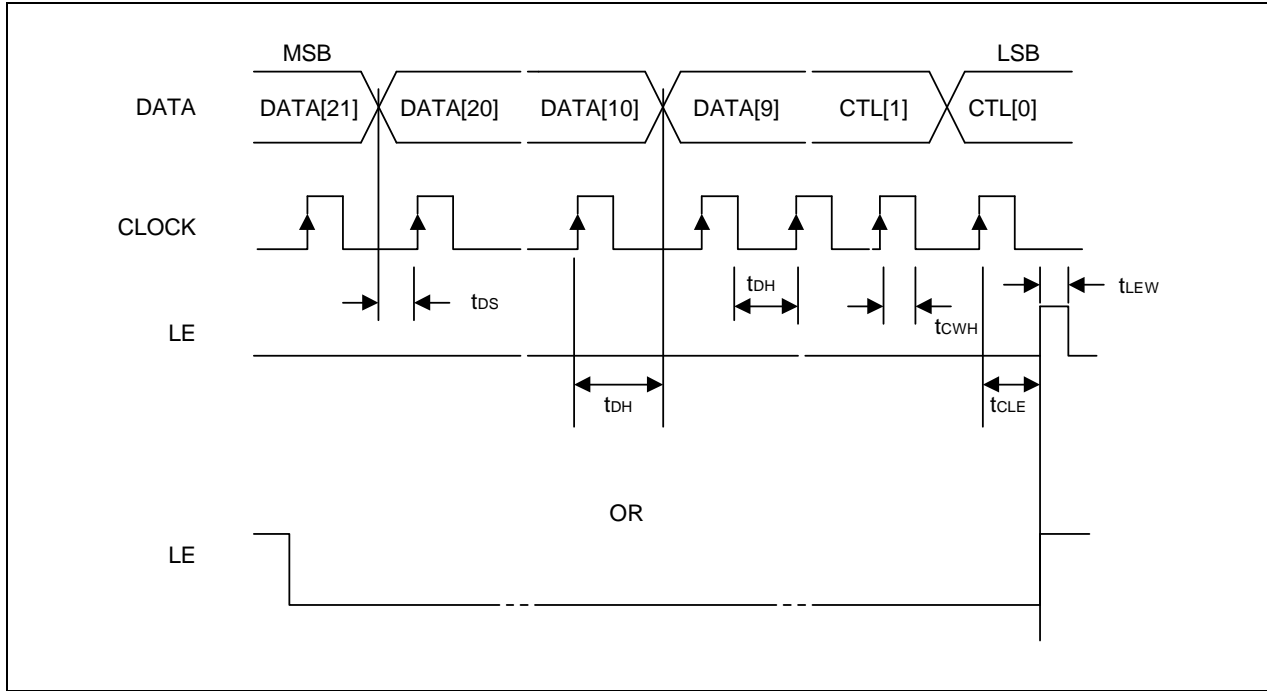
For examples in S1M8836 fractional-N mode ($f_{OSC}=19.68\text{MHz}$, $R=2$, $P=8$)

- 1) for $f_{VCO} = 955.02\text{MHz}$; $N = 97.05487805$, $B=12$, $A=1$, $F=3456$ (= 0 0000 1101 1000 0000)
- 2) for $f_{VCO} = 955.03\text{MHz}$; $N = 97.05589431$, $B=12$, $A=1$, $F=3520$
- 3) for $f_{VCO} = 956.25\text{MHz}$; $N = 97.17987805$, $B=12$, $A=1$, $F=11328$
- 4) for $f_{VCO} = 979.35\text{MHz}$; $N = 99.52743902$, $B=12$, $A=4$, $F=-29760$

For examples in S1M8837 fractional-N mode ($f_{OSC}=19.68\text{MHz}$, $R=2$, $P=16$)

- 1) for $f_{VCO} = 1620.87\text{MHz}$ (CH25) ; $N = 164.722561$, $B=10$, $A=5$, $F=-17472$ (= 1 1011 1011 1100 0000)
- 2) for $f_{VCO} = 1620.88\text{MHz}$; $N = 164.7235772$, $B=10$, $A=5$, $F=-17408$
- 3) for $f_{VCO} = 1622.12\text{MHz}$ (CH50) ; $N = 164.8495935$, $B=10$, $A=5$, $F=-9472$
- 4) for $f_{VCO} = 1632.12\text{MHz}$ (CH250) ; $N = 165.8658537$, $B=10$, $A=6$, $F=-8448$
- 5) for $f_{VCO} = 1648.37\text{MHz}$ (CH575) ; $N = 167.5172764$, $B=10$, $A=8$, $F=-30400$

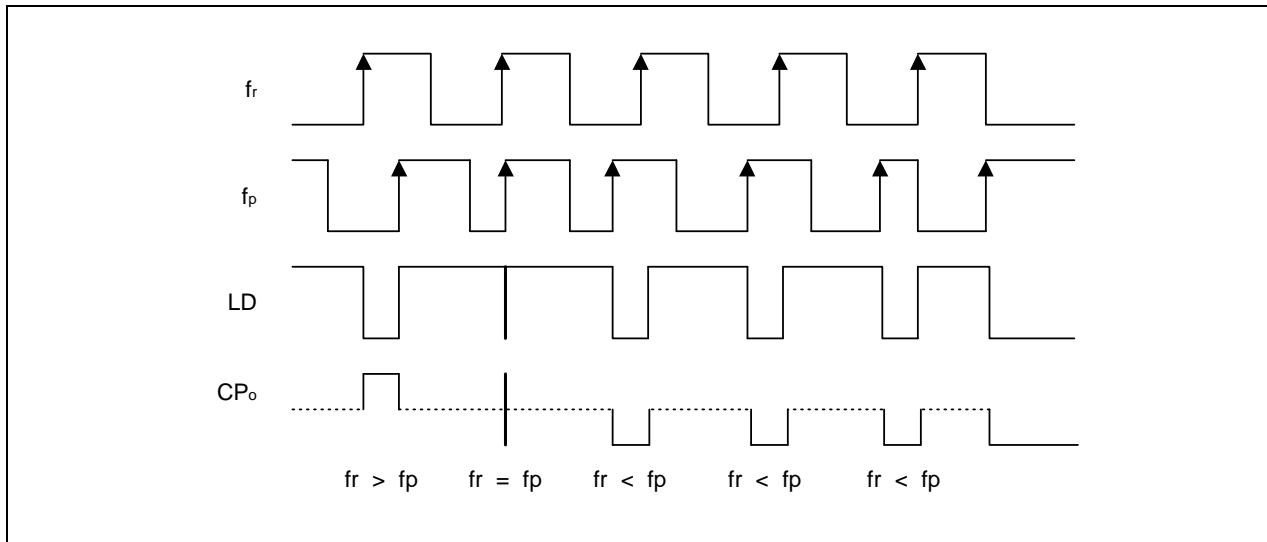
Serial Data Input Timing



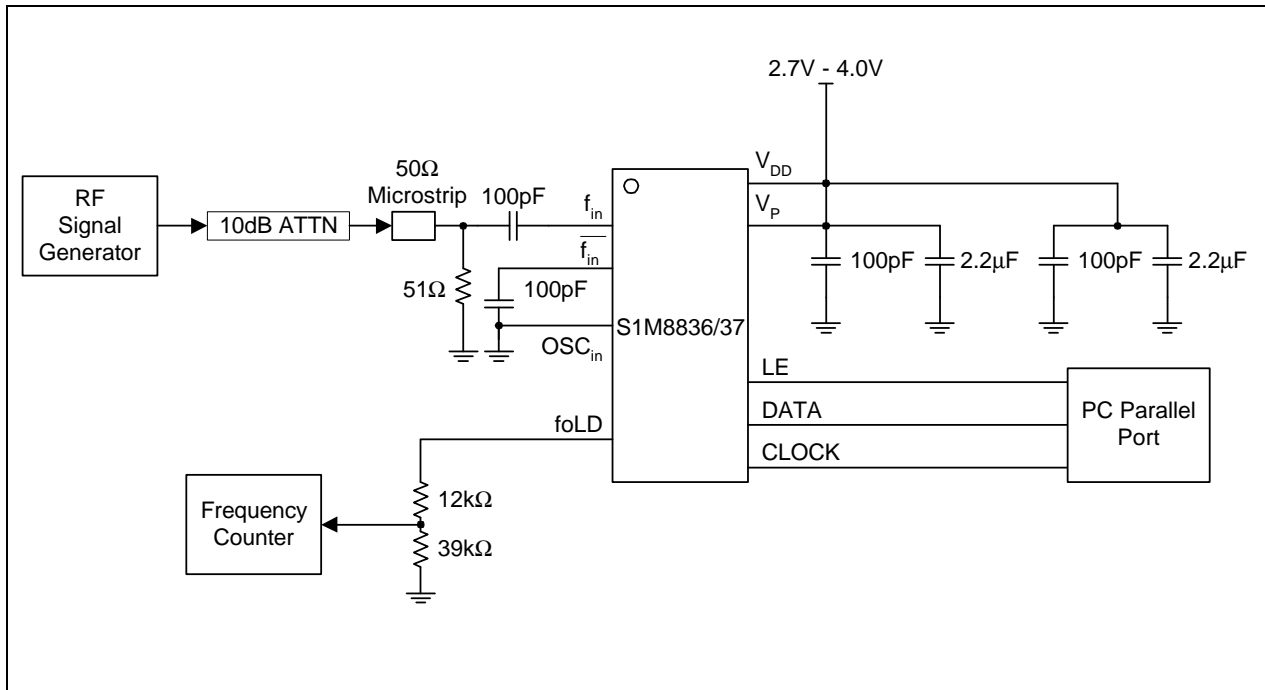
Phase Detector and Charge Pump Characteristics

Phase difference detection Range : -2π to $+2\pi$

When the positive-slope polarity of PFD is selected, $W2[17]=HIGH$ or $W3[13]=HIGH$;

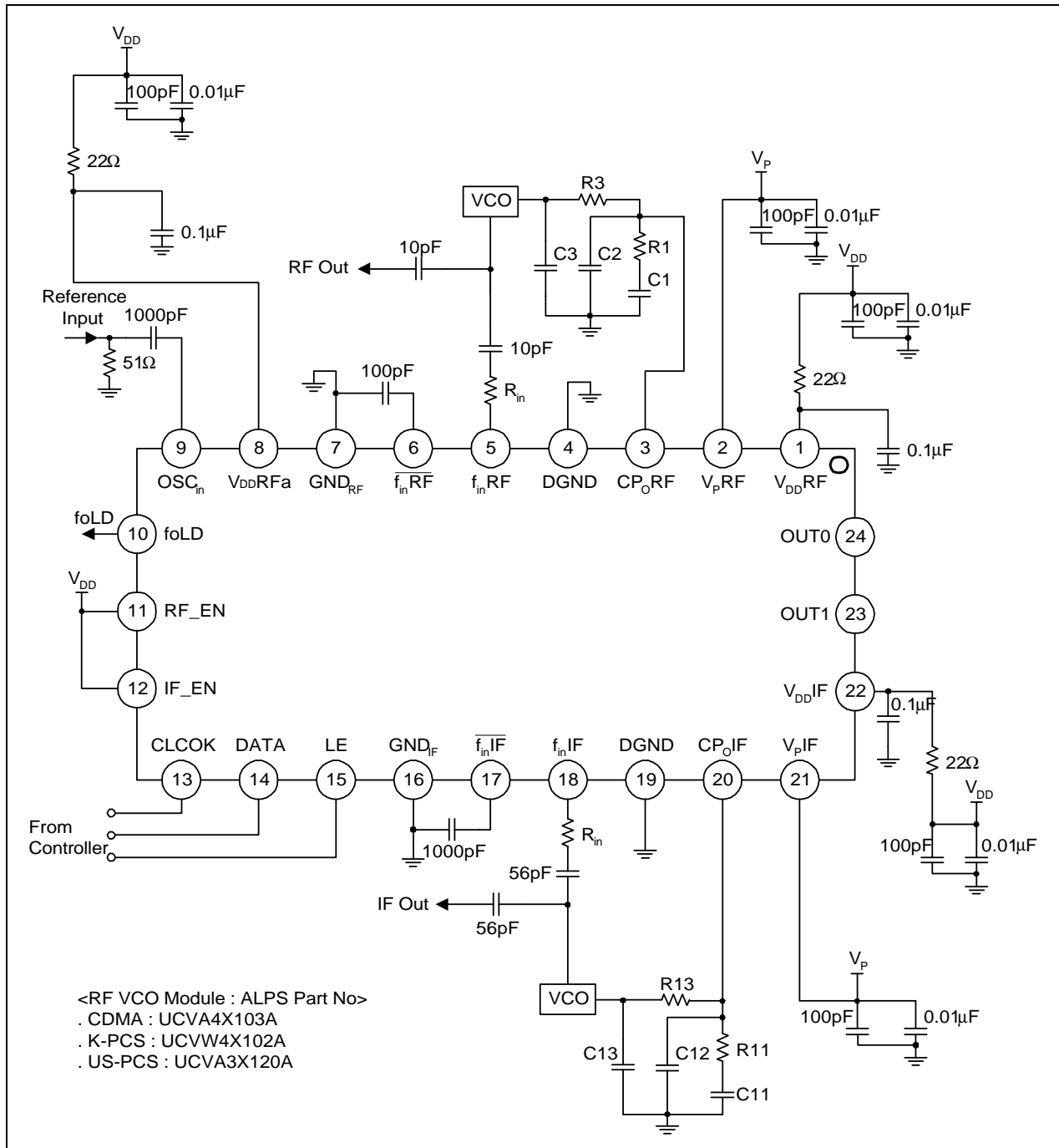


SIMPLIFIED SCHEMATIC DIAGRAM FOR RF SENSITIVITY TEST



- Sensitivity limit is determined when the error of the divided RF output (foLD) becomes 10Hz.
- $f_{VCO} = 1.0\text{GHz}$, $N = 100$, $P = 8$, $R = 2$ in S1M8836 Integer-N test mode
- $f_{VCO} = 2.1\text{GHz}$, $N = 210$, $P = 16$, $R = 2$ in S1M8837 Integer-N test mode Typical Application Example

TYPICAL APPLICATION CIRCUIT



— The role of Rin : Rin makes a large portion of VCO output power go to the load rather than the PLL. The value of Rin depends on the VCO power level

PCB LAYOUT GUIDE

In doing PCB layouts for S1M8836/37, we recommend that you apply the following design guide to your handsets, thus improving the phase noise and reference spurious performances of the phones.

1. The S1M8836/37 has external four power supply pins to supply on-chip bias, each for analog and digital blocks of RF and IF PLLs. Basically in doing PCB layout, it is important that power supply lines should be separated from one another and thus coupling noises through the voltage supply lines can be minimized. If you have some troubles with the direction to separate, you can choose the following recommendations for your convenience;
 - Tying analog power lines, V_{DDRF} and V_{DDIF} , is possible.
 - Tying digital power lines, V_{P1} and V_{P2} , is possible.
 - A point connecting the analog and digital power lines should be near to battery line as close as possible. It minimizes coupling noise effects from a digital switching noise into analog blocks. We also recommend that a passive RC low pass filter($R(22\Omega), C(100nF)$) be utilized for suppressing high frequency noise on the analog power supply line and reducing any digital noise couplings.
2. VCO power lines should be well separated from those of PLL because VCO is generally a very sensitive device from power line noises and PLL is a digital noise generator.
3. For more improvement of reference spurious performance, it is recommended that the LPF ground be tied to the PLL ground, not the VCO ground.

PACKAGE DIMENSIONS

