INTRODUCTION

S1M8673 is an integrated receiver chip intended for use in cellular phones operating in IS-95 AMPS/CDMA applications.

This device incorporates all the components required to implement the receiver RF front-end except the filter blocks. It has a Low Noise Amplifier (LNA) and a Mixer.

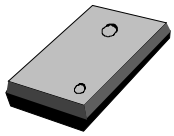
LNA has a single-ended input and a single-ended output for the RF Surface Acoustic Wave (SAW) filter. RF Mixer, of which output is balanced, is followed by an IF SAW filter.

The noise figure, gain, and IP3 of each stage in the receiver chip are optimized to meet the system requirements for AMPS/CDMA mode as per IS-98A. Using 0.5um silicon BiCMOS technology, the S1M8673 has been designed for high performance and low cost applications.

The device package and pins are shown in Figure 1. A block diagram of the S1M8673 is shown in Figure 2.

20-eTSSOP-BD44

24-QFN-3.5×4.5



FEATURES

- Supports cellular CDMA/AMPS mode.
- On-chip High IIP3 (+4dBm) Low Noise Amplifier.
- Low noise, High IIP3 mixer (+4dBm).
- 3V operation.
- 20-eTSSOP, or 24-QFN package with exposed paddle.

APPLICATIONS

- Cellular CDMA/AMPS Hand Held Phone

ORDERING INFORMATION

Device	Package	Operating Temperature
+ S1M8673X01-V0T0	20-eTSSOP-BD44	-30 to +80°C
+ S1M8673X01-G0T0	24-QFN-3.5×4.5	-30 to +80°C

+: New product

BLOCK DIAGRAM

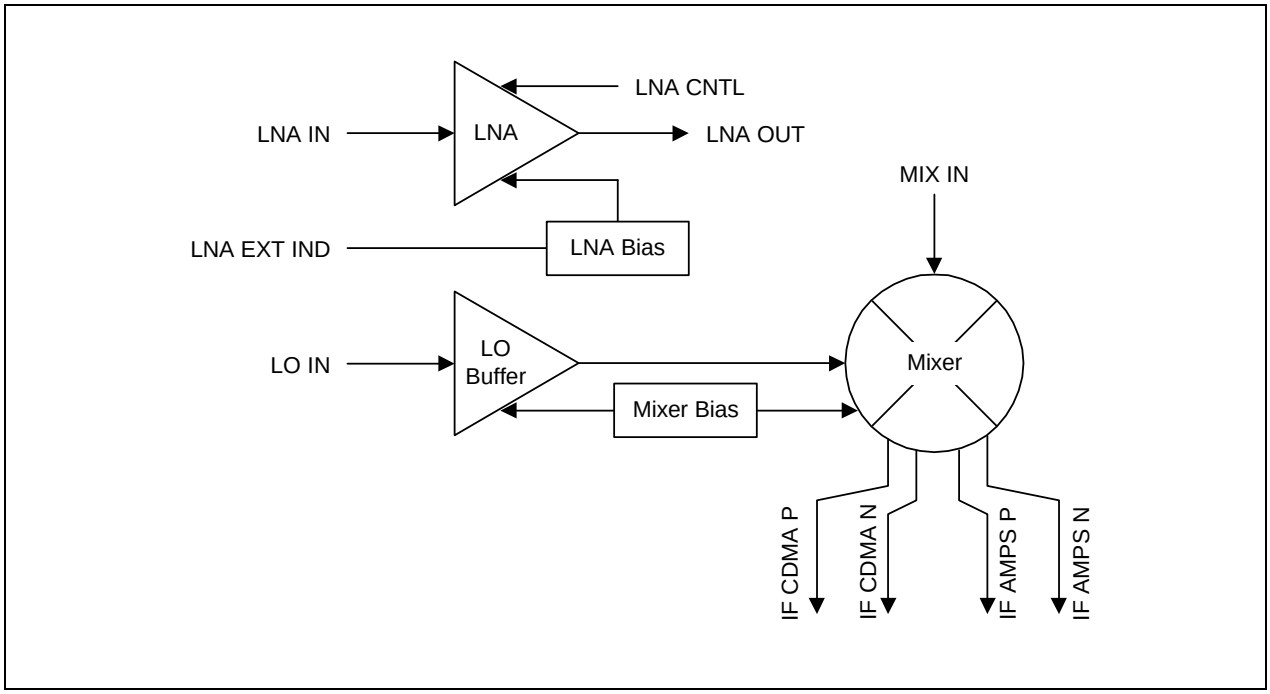


Figure 1. S1M8673 Block Diagram

PIN DESCRIPTION

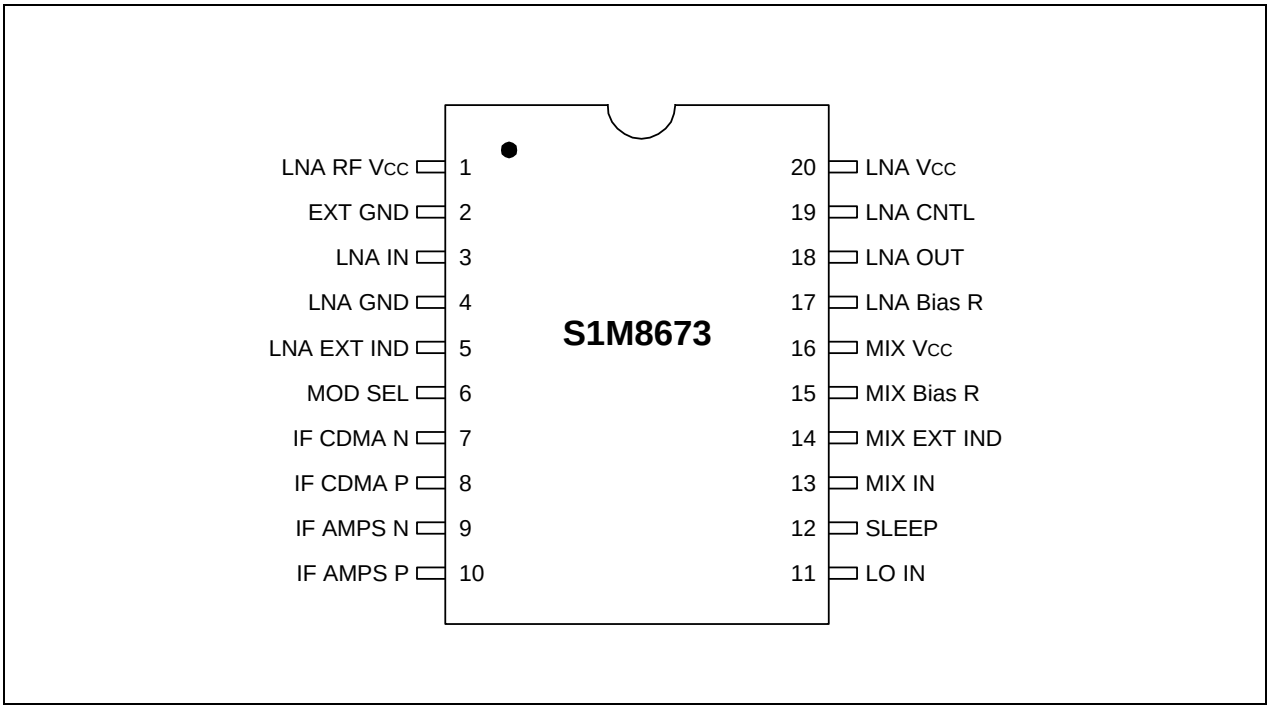


Figure 2. S1M8673 Pin Description (20-eTSSOP)

PIN DESCRIPTION

Pin No.	Pin Name	Type	Descriptions
1	LNA_RF_VCC		Power supply voltage for LNA amplifier core
2	EXT_GND		Ground
3	LNA_IN	Input	RF signal input of LNA
4	LNA_GND		Ground
5	LNA_EXT_IND		LNA Bias pin
6	MOD_SEL	Input	AMPS/CDMA mode selection
7	IF_CDMA_N	Output	Mixer IF Output (CDMA)
8	IF_CDMA_P	Output	Mixer IF Output (CDMA)
9	IF_AMPS_N	Output	Mixer IF Output (AMPS)
10	IF_AMPS_P	Output	Mixer IF Output (AMPS)
11	LO_IN	Input	Local oscillator power input
12	SLEEP		Power down
13	MIX_IN	Input	Mixer RF signal input
14	MIX_EXT_IND		Attach external Inductor
15	MIX_Bias_R		Current control resistor for mixer
16	MIX_VCC		Power supply voltage for MIXER
17	LNA_Bias_R		LNA current control resistor
18	LNA_OUT	Output	LNA Output
19	LNA_CNTL		LNA Gain Control
20	LNA_VCC		Power supply voltage for LNA bias circuit

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{CC}	-0.3 to 5.0	V
Input voltage range	V_I	-0.3 to 5.0	V
LNA input power	$P_{I(LNA)}$	+ 5.0	dBm
Power dissipation	P_D	600	mW
Operating temperature	T_{OPR}	-30 to +80	°C
Storage temperature	T_{STG}	-65 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{CC}	2.5 to 3.3	V
Operating temperature	Ta	-30 to +80	°C
Logic 0		$0.2 \times V_{CC}$	V
Logic 1		V_{CC}	V

ELECTRICAL CHARACTERISTICS

(T_a = 25 °C, V_{CC} = 3.0V, PLO = -10dBm, input/output externally matched)

Characteristic	Test Conditions	Min	Typ	Max	Unit
LNA					
Frequency Range			869 - 894		MHz
Gain High gain state Low gain state	@ 885 MHz (Vcntl=3V) (Vcntl=0V)	 14 2	 16 4	 18 6	dB
Noise Figure High gain state Low gain state	@ 885 MHz (Vcntl=3V) (Vcntl=0V)		 1.8 8	 2.2 9	dB
Input Return Loss			- 15	- 10	dB
Output Return Loss			- 15	- 10	dB
Reverse Isolation			- 35	- 30	dB
P1dB High gain state Low gain state	@ Input (Vcntl=3V) (Vcntl=0V)	 - 8 - 8	 - 6 - 6		dBm
IP3 High gain state Low gain state	@ Input (Vcntl=3V) (Vcntl=0V)	 2 2	 4 4		dBm
Current Consumption			8		mA
Mixer					
RF Frequency Range			869 - 894		MHz
IF Frequency			50 - 200		MHz
Conversion Gain CDMA mode AMPS mode		 6.5 4.0	 7.5 5.0	 8.5 6.0	dB
Output Impedance CDMA AMPS	 (Differential) (Single-ended)		 2 1.5		KΩ
Noise Figure (SSB) CDMA mode AMPS mode			 8.0 9.2	 9.0 9.5	dB
LO Power		- 15	- 10	- 5	dB
RF Input Return Loss			- 15	- 10	dB
LO Input Return Loss			- 15	- 10	
IIP3 CDMA mode AMPS mode	@ Input	 2 2	 4 4		dBm
LO to RF Isolation			- 20	- 15	dB
Current Consumption			14		mA

TECHNICAL DESCRIPTION

LOW NOISE AMPLIFIER (LNA)

The LNA is designed to provide low noise figure and high linearity to achieve maximum dynamic range. Pin 17, LNA bias control pin, is required to connect grounded resistor to decide the LNA current. The input and output are logic 0, mathod externally. For handling high level signals, LNA provides the low gain state by setting Pin 19 to ground.

MIXER

The mixer is designed to operate with very low LO power of -10dBm. The LO port is matched externally to the chip. Bias control resistors have to be connected to the Pin 15 to adjust the mixer current.

The sleep mode is controlled by a signal at Pin 12. The supply voltage should be present at all the VCC pins for normal operation.

The signal pin assignments and functional pin descriptions are found in Table 1. The absolute maximum ratings of the S1M8673 are provided in Table 2, the recommended operating conditions are specified in Table 3, and electrical specifications are provided in Table 4.

ESD SENSITIVITY

The S1M8673 is a Class 1 device. The following extreme Electrostatic Discharge (ESD) precautions are required according to the TBD Human Body Model (HBM) or Charged Device Model (CDM)

- Complete ESD training program required.
- Protective outer garments.
- Handle device in ESD safeguard work area.
- Transport device in ESD shielded containers.
- Monitor and test all ESD protection **equipment**.

Treat the S1M8673 as extremely sensitive to ESD since ESD sensitivity has not yet been determined for this device.

PASSIVE ELEMENT VALUE OF TEST CIRCUIT

Element	Value	Element	Value
R1	16 kΩ	C64	39 pF
R2	11 kΩ	C65	1000 pF
R3	1 kΩ	C66	1.8 pF
R4	1 kΩ	C67	1000 pF
R5	560 Ω	C68	9 pF
R6	1.5 kΩ	C81	1000 pF
C2	1000 pF	C82	1000 pF
C4	1000 pF	L1	10 nH
C6	1000 pF	L2	47 nH
C8	1000 pF	L3	390 nH
C10	1000 pF	L4	390 nH
C14	1000 pF	L5	1.8 uH
C51	39 pF	L6	1.8 uH
C52	5.7 pF	L7	4.7 nH
C54	8 pF	L8	8.2 nH
C55	8 pF	L9	82 nH
C56	1000 pF	L10	18 nH
C57	1000 pF	L11	1.8 uH
C58	3.3 pF	L12	1.8 uH
C60	39 pF	L13	330 nH
C61	1.5 pF	T1	1:8 Transformer
C63	39 pF	T2	1:8 Transformer

NOTES:

1. Transformer: TC8-1 by Mini-Circuits (See the data book of Mini-Circuits for more detailed information)
2. High Q components are recommended for C51, C52, L1, and L2 to reduce the noise figure.
3. For cascade measurement, RF filter with input and output impedance of 50Ω can be inserted between SC2 and SC3.

BLOCK TEST CIRCUIT (20TSSOP)

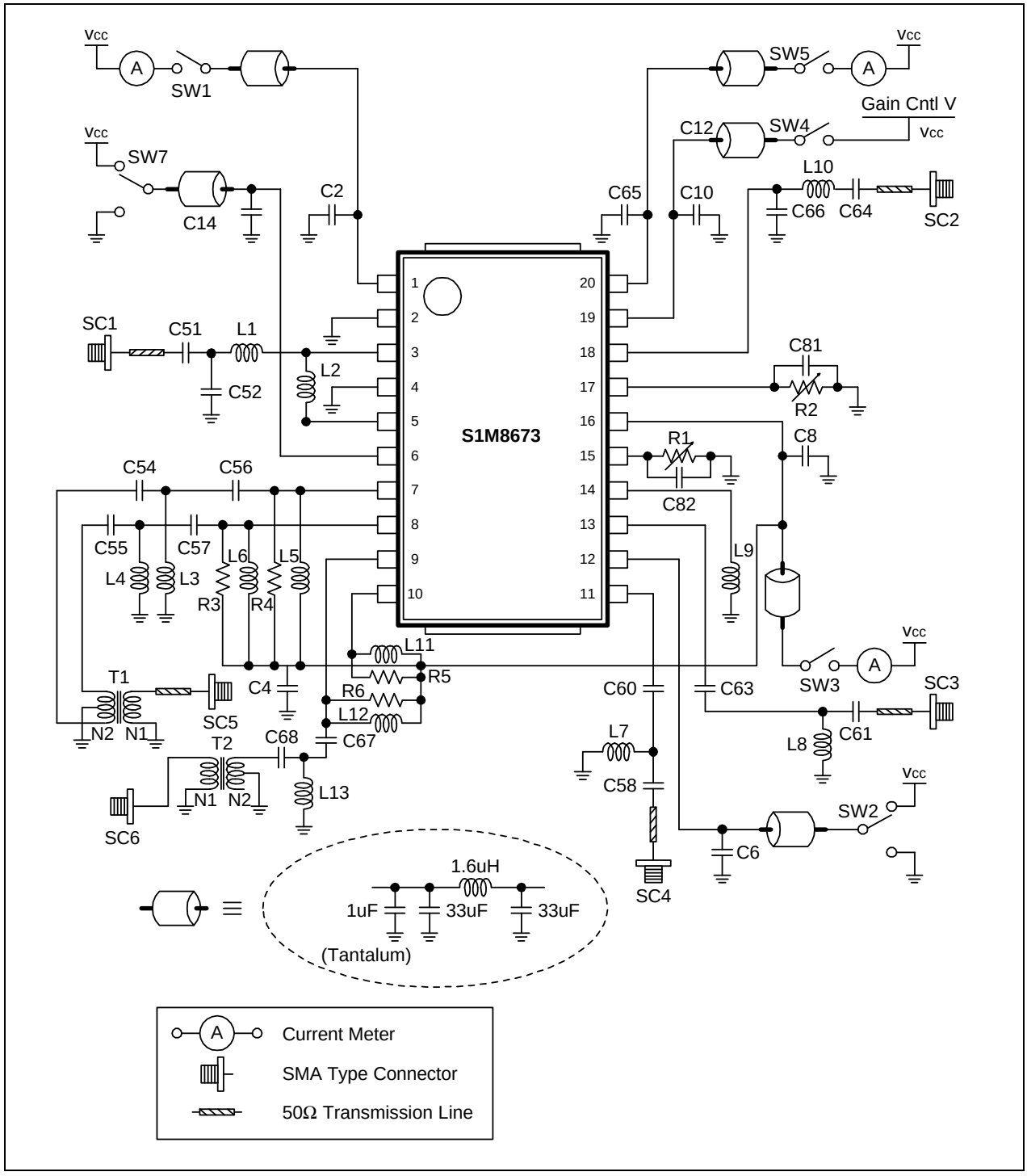


Figure 3. Package Block Test Circuit (B-Type)

NOTES