EPSON

PF1195-01

S1M1W043B0J7

4M-bit Static RAM

Preliminary

Super Low Voltage Operation Products

- ●Super Low Voltage Operation and Low Current Consumption
- ●Access Time 70ns (1.65V)
- ●262,144 Words x 16-bit Asynchronous
- ●Wide Temperature Range

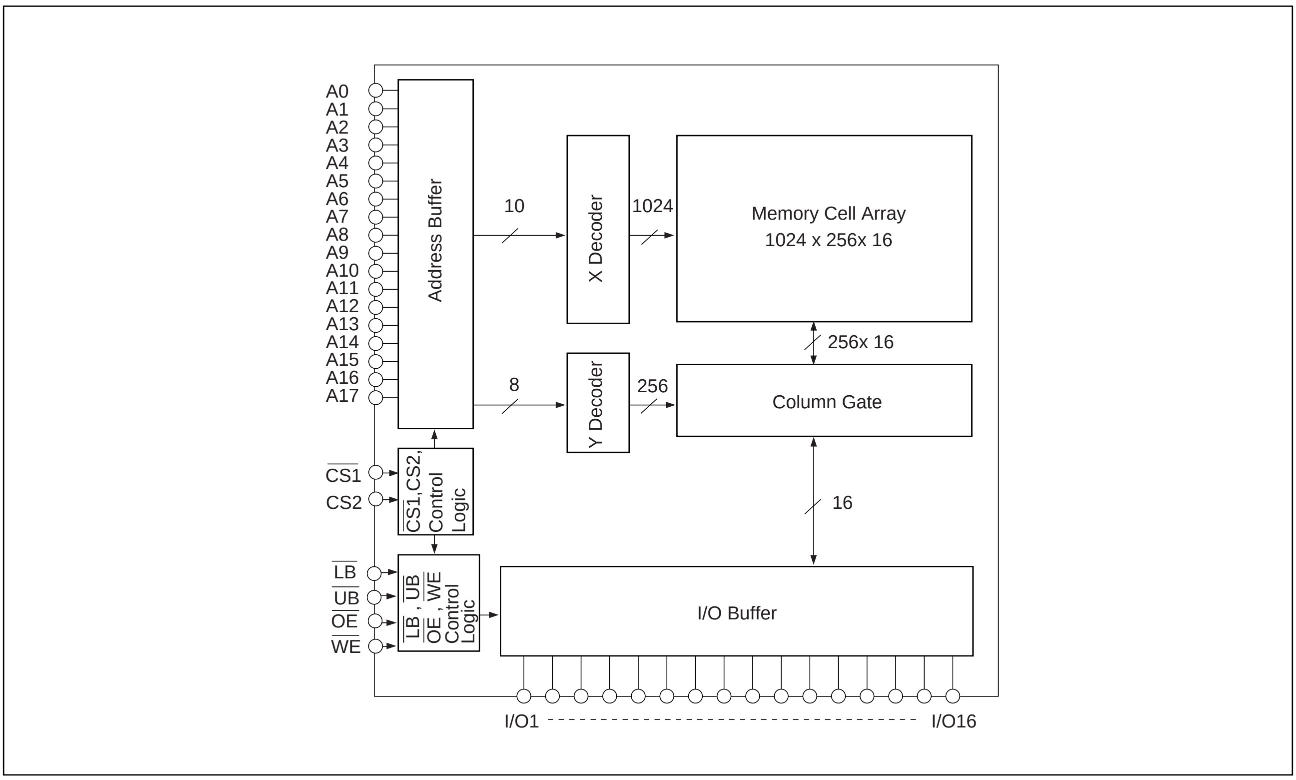
■ DESCRIPTION

The S1M1W043B0J7 is a 262,144 words x 16-bit asynchronous, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock and no refreshing circuit. It is possible to control the data width by the data byte control. 3-state output allows easy expansion of memory capacity. The temperature range of the S1M1W043B0J7 is from –40 to 85°C, and it is suitable for the industrial products.

■ FEATURES

- ● Fast Access time 70ns (1.65V)
- ● Low supply current .... LL Version
- ● Completely static .... No clock required
- ● Supply voltage .... 1.65V to 2.2V
- ● 3-state output with wired-OR capability
- ● Non-volatile storage with back-up batteries
- ● Package .... S1M1W043B0J PFBGA-48 pin (Plastic CSP)

■ BLOCK DIAGRAM



PIN CONFIGURATION

TFBGA-48 pin

S1M1V083B0J

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CS2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CS1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{DD}
E	V_{DD}	I/O13	NC	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	$\overline{WE}$	I/O8
H	NC	A8	A9	A10	A11	NC

Top view (Looking through part)

PIN DESCRIPTION

A0 to A17	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$	Chip Select1
CS2	Chip Select2
$\overline{LB}$	LOWER Byte Enable
$\overline{UB}$	UPPER Byte Enable
I/O1 to 16	Data I/O
V_{DD}	Power Supply (1.8V to 2.7V)
V_{SS}	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	– 0.3 to 2.7	V
Input voltage	V_I	– 0.3 * to V_{DD} + 0.3	V
Input/Output voltage	$V_{I/O}$	– 0.3 * to V_{DD} + 0.3	V
Power dissipation	P_D	0.5	W
Operating temperature	T_{opr}	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	–

* V_I,$V_{I/O}$ (Min.) = –2.0V (when pulse width is less than 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

(Ta = –40 to 85 °C)

Parameter	Symbol	V_{DD} = 1.65 to 2.2V			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{DD}	1.65	1.8/2.0	2.2	V
	V_{SS}	0.0	0.0	0.0	V
Input voltege	V_{IH}	0.75V_{DD}	–	V_{DD}+0.3	V
	V_{IL}	– 0.3*	–	0.3	V

* if pulse width is less than 50ns it is – 2.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{SS} =0V, Ta = –40 to 85 °C)

Parameter	Symbol	Conditions		V_{DD} = 1.65 to 2.2V			Unit
				Min.	Typ.*1	Max.	
Input leakage current	I_{LI}	V_I = 0 to V_{DD}		–1.0	–	1.0	µA
Output leakage current	I_{LO}	$\overline{LB}$ and $\overline{UB}$ = V_{IH} or $\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{DD}		–1.0	–	1.0	µA
High level output voltage	V_{OH}	I_{OH}	–0.5mA	1.4	–	–	V
			–100µA	V_{DD}–0.2	–	–	
Low level output voltage	V_{OL}	I_{OL}	0.5mA	–	–	0.4	V
			100µA	–	–	0.2	
Standby supply current	I_{DDS}	$\overline{CS1}$ = V_{IH} or CS2= V_{IL}		–	–	0.5	mA
	I_{DDS1}	$\overline{CS1}$ = CS2 ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V		–	–	10	µA
			Ta ≤ 25°C	–	0.5	1.0	
Average operating current	I_{DDA}	V_I = V_{IL} or V_{IH} $I_{I/O}$ = 0mA, tcyc = Min.		–	17.8	25	mA
	I_{DDA1}	V_I = V_{IL} or V_{IH} $I_{I/O}$ = 0mA, tcyc = 1µs		–	2.1	3.5	mA
Operating Supply Current	I_{DDO}	V_I = V_{IL} or V_{IH} $I_{I/O}$ = 0mA		–	2.1	3.5	mA

*1 : Typical values are measured at Ta = 25°C and V_{DD} = 1.8V

● Terminal Capacitance

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C_{ADD}	V_{ADD} = 0V	–	–	8	pF
Input Capacitance	C_I	V_I = 0V	–	–	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	–	10	pF

Note : This parameter is made by the inspection data of sample, not of all products

● AC Electrical Characteristics

❍ Read Cycle

(V_{SS} = 0V, Ta = –40 to 85°C)

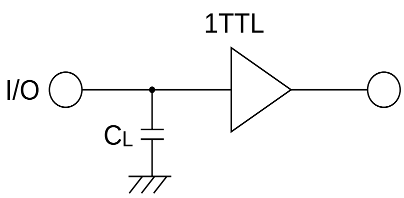
Parameter	Symbol	Test Conditions	S1M1W043B0J7 1.65 to 2.2V		Unit
			Min.	Max.	
Read cycle time	t_{RC}	1	70	–	ns
Address access time	t_{ACC}	1	–	70	ns
$\overline{CS1}$ access time	t_{ACS1}	1	–	70	ns
CS2 access time	t_{ACS2}	1	–	70	ns
$\overline{OE}$ access time	t_{OE}	1	–	40	ns
$\overline{LB}$, $\overline{UB}$ access time	t_{AB}	1	–	40	ns
$\overline{CS1}$ output set time	t_{CLZ1}	2	5	–	ns
CS2 output set time	t_{CLZ2}	2	5	–	ns
$\overline{CS1}$ output floating	t_{CHZ1}	2	–	30	ns
CS2 output floating	t_{CHZ2}	2	–	30	ns
$\overline{LB}$, $\overline{UB}$ output set time	t_{BLZ}	2	0	–	ns
$\overline{LB}$, $\overline{UB}$ output floating	t_{BHZ}	2	–	30	ns
$\overline{OE}$ output set time	t_{OLZ}	2	0	–	ns
$\overline{OE}$ output floating	t_{OHZ}	2	–	30	ns
Output hold time	t_{OH}	1	5	–	ns

❍ Write Cycle

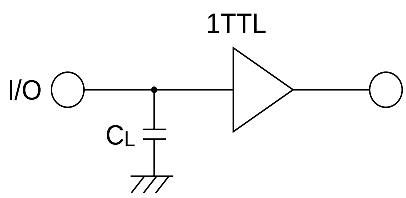
(V_{SS} = 0V, Ta = –40 to 85°C)

Parameter	Symbol	Test Conditions	S1M1W043B0J7 1.65 to 2.2V		Unit
			Min.	Max.	
Write cycle time	t_{WC}	1	70	–	ns
Chip select time ($\overline{CS1}$)	t_{CW1}	1	60	–	ns
Chip select time (CS2)	t_{CW2}	1	60	–	ns
Address enable time	t_{AW}	1	60	–	ns
Address setup time	t_{AS}	1	0	–	ns
Write pulse width	t_{WP}	1	55	–	ns
$\overline{LB}$, $\overline{UB}$ select time	t_{BW}	1	60	–	ns
Address hold time	t_{WR}	1	0	–	ns
Data setup time	t_{DW}	1	35	–	ns
Data hold time	t_{DH}	1	0	–	ns
$\overline{WE}$ output floating	t_{WHZ}	2	–	30	ns
$\overline{WE}$ output set time	t_{OW}	2	5	–	ns

*1 Test Conditions
1. Input pulse level : 0.3V to 0.8V_{DD}(1.65V to 2.2V)
2. $t_r = t_f$ = 5ns
3. Input and output timing reference levels :1/2V_{DD}(1.65V to 2.2V)
4. Output load : C_L =30pF (Includes Jig Capacitance)

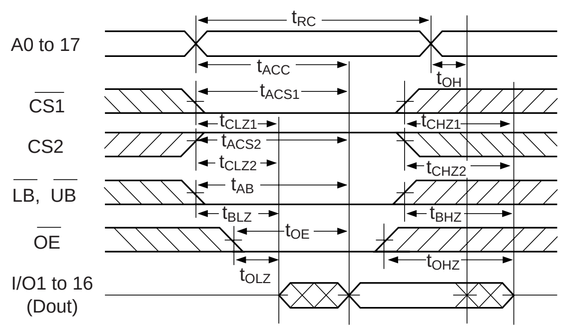


*2 Test Conditions
1. Input pulse level : 0.3V to 0.8V_{DD}(1.65V to 2.2V)
2. $t_r = t_f$ = 5ns
3. Input timing reference levels :1/2V_{DD}(1.65V to 2.2V)
4. Output timing reference levels : ±200mV (The level changed from stable output voltage level)
5. Output load :C_L = 5pF (Includes Jig Capacitance)

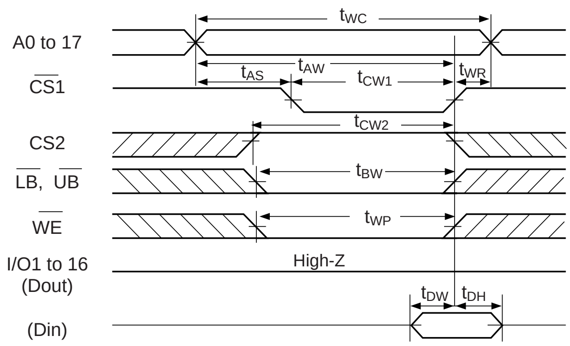


● Timing Chart

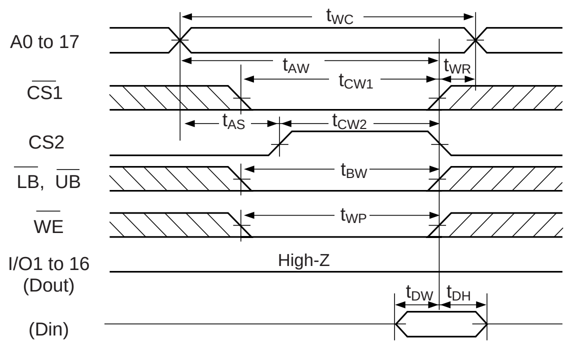
Read Cycle*1



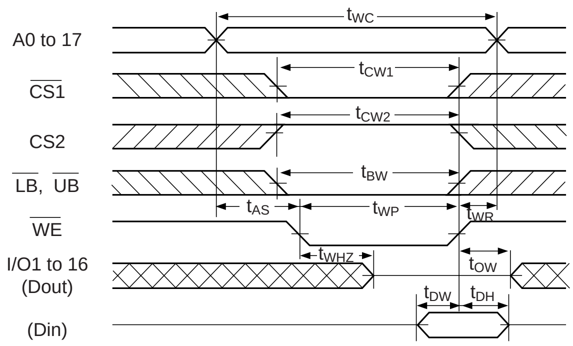
Write Cycle 1 (CS1 Control) *2, *3



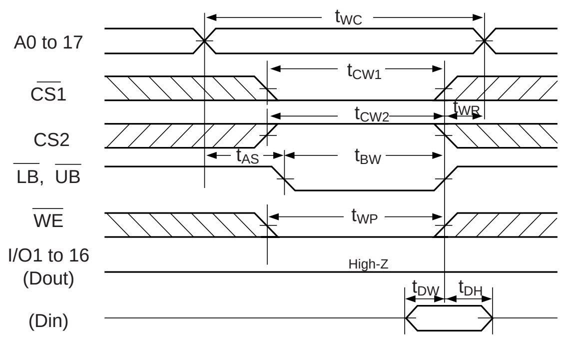
Write Cycle 2 (CS2 Control) *2, *3



Write Cycle 3 (WE Control)*3



Write Cycle 4 (UB, LB Control) *3



Note : *1 During read cycle time, WE is to be "High" level.
*2 In write cycle time that is controlled by CS1 or CS2, output buffer is to be "Hi-Z" state even if OE is "Low" level.
*3 When output buffer is in output state, be careful that do not input the opposite signals to the output data.

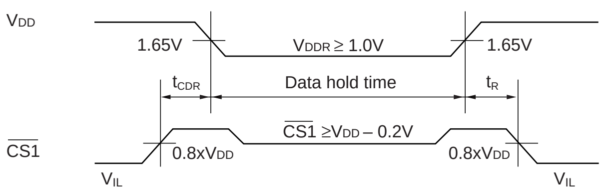
● DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(VSS = 0V, Ta = –40 to 85°C)

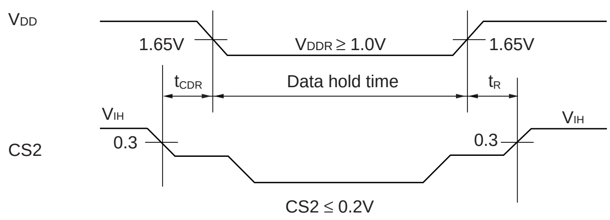
Parameter	Symbol	Conditions	Min.	Typ.*	Max.	Unit
Data retention supply voltage	V_{DDR}		1.0	–	2.2	V
Data retention curren	I_{DDR}	V_{DDR} = 1.2V CS1 = CS2≥ V_{DD} – 0.2V or CS2 ≤0.2V	–	0.25	5	µA
Data hold time	t_{CDR}		0	–	–	ns
Operation recovery time	t_R		100	–	–	ns

* : Reference data at Ta=25°C

Data retention timing ($\overline{\text{CS1}}$ Control)



Data retention timing (CS2 Control)



■ FUNCTIONS

● Truth Table

$\overline{\text{CS1}}$	CS2	$\overline{\text{LB}}$	$\overline{\text{UB}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O1 to 8	I/O9 to 16	MODE	I_{DD}
H	X	X	X	X	X	High-Z	High-Z	Not Selected	I_{DDS}, I_{DDS1}
X	L	X	X	X	X	High-Z	High-Z	Not Selected	I_{DDS}, I_{DDS1}
L	H	X	X	H	H	High-Z	High-Z	Output disable	I_{DDA}, I_{DDA1}
L	H	H	H	X	X	High-Z	High-Z	Output disable	I_{DDA}, I_{DDA1}
L	H	L	H	X	L	Data In	High-Z	Lower Byte Write	I_{DDA}, I_{DDA1}
L	H	H	L	X	L	High-Z	Data In	Upper Byte Write	I_{DDA}, I_{DDA1}
L	H	L	L	X	L	Data In	Data In	All Byte Write	I_{DDA}, I_{DDA1}
L	H	L	H	L	H	DataOut	High-Z	Lower Byte Read	I_{DDA}, I_{DDA1}
L	H	H	L	L	H	High-Z	DataOut	Upper Byte Read	I_{DDA}, I_{DDA1}
L	H	L	L	L	H	Data Out	Data Out	All Byte Read	I_{DDA}, I_{DDA1}

X : High or Low

● Reading data

It is possible to control the data width by $\overline{\text{LB}}$ and $\overline{\text{UB}}$ pins.

(1) Reading data from lower byte

Data is able to be read when the address is set while holding $\overline{\text{CS1}}$ ="Low",CS2 = "High", $\overline{\text{OE}}$ = "Low", $\overline{\text{LB}}$ ="Low", and $\overline{\text{WE}}$ = "High".

(2) Reading data from upper byte

Data is able to be read when the address is set while holding $\overline{\text{CS1}}$ = "Low",CS2 = "High", $\overline{\text{OE}}$ = "Low", $\overline{\text{UB}}$ = "Low", and $\overline{\text{WE}}$ ="High".

(3) Reading data from both bytes

Data is able to be read when the address is set while holding $\overline{\text{CS1}}$ = "Low",CS2= "High", $\overline{\text{OE}}$ ="Low", $\overline{\text{UB}}$ ="Low", $\overline{\text{LB}}$ = "Low", and $\overline{\text{WE}}$ = "High".

Since I/O pins are in "Hi-Z" state when, $\overline{\text{OE}}$ = "High", the data bus line can be used for any other objective, then access time is apparently able to be cut down.

● Writing data

(1) Writing data into lower byte

There are the following four ways of writing data into memory.

i) Hold CS2 = "High", $\overline{\text{WE}}$ = "Low", $\overline{\text{UB}}$ ="High", and $\overline{\text{LB}}$ = "Low",set address and give "Low" pulse to $\overline{\text{CS1}}$.

ii) Hold $\overline{\text{CS1}}$ = "Low", $\overline{\text{WE}}$ = "Low", $\overline{\text{UB}}$ ="High", and $\overline{\text{LB}}$ = "Low",set address and give "High" pulse to CS2.

iii) Hold $\overline{\text{CS1}}$ = "Low", CS2 = "High", $\overline{\text{UB}}$ ="High", and $\overline{\text{LB}}$ = "Low",set address and give "Low" pulse to $\overline{\text{WE}}$

ix) Hold $\overline{\text{CS1}}$ = "Low", CS2 = "High", $\overline{\text{WE}}$ ="Low",and $\overline{\text{UB}}$ = "High",set address and give "Low" pulse to $\overline{\text{LB}}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{\text{CS1}}$ ="Low",CS2 = "High", $\overline{\text{WE}}$ and $\overline{\text{LB}}$ ="Low".

(2) Writing data into upper byte

There are the following four ways of writing data into the memory.

i) Hold CS2 ="High",WE ="Low", $\overline{LB}$ ="High",and $\overline{UB}$ ="Low",set address and give "Low" pulse to $\overline{CS1}$.

ii) Hold $\overline{CS1}$ ="Low",WE ="Low", $\overline{LB}$ ="High",and $\overline{UB}$ ="Low",set address and give "High" pulse to CS2.

iii) Hold $\overline{CS1}$ ="Low",CS2 ="High", $\overline{LB}$ ="High",and $\overline{UB}$ ="Low",set address and give "Low" pulse to $\overline{WE}$.

ix) Hold $\overline{CS1}$ ="Low",CS2 ="High",WE="Low",and $\overline{LB}$ ="High",set address and give "Low" pulse to $\overline{UB}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS1}$ ="Low",CS2 = "High", $\overline{WE}$ and $\overline{UB}$ ="Low".

(3)Writing data into both bytes

There are the following four ways of writing data into the memory.

i) Hold CS2 = "High", $\overline{WE}$ = "Low", $\overline{LB}$ and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{CS1}$.

ii) Hold $\overline{CS1}$ = "Low", $\overline{WE}$ = "Low", $\overline{LB}$ and $\overline{UB}$ = "Low", set address and give "High" pulse to CS2.

iii) Hold $\overline{CS1}$ = "Low", CS2 = "High", $\overline{LB}$ and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{WE}$.

ix) Hold $\overline{CS1}$ = "Low", CS2 = "High", $\overline{WE}$ = "Low", set address and give "Low" pulse to LB and $\overline{UB}$.

Anyway, data on I/Opins are latched up into the memory cell during $\overline{CS1}$ = "Low" , CS2 ="High" , $\overline{WE}$ = "Low", $\overline{UB}$ and $\overline{LB}$ = "Low".

As DATA I/O pins are in "Hi-Z" when $\overline{CS1}$= "High", CS2 = "Low", $\overline{OE}$ = "High", or $\overline{LB}$ and $\overline{UB}$ ="High", the contention on the data bus can be avoided. But while I/O pins are in the output state, the data that is opposite to the output data should not be given.

● Standby mode

When $\overline{CS1}$ is "High" or CS2 is "Low" the chip is in the standby mode (only retaining data operation). In this case data I/O pins are Hi-Z, and all inputs of addresses, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$, and data are inhibited. When $\overline{CS1}$ = CS2 $\geq V_{DD}$ - 0.2V or CS2 $\leq$ 0.2V, there is almost no current flow except through the high resistance parts of the memory.

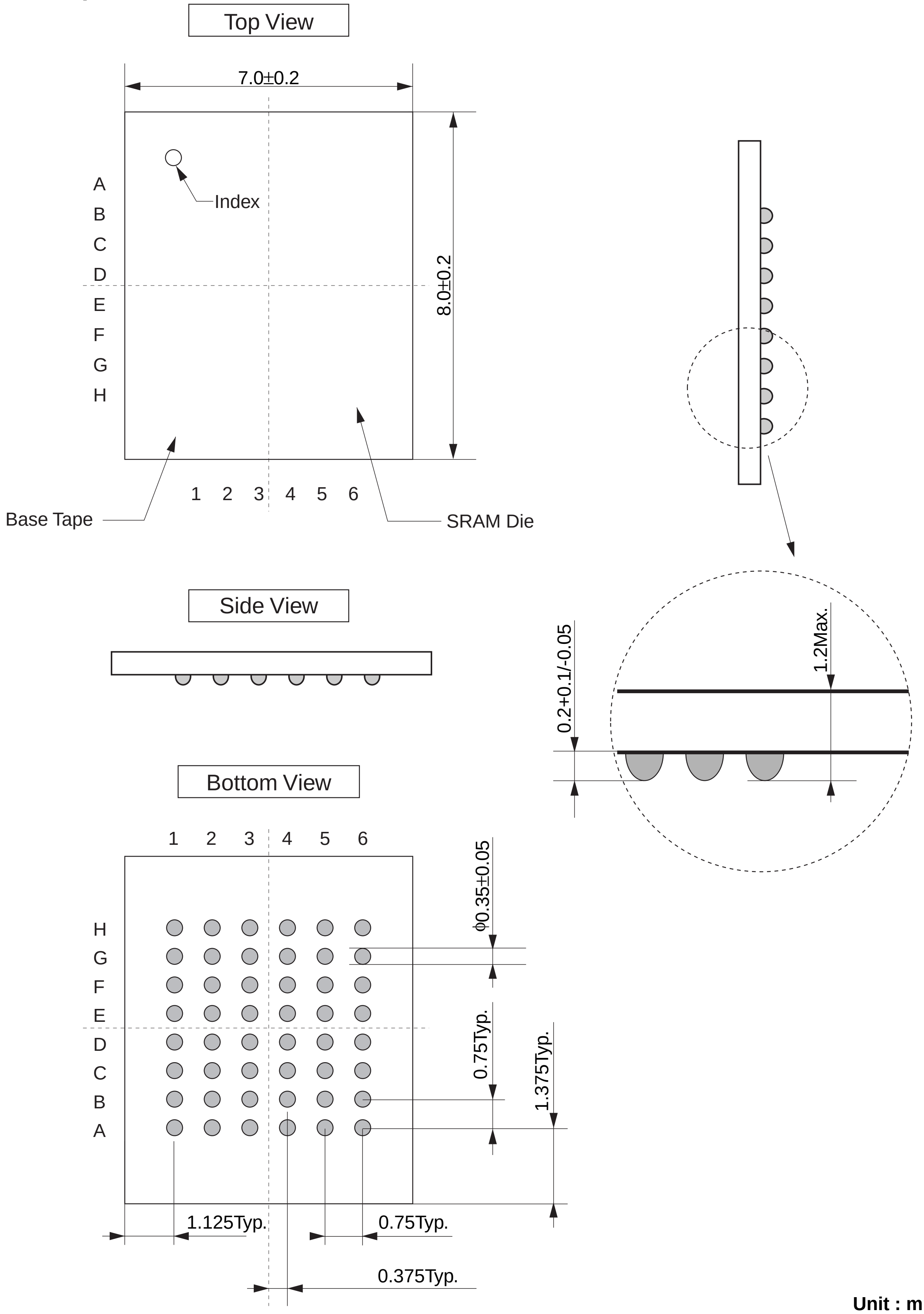
● Data retention at low voltage

In case of the data retention in the stadby mode, the power supply can be gone down till the specified voltage.

But it is impossible to write or read in this mode.

■ PACKAGE DIMENSIONS

PFBGA-48 pin



Unit : mm

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