

# S1M1V045B0J7

## 4M-bit Static RAM

Preliminary

Super Low Voltage  
Operation  
Products

- Super Low Voltage Operation and Low Current Consumption
- Access Time 70ns (2.4V)
- 262,144 Words x 16-bit / 524,288 Words x 8-bit Asynchronous
- Wide Temperature Range

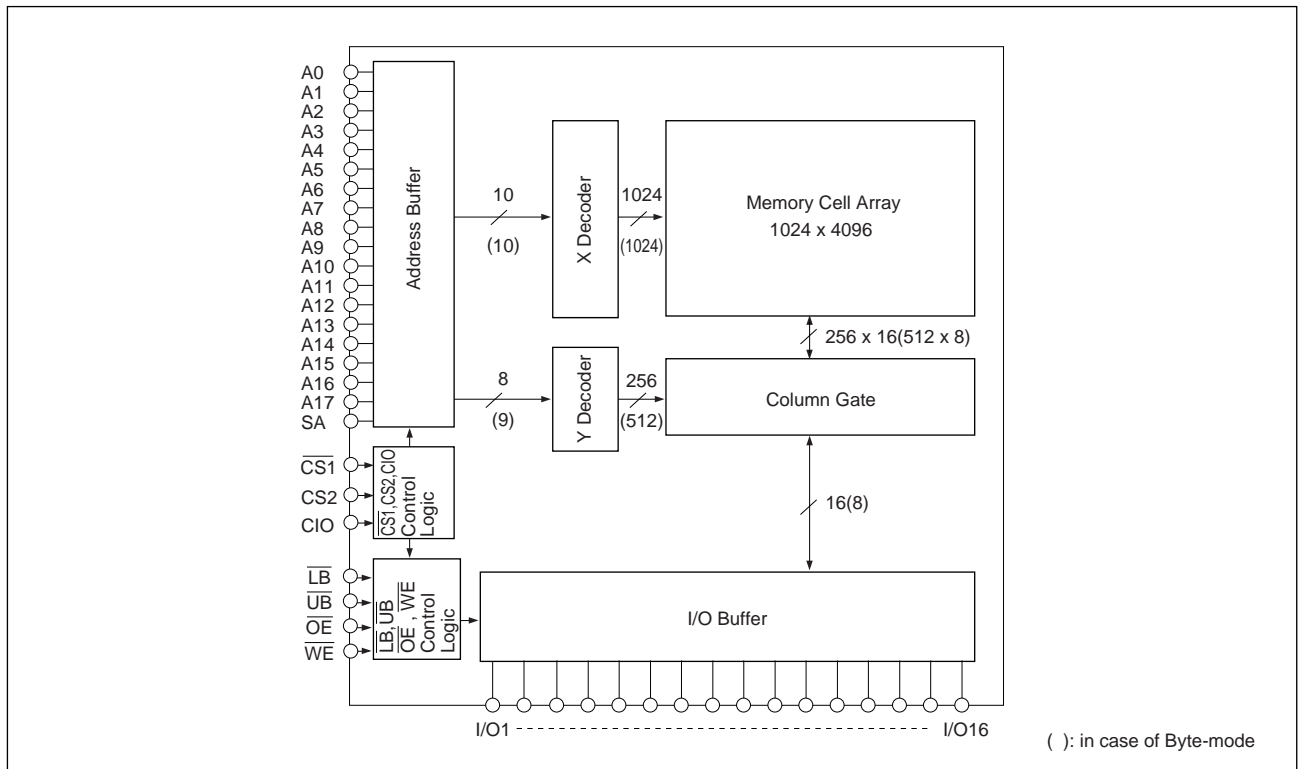
### DESCRIPTION

The S1M1V045B0J7 is a 262,144 words x 16-bit (Word-mode) / 524,288 words x 8-bit (Byte-mode) asynchronous, random access memory on a monolithic CMOS chip. It is possible to select Word-mode or Byte-mode by CIO-pin: CIO=VDD for Word-mode and CIO=Vss for Byte-mode. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock and no refreshing circuit. It is possible to control the data width by the data byte control for Word-mode. 3-state output allows easy expansion of memory capacity. The temperature range of the S1M1V045B0J7 is from -40 to 85°C, and it is suitable for the industrial products.

### FEATURES

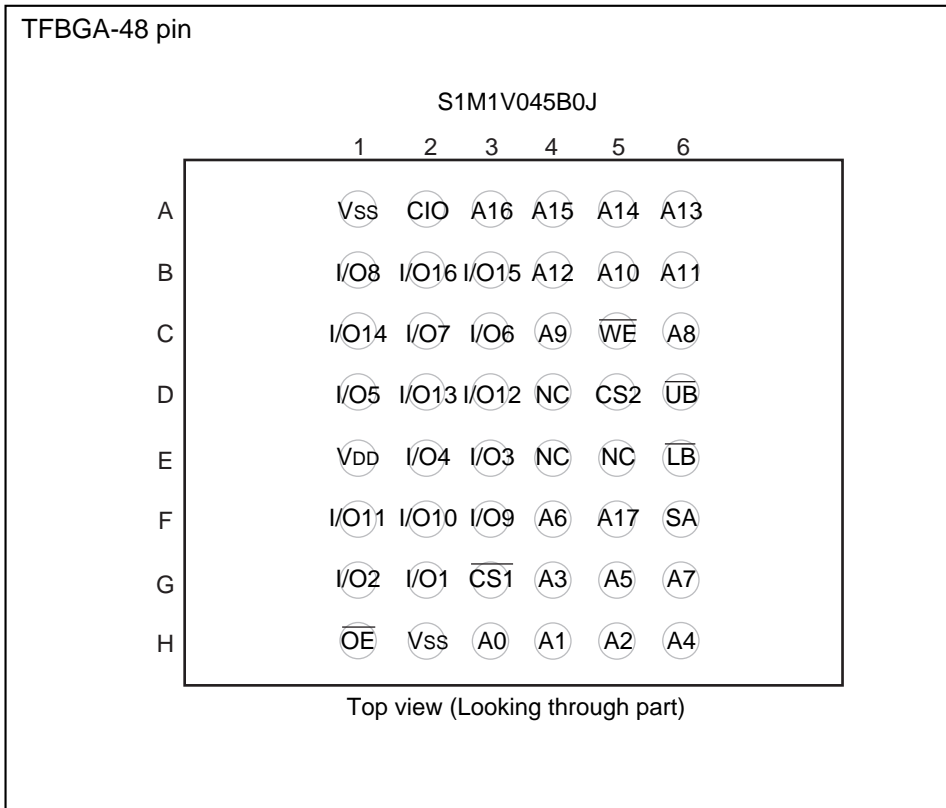
- Fast Access time ..... 70ns (2.4V)
- Low supply current ..... LL Version
- Completely static ..... No clock required
- Supply voltage ..... 2.4V to 3.0V
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ..... S1M1V045B0J                      TFBGA-48 pin (Tape CSP)

### BLOCK DIAGRAM



# S1M1V045B0J7

## ■ PIN CONFIGURATION



## ■ PIN DESCRIPTION

A0 to A17	Address Input
SA	Address Input (Byte-mode use)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$	Chip Select1
$\overline{CS2}$	Chip Select2
$\overline{LB}$	LOWER Byte Enable (Word-mode use)
$\overline{UB}$	UPPER Byte Enable (Word-mode use)
I/O1 to 16	Data I/O
CIO	Word-mode/Byte-mode Selection
V <sub>DD</sub>	Power Supply (2.4V to 3.0V)
V <sub>SS</sub>	Power Supply (0V)
NC	No connection

## ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub>=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	- 0.5 to 3.6	V
Input voltage	V <sub>I</sub>	- 0.5 * to V <sub>DD</sub> + 0.3	V
Input/Output voltage	V <sub>I/O</sub>	- 0.5 * to V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	0.5	W
Operating temperature	T <sub>opr</sub>	- 40 to 85	°C
Storage temperature	T <sub>stg</sub>	- 65 to 150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C, 10s (at lead)	-

\* V<sub>I</sub>, V<sub>I/O</sub> (Min.) = -2.0V (when pulse width is less than 50ns)

## ■ DC RECOMMENDED OPERATING CONDITIONS

(Ta = -40 to 85 °C)

Parameter	Symbol	V <sub>DD</sub> = 2.4 to 3.0V			Unit
		Min.	Typ.	Max.	
Supply voltage	V <sub>DD</sub>	2.4	2.7	3.0	V
	V <sub>SS</sub>	0.0	0.0	0.0	V
Input voltage	V <sub>IH</sub>	0.75V <sub>DD</sub>	-	V <sub>DD</sub> +0.3	V
	V <sub>IL</sub>	- 0.3*	-	0.3	V

\* if pulse width is less than 50ns it is - 2.0V

## ■ ELECTRICAL CHARACTERISTICS

### ● DC Electrical Characteristics

(V<sub>SS</sub>=0V, Ta = -40 to 85 °C)

Parameter	Symbol	Conditions	V <sub>DD</sub> = 2.4 to 3.0V			Unit	
			Min.	Typ. *1	Max.		
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = 0 to V <sub>DD</sub>	-1.0	-	1.0	μA	
Output leakage current	I <sub>LO</sub>	$\overline{\text{LB}}$ and $\overline{\text{UB}} = V_{IH}$ or $\overline{\text{CS1}} = V_{IH}$ or $\overline{\text{CS2}} = V_{IL}$ or $\overline{\text{WE}} = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ , V <sub>I/O</sub> = 0 to V <sub>DD</sub>	-1.0	-	1.0	μA	
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub>	-0.5mA	1.8	-	-	V
			-100μA	V <sub>DD</sub> -0.2	-	-	
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub>	0.5mA	-	-	0.4	V
			100μA	-	-	0.2	
Standby supply current	I <sub>D<sub>DS</sub></sub>	$\overline{\text{CS1}} = V_{IH}$ or $\overline{\text{CS2}} = V_{IL}$	-	-	1.0	mA	
	I <sub>D<sub>DS1</sub></sub>	$\overline{\text{CS1}} = \overline{\text{CS2}} \geq V_{DD} - 0.2V$ or $\overline{\text{CS2}} \leq 0.2V$	-	0.4	12	μA	
Average operating current	I <sub>D<sub>DA</sub></sub>	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>I/O</sub> = 0mA, t <sub>cyc</sub> = Min.	-	25	35	mA	
	I <sub>D<sub>DA1</sub></sub>	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>I/O</sub> = 0mA, t <sub>cyc</sub> = 1μs	-	3.0	5.0	mA	
Operating Supply Current	I <sub>D<sub>DO</sub></sub>	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>I/O</sub> = 0mA	-	3.0	5.0	mA	

\*1 : Typical values are measured at Ta = 25°C and V<sub>DD</sub> = 2.85V

### ● Terminal Capacitance

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C <sub>ADD</sub>	V <sub>ADD</sub> = 0V	-	-	8	pF
Input Capacitance	C <sub>I</sub>	V <sub>I</sub> = 0V	-	-	8	pF
I/O Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	-	-	10	pF

Note : This parameter is made by the inspection data of sample, not of all products

# S1M1V045B0J7

## ● AC Electrical Characteristics

### ○ Read Cycle

(V<sub>SS</sub> = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Test Conditions	S1M1V045B0J7		Unit
			2.4 to 3.0V		
			Min.	Max.	
Read cycle time	t <sub>RC</sub>	1	70	–	ns
Address access time	t <sub>ACC</sub>	1	–	70	ns
CS1 access time	t <sub>ACS1</sub>	1	–	70	ns
CS2 access time	t <sub>ACS2</sub>	1	–	70	ns
$\overline{OE}$ access time	t <sub>OE</sub>	1	–	40	ns
$\overline{LB}$ , $\overline{UB}$ access time*	t <sub>AB</sub>	1	–	40	ns
$\overline{CS1}$ output set time	t <sub>CLZ1</sub>	2	5	–	ns
CS2 output set time	t <sub>CLZ2</sub>	2	5	–	ns
$\overline{CS1}$ output floating	t <sub>CHZ1</sub>	2	–	30	ns
CS2 output floating	t <sub>CHZ2</sub>	2	–	30	ns
$\overline{LB}$ , $\overline{UB}$ output set time*	t <sub>BLZ</sub>	2	0	–	ns
$\overline{LB}$ , $\overline{UB}$ output floating*	t <sub>BHZ</sub>	2	–	30	ns
$\overline{OE}$ output set time	t <sub>OLZ</sub>	2	0	–	ns
$\overline{OE}$ output floating	t <sub>OHZ</sub>	2	–	30	ns
Output hold time	t <sub>OH</sub>	1	5	–	ns

\*Word-mode only

### ○ Write Cycle

(V<sub>SS</sub> = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Test Conditions	S1M1V045B0J7		Unit
			2.4 to 3.0V		
			Min.	Max.	
Write cycle time	t <sub>WC</sub>	1	70	–	ns
Chip select time ( $\overline{CS1}$ )	t <sub>CW1</sub>	1	60	–	ns
Chip select time (CS2)	t <sub>CW2</sub>	1	60	–	ns
Address enable time	t <sub>AW</sub>	1	60	–	ns
Address setup time	t <sub>AS</sub>	1	0	–	ns
Write pulse width	t <sub>WP</sub>	1	55	–	ns
$\overline{LB}$ , $\overline{UB}$ select time *	t <sub>BW</sub>	1	60	–	ns
Address hold time	t <sub>WR</sub>	1	0	–	ns
Data setup time	t <sub>DW</sub>	1	35	–	ns
Data hold time	t <sub>DH</sub>	1	0	–	ns
$\overline{WE}$ output floating	t <sub>WHZ</sub>	2	–	30	ns
$\overline{WE}$ output set time	t <sub>OW</sub>	2	5	–	ns

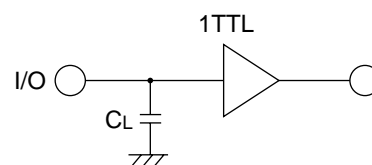
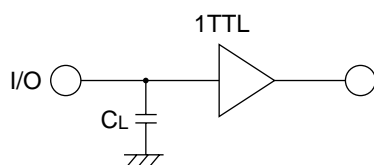
\*Word-mode only

#### \*1 Test Conditions

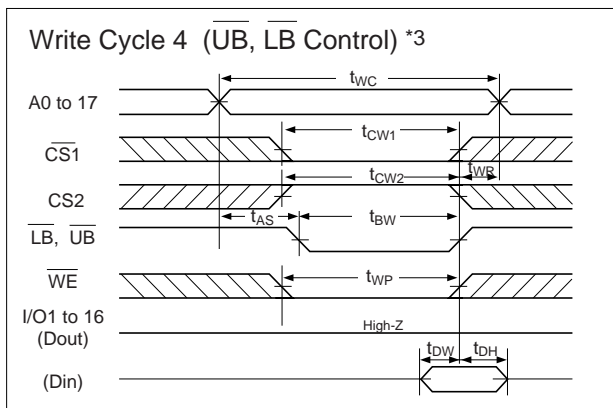
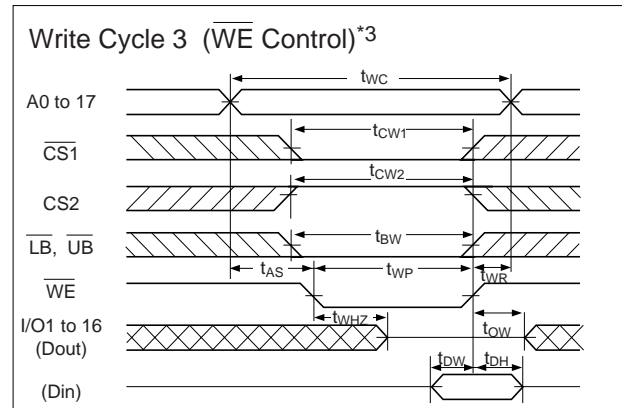
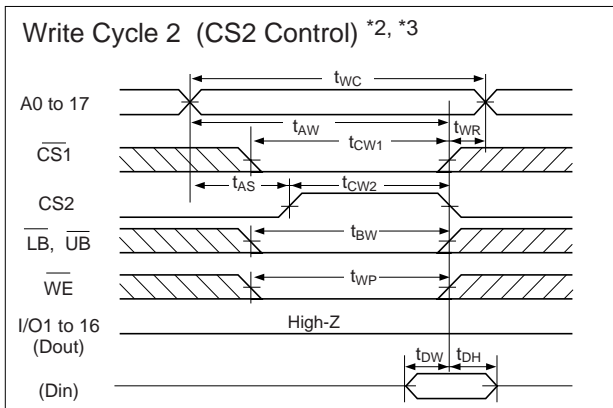
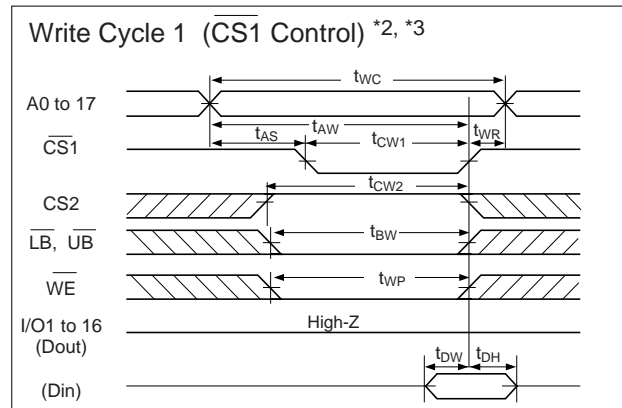
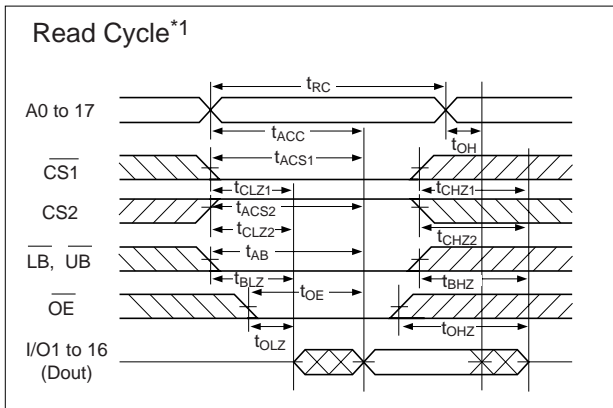
1. Input pulse level : 0.3V to 0.8V<sub>DD</sub> (2.4V to 3.0V)
2. t<sub>r</sub> = t<sub>f</sub> = 5ns
3. Input and output timing reference levels : 1/2V<sub>DD</sub> (2.4V to 3.0V)
4. Output load : C<sub>L</sub> = 100pF (Includes Jig Capacitance)

#### \*2 Test Conditions

1. Input pulse level : 0.3V to 0.8V<sub>DD</sub> (2.4V to 3.0V)
2. t<sub>r</sub> = t<sub>f</sub> = 5ns
3. Input timing reference levels : 1/2V<sub>DD</sub> (2.4V to 3.0V)
4. Output timing reference levels : ±200mV (The level changed from stable output voltage level)
5. Output load : C<sub>L</sub> = 5pF (Includes Jig Capacitance)



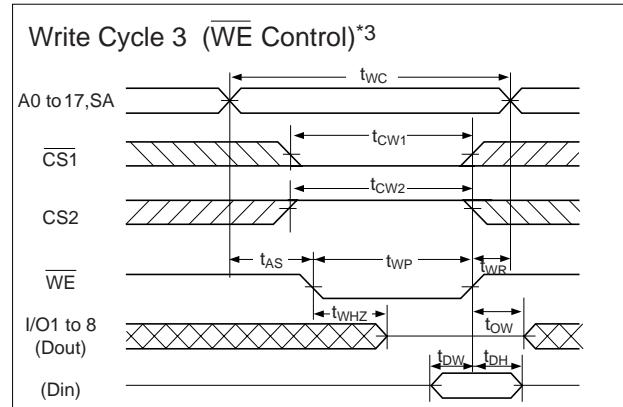
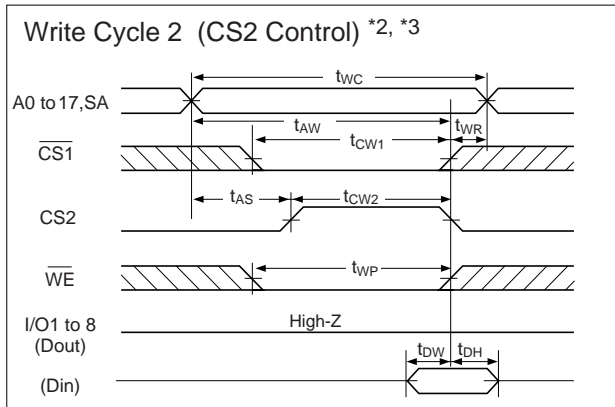
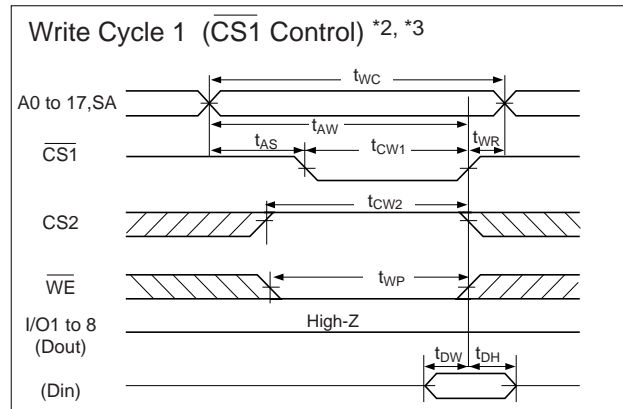
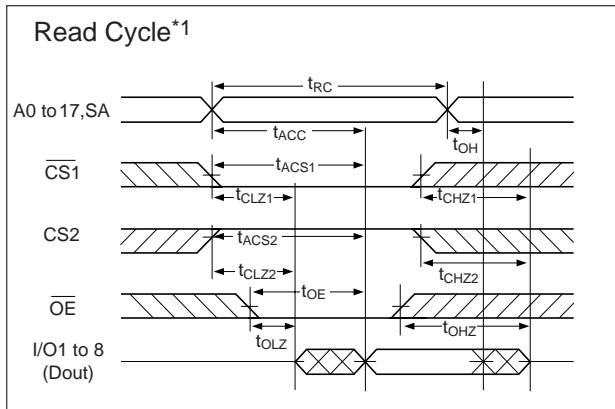
## ● Timing Chart (Word-mode)



- Note : \*1 During read cycle time,  $\overline{WE}$  is to be "High" level.  
 \*2 In write cycle time that is controlled by CS1 or CS2, output buffer is to be "Hi-Z" state even if  $\overline{OE}$  is "Low" level.  
 \*3 When output buffer is in output state, be careful that do not input the opposite signals to the output data.

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## ● Timing Chart (Byte-mode)



- Note : \*1 During read cycle time,  $\overline{WE}$  is to be "High" level.  
 \*2 In write cycle time that is controlled by  $\overline{CS1}$  or CS2, output buffer is to be "Hi-Z" state even if  $\overline{OE}$  is "Low" level.  
 \*3 When output buffer is in output state, be careful that do not input the opposite signals to the output data.

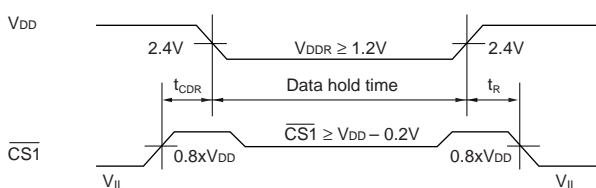
## ● DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

( $V_{SS} = 0V$ ,  $T_a = -40$  to  $85^\circ C$ )

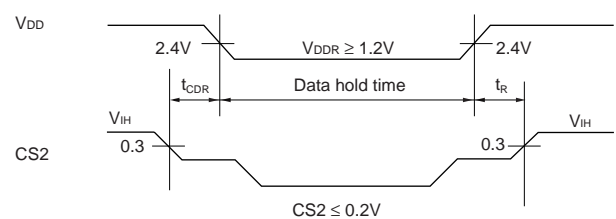
Parameter	Symbol	Conditions	Min.	Typ.*	Max.	Unit
Data retention supply voltage	$V_{DDR}$		1.2	—	3.0	V
Data retention curren	$I_{DDR}$	$V_{DDR} = 2.5V$ $\overline{CS1} = CS2 \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$	—	0.3	9	$\mu A$
Data hold time	$t_{CDR}$		0	—	—	ns
Operation recovery time	$t_R$		100	—	—	ns

\* : Reference data at  $T_a = 25^\circ C$

### Data retention timing ( $\overline{CS1}$ Control)



### Data retention timing (CS2 Control)



## FUNCTIONS

### ● Truth Table

#### <Word-mode>

CIO	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	I/O1 to 8	I/O9 to 16	MODE	I <sub>DD</sub>
H	H	X	X	X	X	X	X	High-Z	High-Z	Not Selected	I <sub>DD</sub> , I <sub>DD</sub> S1
H	X	L	X	X	X	X	X	High-Z	High-Z	Not Selected	I <sub>DD</sub> , I <sub>DD</sub> S1
H	L	H	X	X	X	H	H	High-Z	High-Z	Output disable	I <sub>DD</sub> A, I <sub>DD</sub> A1
H	L	H	H	H	X	X	X	High-Z	High-Z	Output disable	I <sub>DD</sub> A, I <sub>DD</sub> A1
H	L	H	L	H	X	L	L	Data Out	Data Out	Word Read	I <sub>DD</sub> A, I <sub>DD</sub> A1
H	L	H	L	H	X	L	H	Data Out	High-Z	Lower Byte Read	I <sub>DD</sub> A, I <sub>DD</sub> A1
H	L	H	L	H	X	H	L	High-Z	Data Out	Upper Byte Read	I <sub>DD</sub> A, I <sub>DD</sub> A1
H	L	H	X	L	X	L	L	Data In	Data In	Word Write	I <sub>DD</sub> A, I <sub>DD</sub> A1
H	L	H	X	L	X	L	H	Data In	High-Z	Lower Byte Write	I <sub>DD</sub> A, I <sub>DD</sub> A1
H	L	H	X	L	X	H	L	High-Z	Data In	Upper Byte Write	I <sub>DD</sub> A, I <sub>DD</sub> A1

X : High or Low

#### <Byte-mode>

CIO	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	I/O1 to 8	I/O9 to 16	MODE	I <sub>DD</sub>
L	H	X	X	X	X	X	X	High-Z	High-Z	Not Selected	I <sub>DD</sub> , I <sub>DD</sub> S1
L	X	L	X	X	X	X	X	High-Z	High-Z	Not Selected	I <sub>DD</sub> , I <sub>DD</sub> S1
L	L	H	H	H	SA	X	X	High-Z	High-Z	Output disable	I <sub>DD</sub> A, I <sub>DD</sub> A1
L	L	H	L	H	SA	X	X	Data Out	High-Z	Byte Read	I <sub>DD</sub> A, I <sub>DD</sub> A1
L	L	H	X	L	SA	X	X	Data In	High-Z	Byte Write	I <sub>DD</sub> A, I <sub>DD</sub> A1

X : High or Low

SA : available as address

### ● Selection of Word-mode or Byte-mode

It is possible to select Word-mode (262,144 words x 16-bit) or Byte-mode (524,288 words x 8-bit) by CIO-pin: CIO=V<sub>DD</sub> for Word-mode and CIO=V<sub>SS</sub> for Byte-mode.

During Reading data, Writing date, Standby mode, or Data retention, do not change the voltage on CIO.

#### (1) Word-mode (262,144 words x 16-bit)

In case of Word-mode, SA-pin is invalid and "High" or "Low" can be applied.

It is possible to control the data width by  $\overline{UB}$  and  $\overline{LB}$  pins.

#### (2) Byte-mode (524,288 words x 8-bit)

In case of Byte-mode, SA-pin can be used as an address pin.

$\overline{UB}$  and  $\overline{LB}$  pins are invalid and "High" or "Low" can be applied.

And I/O 9 to 16 are in "Hige-Z" states.

### ● Reading data

#### ● Word-mode

It is possible to control the data width by  $\overline{LB}$  and  $\overline{UB}$  pins.

#### (1) Reading data from lower byte

Data is able to be read when the address is set while holding  $\overline{CS1}$  = "Low", CS2= "High",  $\overline{OE}$  = "Low",  $\overline{LB}$  = "Low", and  $\overline{WE}$  = "High".

#### (2) Reading data from upper byte

Data is able to be read when the address is set while holding  $\overline{CS1}$  = "Low", CS2= "High",  $\overline{OE}$  = "Low",  $\overline{UB}$  = "Low", and  $\overline{WE}$  = "High".

#### (3) Reading data from both bytes

Data is able to be read when the address is set while holding  $\overline{CS1}$  = "Low", CS2= "High",  $\overline{OE}$  = "Low",  $\overline{UB}$  = "Low",  $\overline{LB}$  = "Low", and  $\overline{WE}$  = "High".

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## ● Byte-mode

### (1) Reading data from byte

Data is able to read when address and SA are set while holding  $\overline{CS1}$  = "Low", CS2= "High",  $\overline{OE}$  ="Low", and  $\overline{WE}$  = "High".

Since I/O pins are in "Hi-Z" state when  $\overline{OE}$  = "High", the data bus line can be used for any other objective, then access time is apparently able to be cut down.

## ● Writing data

### ● Word-mode

#### (1)Writing data into lower byte

There are the following four ways of writing data into the memory.

- i) Hold  $\overline{CS2}$  = "High",  $\overline{WE}$  = "Low",  $\overline{UB}$  = "High", and  $\overline{LB}$  = "Low", set address and give "Low" pulse to  $\overline{CS1}$ .
- ii) Hold  $\overline{CS1}$  = "Low",  $\overline{WE}$  = "Low",  $\overline{UB}$  = "High", and  $\overline{LB}$  = "Low", set address and give "High" pulse to CS2.
- iii) Hold  $\overline{CS1}$  = "Low", CS2 = "High",  $\overline{UB}$  = "High", and  $\overline{LB}$  = "Low", set address and give "Low" pulse to  $\overline{WE}$ .
- iv) Hold  $\overline{CS1}$  = "Low", CS2 = "High",  $\overline{WE}$  = "Low", and  $\overline{UB}$  = "High", set address and give "Low" pulse to  $\overline{LB}$ .

Anyway, data on I/O pins are latched up into the memory cell during  $\overline{CS1}$  = "Low", CS2 ="High",  $\overline{WE}$  and  $\overline{LB}$  = "Low".

#### (2)Writing data into upper byte

There are the following four ways of writing data into the memory.

- i) Hold  $\overline{CS2}$  = "High",  $\overline{WE}$  = "Low",  $\overline{LB}$  = "High", and  $\overline{UB}$  = "Low", set address and give "Low" pulse to  $\overline{CS1}$ .
- ii) Hold  $\overline{CS1}$  = "Low",  $\overline{WE}$  = "Low",  $\overline{LB}$  = "High", and  $\overline{UB}$  = "Low", set address and give "High" pulse to CS2.
- iii) Hold  $\overline{CS1}$  = "Low", CS2 = "High",  $\overline{LB}$  = "High", and  $\overline{UB}$  = "Low", set address and give "Low" pulse to  $\overline{WE}$ .
- iv) Hold  $\overline{CS1}$  = "Low", CS2 = "High",  $\overline{WE}$  = "Low", and  $\overline{LB}$  = "High", set address and give "Low" pulse to  $\overline{UB}$ .

Anyway, data on I/O pins are latched up into the memory cell during  $\overline{CS1}$  = "Low", CS2 ="High",  $\overline{WE}$  and  $\overline{UB}$  = "Low".

#### (3)Writing data into both bytes

There are the following four ways of writing data into the memory.

- i) Hold  $\overline{CS2}$  = "High",  $\overline{WE}$  = "Low",  $\overline{LB}$  and  $\overline{UB}$  = "Low", set address and give "Low" pulse to  $\overline{CS1}$ .
- ii) Hold  $\overline{CS1}$  = "Low",  $\overline{WE}$  = "Low",  $\overline{LB}$  and  $\overline{UB}$  = "Low", set address and give "High" pulse to CS2.
- iii) Hold  $\overline{CS1}$  = "Low", CS2 = "High",  $\overline{LB}$  and  $\overline{UB}$  = "Low", set address and give "Low" pulse to  $\overline{WE}$ .
- iv) Hold  $\overline{CS1}$  = "Low", CS2 = "High",  $\overline{WE}$  = "Low", set address and give "Low" pulse to  $\overline{LB}$  and  $\overline{UB}$ .

Anyway, data on I/O pins are latched up into the memory cell during  $\overline{CS1}$  = "Low", CS2 ="High",  $\overline{WE}$  = "Low",  $\overline{UB}$  and  $\overline{LB}$  = "Low".

### ● Byte-mode

#### (1)Writing data into byte

There are the following three ways of writing data into the memory.

- i) Hold  $\overline{CS2}$  = "High",  $\overline{WE}$  = "Low", set address and SA, then give "Low" pulse to  $\overline{CS1}$ .
- ii) Hold  $\overline{CS1}$  = "Low",  $\overline{WE}$  = "Low", set address and SA, then give "High" pulse to CS2.
- iii) Hold  $\overline{CS1}$  = "Low", CS2 = "High", set address and SA, then give "Low" pulse to  $\overline{WE}$ .

Anyway, data on I/O pins are latched up into the memory cell during  $\overline{CS1}$  = "Low", CS2 ="High", and  $\overline{WE}$  = "Low".

As DATA I/O pins are in "Hi-Z" when  $\overline{CS1}$  = "High", CS2 = "Low",  $\overline{OE}$  = "High", or  $\overline{LB}$  and  $\overline{UB}$  = "High" (Word-mode), the contention on the data bus can be avoided. But while I/O pins are in the output state, the data that is opposite to the output data should not be given.



## ● Standby mode

When  $\overline{CS1}$  is "High" or  $CS2$  is "Low" the chip is in the standby mode (only retaining data operation). In this case data I/O pins are Hi-Z, and all inputs of addresses,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and data are inhibited.

When  $\overline{CS1} = CS2 \geq V_{DD} - 0.2V$  or  $CS2 \leq 0.2V$ , there is almost no current flow except through the high resistance parts of the memory.

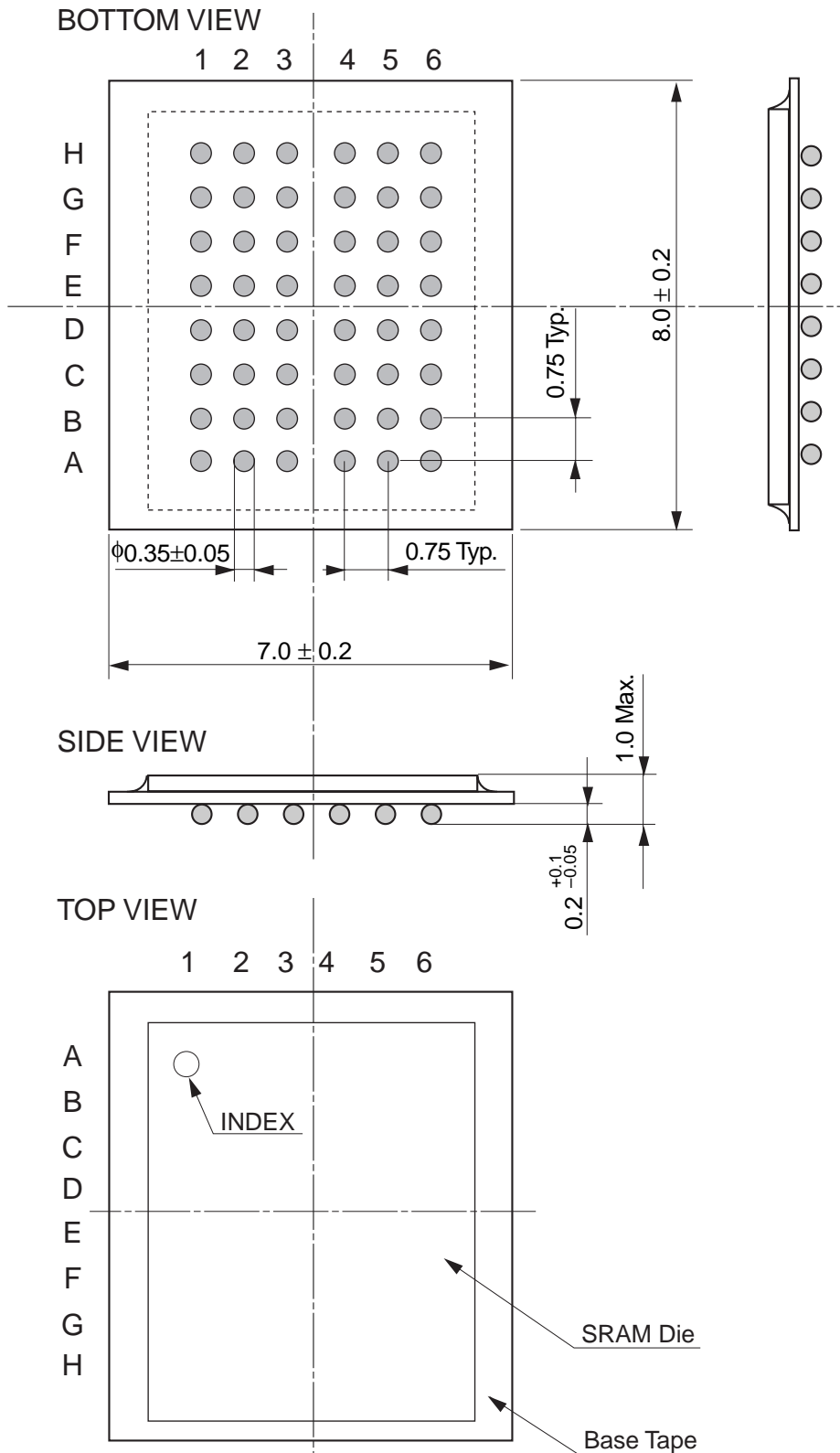
## ● Data retention at low voltage

In case of the data retention in the standby mode, the power supply can be gone down till the specified voltage. But it is impossible to write or read in this mode.

# S1M1V045B0J7

## PACKAGE DIMENSIONS

### TFBGA-48 pin



Unit : mm

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# S1M1V045B0J7

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First issue March, 2001  
Printed in Japan ®

Rev.1.0