GS1532
Serializer for HD-SDI, SD-SDI and DVB-ASI

PRELIMINARY DATA SHEET

KEY FEATURES

- **DVB-ASI support including 8b/10b coding and sync word insertion**
- **SMPTE 292M and SMPTE 259M-C compliant scrambling and NRZI coding (with bypass)**
- **CRC calculation and insertion**
- **line number calculation and insertion**
- **TRS calculation and insertion**
- **illegal code re-mapping**
- **20 bit / 10 bit CMOS parallel input data bus**
- **148.5MHz / 74.25MHz / 27MHz / 13.5MHz parallel digital input**
- **EDH generation and insertion**
- **adjustable loop bandwidth**
- **1.8V core power supply and 3.3V charge pump power supply**
- **3.3V digital I/O supply**
- **JTAG test interface**
- **small footprint compatible with GS1560, GS1561, GS9060 and GS9062**
- **low power operation (typically 460mW for HD)**

APPLICATIONS

- SMPTE 292M Serial Digital Interfaces
- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

DESCRIPTION

The GS1532 is a multi-standard serializer with an integrated cable driver. When used in conjunction with the GO1525 voltage controlled oscillator, a transmit solution for HD-SDI, SD-SDI and DVB-ASI applications can be realized.

This device performs the functions of parallel to serial conversion, scrambling as per SMPTE 292M/259M-C and NRZ-to-NRZI conversion. The SMPTE scrambler may optionally be bypassed to support the transmission of other coding schemes.

In addition, the device can insert TRS signals, calculate and insert line numbers and CRC's, re-map illegal code words and insert SMPTE 352M payload identifier packets. All processing features are optional and may be enabled/ disabled via external control pin(s) and/or host interface programming.

The GS1532 may also be used in data pass-through mode where no processing of the data is performed.

Parallel data inputs are provided in both 10-bit multiplexed and 20-bit demultiplexed format for HD and SD signal rates. An associated parallel clock input signal is provided operating at: 148.5 or 148.5/1.001MHz, (HDTV 10-bit multiplexed input); 74.25 or 74.25/1.001MHz, (HDTV 20-bit demultiplexed input); 27MHz, (SDTV 10-bit multiplexed input); and 13.5MHz, (SDTV 20-bit demultiplexed input).

The integrated cable driver features an output mute on loss of parallel clock, high impedance mode, adjustable signal swing, and automatic dual slew rate selection depending on HD/SD operational requirements.

The device may also be configured for DVB-ASI operation where it will insert K28.5 sync words and 8b/10b encode the data stream prior to transmission.

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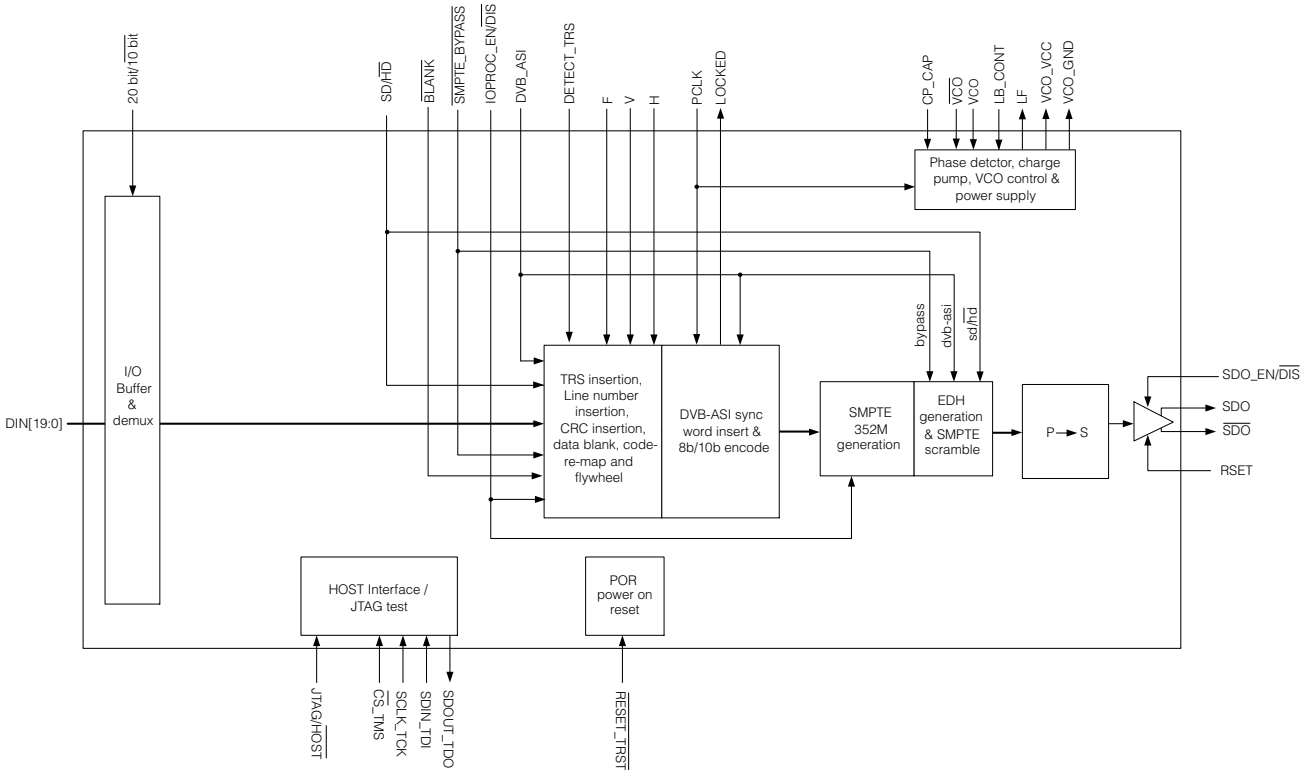
GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
www.gennum.com



GS1532 FUNCTIONAL BLOCK DIAGRAM

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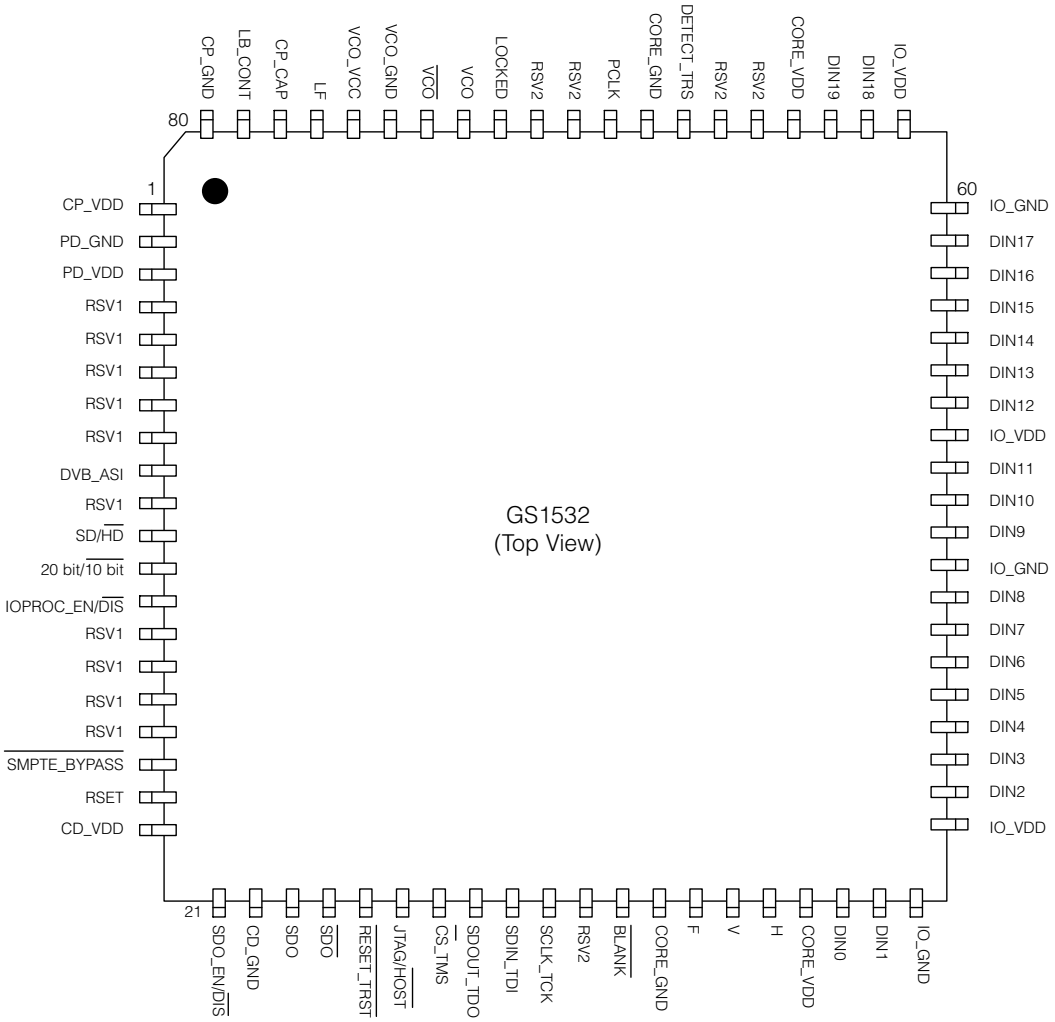
1. PIN OUT

1.1 PIN ASSIGNMENT



1.2 PIN DESCRIPTIONS

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
1	CP_VDD	Analog	Input Power	Power supply connection for the charge pump 3.3V DC
2	PD_GND	Analog	Input Power	GND pin for the phase detector
3	PD_VDD	Analog	Input Power	Power supply for the Phase Detector 1.8V DC
9	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH, the device will be configured for the transmission of DVB-ASI data in SDTV mode, (SD/$\overline{HD}$ must be HIGH and $\overline{SMPTE\_BYPASS}$ must be LOW). When set LOW, the device will not support the encoding of DVB-ASI data.
11	SD/$\overline{HD}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select the current video rate as either 1.484 Gb/s HDTV or 270Mb/s SDTV. When SD/$\overline{HD}$ is HIGH, the mode is 270Mb/s. The setting of this pin also determines the parallel input / output clock rate and the slew rate of the cable driver output.
12	20bit/$\overline{10bit}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select the input bus width in SMPTE or Data-Through modes.
13	IOPROC_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable I/O processing features When IOPROC_EN/$\overline{DIS}$ is HIGH, the following I/O processing features of the device are enabled. • TRS insertion • Line CRC insertion (HD-only) • Line Number insertion (HD-only) • Ancillary data checksum insertion • EDH CRC insertion (SD-only) • 8b/10b encoding (DVB-ASI only) To enable a subset of these features keep IOPROC_EN/$\overline{DIS}$ HIGH and disable features in the host iterface. When IOPROC_EN/$\overline{DIS}$ is LOW, the I/O processing features of the device are disabled, regardless of whether the features are enabled in the host interface.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
18	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable / disable all SMPTE encoding, scrambling and word alignment. When set LOW, SMPTE scrambling and encoding will be disabled. When set HIGH, the device will carry out SMPTE scrambling / coding. (DVB_ASI must be LOW)
19	RSET	Analog	Input	CONTROL SIGNAL INPUT An external 1% resistor connected to this input is used to set the SDO / $\overline{\text{SDO}}$ output signal amplitude.
20	CD_VDD	Analog	Input Power	Power supply for the serial digital cable driver 1.8V DC
21	SDO_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the serial digital output stage. When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When connected to logic HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.
22	CD_GND	Analog	Input Power	GND connection - serial digital cable driver
23, 24	SDO, $\overline{\text{SDO}}$	Analog	Output	SERIAL DATA OUTPUT SIGNAL Serial digital output signal from the parallel to serial converter operating at 1.485Gb/s, 1.485 /1.001Gb/s, or 270Mb/s. The slew rate of the output is automatically controlled to meet SMPTE 292M and 259M specifications according to the setting of the SD/$\overline{\text{HD}}$ pin. NOTE: The SDO / $\overline{\text{SDO}}$ output signals will be forced to a logic LOW level when the LOCKED pin = LOW.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
25	$\overline{\text{RESET\_TRST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Normal mode (JTAG/$\overline{\text{HOST}}$ = LOW) When LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance including the serial digital outputs SDO and $\overline{\text{SDO}}$. When HIGH, normal operation of the device resumes 10µsec after the low to high transition of the $\overline{\text{RESET\_TRST}}$ signal. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH) When LOW, all functional blocks will be set to default and the JTAG test sequence will be held reset. When HIGH, normal operation of the JTAG test sequence resumes.
26	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK pins are configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, the above pins are configured for normal host interface operation.
27	$\overline{\text{CS}}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Chip Select / Test Mode Select When JTAG/$\overline{\text{HOST}}$ = HIGH, this pin is JTAG TMS. When JTAG/$\overline{\text{HOST}}$ = LOW, this pin operates as the host interface chip select and is active LOW.
28	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Output / Test Data Output When JTAG/$\overline{\text{HOST}}$ = HIGH, this pin is JTAG TDO. When JTAG/$\overline{\text{HOST}}$ = LOW, this pin is used to read status and configuration data from the device.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
29	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data In / Test Data In When JTAG/$\overline{\text{HOST}}$ = HIGH, this pin is JTAG TDI When JTAG/$\overline{\text{HOST}}$ = LOW, this pin is used to write address and configuration data words into the device.
30	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Clock / Test Clock When JTAG/$\overline{\text{HOST}}$ = HIGH, this pin is JTAG TCK When JTAG/$\overline{\text{HOST}}$ = LOW, the host interface address and data is shifted into / out of the device synchronously with this clock.
32	$\overline{\text{BLANK}}$	Synchronous with PCLK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When $\overline{\text{BLANK}}$ is LOW, the GS1532 sets the Luma and Chroma input data to their appropriate blanking levels. When $\overline{\text{BLANK}}$ is HIGH, the Luma and Chroma data pass through this device unaltered.
33	CORE_GND	Non Synchronous	Input Power	GND connection - Digital logic
34	F	Synchronous with PCLK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. The F signal is used to indicate the ODD/EVEN field of the video signal. The F signal will go HIGH for the entire period of field 2 as indicated by the F bit in the received TRS signals. The F signal will be LOW for all lines in field 1 and for all lines in progressive scan systems. The GS1532 uses the F input signal for internal timing generation (when DETECT_TRS = LOW) and will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH. The F input is ignored when DETECT_TRS is HIGH.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
35	V	Synchronous with PCLK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. The V signal is used to indicate the portion of the video field / frame that is used for vertical blanking. The V signal will be HIGH for the entire vertical blanking period. The GS1532 uses the V input signal for internal timing generation (when DETECT_TRS = LOW) and will set the V bit in all outgoing TRS signals for the entire period that the V input signal is HIGH (when IOPROC_EN/$\overline{\text{DIS}}$ is HIGH). The V input is ignored when DETECT_TRS is HIGH.
36	H	Synchronous with PCLK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. The H signal is used to indicate the portion of the video line containing active video data. Active Line Blanking By default, the H signal should be LOW for the active portion of the video line. The signal goes LOW at the first active pixel of the line, and then goes HIGH after the last active pixel of the line. The H signal should remain HIGH throughout the horizontal blanking period (including both SAV and EAV TRS). TRS Based Blanking The timing of this signal is programmable via the host interface such that the H timing can be changed to be HIGH for the entire horizontal blanking period as indicated by the H bit in the TRS words. The GS1532 uses the H input signal for internal timing generation (when DETECT_TRS = LOW) and will use this signal in the generation of the TRS signals (when IOPROC_EN/$\overline{\text{DIS}}$ is HIGH). The H input is ignored when DETECT_TRS is HIGH.
37	CORE_VDD	Non Synchronous	Input Power	Power connection - Digital logic 1.8V DC

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION	
38, 39, 42~48, 50	DIN[0:9]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS / LVTTL compatible.	
				HDTV 20 bit mode SD/$\overline{HD}$ = LOW 20 bit/$\overline{10\ bit}$ = HIGH	Chroma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW
				HDTV 10 bit mode SD/$\overline{HD}$ = LOW 20 bit/$\overline{10\ bit}$ = LOW	Must be connected to GND
				SDTV 20 bit mode SD/$\overline{HD}$ = HIGH 20 bit/$\overline{10\ bit}$ = HIGH	Chroma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH, DVB_ASI = LOW Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW, DVB_ASI = LOW Must be connected to GND in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW, DVB_ASI = HIGH
				SDTV 10 bit mode SD/$\overline{HD}$ = HIGH 20 bit/$\overline{10\ bit}$ = LOW	Must be connected to GND
40, 49	IO_GND	Non Synchronous	Input Power	GND connection - Digital I/O	
41, 53	IO_VDD	Non Synchronous	Input Power	Power connection - Digital I/O 3.3V DC.	

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION	
51, 52, 54~59, 62, 63	DIN[10:19]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS / LVTTL compatible.	
				HDTV 20 bit mode SD/$\overline{HD}$ = LOW 20 bit/$\overline{10\ bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW
				HDTV 10 bit mode SD/$\overline{HD}$= LOW 20 bit/$\overline{10\ bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW
				SDTV 20 bit mode SD/$\overline{HD}$ = HIGH 20 bit/$\overline{10\ bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH, DVB_ASI = LOW Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW, DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW, DVB_ASI = HIGH
				SDTV 10 bit mode SD/$\overline{HD}$ = HIGH 20 bit/$\overline{10\ bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH, DVB_ASI = LOW Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW, DVB_ASI = HIGH
60	IO_GND	Non Synchronous	Input Power	GND connection - Digital I/O	
61	IO_VDD	Non Synchronous	Input Power	Power connection - Digital I/O 3.3V DC.	
64	CORE_VDD	Non Synchronous	Input Power	Power connection - Digital logic 1.8V DC.	

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
67	DETECT_TRS	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select external HVF timing mode or TRS extraction timing mode. When DETECT_TRS is LOW, the device will extract all internal timing information from the supplied H:V:F timing signals. When DETECT TRS is HIGH, the device will extract all internal timing information from TRS signals embedded in the supplied video stream.
68	CORE_GND	Non Synchronous	Input Power	GND connection - Digital logic
69	PCLK		Input	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS / LVTTL compatible. HDTV 20 bit mode: PCLK = 74.25MHz (or 74.25/1.001MHz) HDTV 10 bit mode: PCLK = 148. 5MHz (or 148.5/1.001MHz) SDTV 20 bit mode: PCLK = 13.5MHz SDTV 10 bit mode: PCLK = 27MHz
72	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL Output Signal levels are LVCMOS / LVTTL compatible. This signal will be HIGH when the PLL has achieved lock to the supplied PCLK signal. This pin will be LOW under all other conditions. When this signal is LOW, the serial digital output SDO / $\overline{\text{SDO}}$ will be forced to a logic level LOW.
73,74	VCO, $\overline{\text{VCO}}$	Analog	Input	Differential inputs for the external VCO. For single ended devices such as the GO1525, $\overline{\text{VCO}}$ should be decoupled to GND.
75	VCO_GND	Analog	Output Power	GND pin for the voltage controlled oscillator. (Internal regulator output)
76	VCO_VCC	Analog	Output Power	Power supply for the voltage controlled oscillator 2.5V DC supplied by the device to the external VCO. (Internal regulator output).
77	LF	Analog	Output	Control voltage to external VCO.
78	CP_CAP	Analog	Input	PLL lock time constant capacitor connection.
79	LB_CONT	Analog	Input	CONTROL SIGNAL INPUT Control voltage to set the loop bandwidth of the PLL.
80	CP_GND	Analog	Input Power	GND pin for the charge pump.
4, 5, 6, 7, 8, 10, 14, 15, 16, 17	RSV1	-	-	Reserved - connect to PD_GND.
31, 65, 66, 70, 71	RSV2	-	-	Reserved - connect to CORE_GND.

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIUMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +4.6V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
Lead Temperature (soldering, 10 sec)	230°C

NOTES:
1. See reflow profile solder

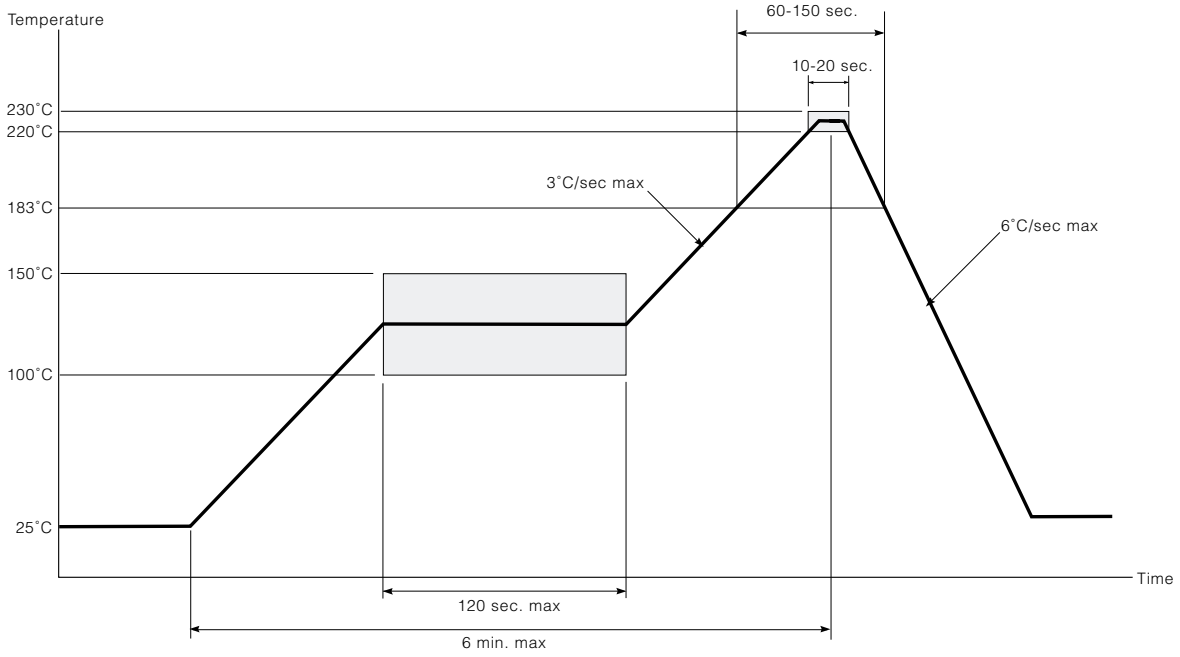


Fig. 1 Reflow Solder Profile

2.2 DC ELECTRICAL CHARACTERISTICS

V_{DDCORE} = 1.8V, V_{DDIO} = 3.3V T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL	NOTES
Operating Temperature Range	T_A		0	25	70	°C		1
Positive Core Supply Voltage	CORE_VDD		1.65	1.8	1.95	V	1	
Positive I/O Supply Voltage	IO_VDD		3.0	3.3	3.6	V	1	
Charge Pump Supply Voltage	CP_VDD		3.0	3.3	3.6	V	1	
Phase Detector Supply Voltage	PD_VDD		1.65	1.8	1.95	V	1	
External VCO Regulator Voltage	VCO_VCC		2.25	2.5	2.75	V	1	
Cable Driver Supply Voltage	CD_VDD		1.71	1.8	1.89	V	1	
Supply Current (Total)		V_{DD} = Max, IO = Max, T=70°C	-	190	260	mA	2	
Power (System Total)	P_D (HD)	V_{DD} = Max, IO = Max, T=70°C	-	460	570	mW	7	
	P_D (SD)	V_{DD} = Max, IO = Max, T=70°C	-	420	535	mW	7	
Input Voltage LOW	V_{IL}		-	-	0.8	V	1	
Input Voltage HIGH	V_{IH}		2.1	-	-	V	1	
Output Voltage LOW	V_{OL}		-	0.2	0.4	V	1	
Output Voltage HIGH	V_{OH}		V_{DDIO} - 0.4	-	-	V	1	
Output Common Mode	V_{CM}	75Ω load, RSET=280Ω, SD and HD	0.8	1.0	1.2	V	1	
RSET Voltage	V_{RSET}	RSET=280Ω	0.54	0.6	0.66	mV	1	2
ESD Protection on all Pins			1	-	-	kV		3

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. All DC and AC electrical parameters within specification.
2. Set by value of RSET resistor.
3. MIL STD 883 ESD protection will be applied to all pins on the device.

2.3 AC ELECTRICAL CHARACTERISTICS

V_{DDCORE} = 1.8V, V_{DDIO} = 3.3V T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL	NOTES
Serial Output Data Rate	DR_{SDO}		-	1.485, 1.485/1.001, 270	-	Gb/s Gb/s Mb/s	1	
Serial Output RiseTime 20% ~ 80%	tr_{SDO}	No compensation for return loss - SMPTE 292M signal	-	150	230	ps		
		Return loss compensation recommended circuit SMPTE 292M signal	-	200	260	ps	1	
		SMPTE 259M-C signal	400	550	1500	ps	1	
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	No compensation for return loss - SMPTE 292M signal	-	150	230	ps		
		Return loss compensation recommended circuit - SMPTE 292M signal	-	235	260	ps	1	
		SMPTE 259M-C signal	400	550	1500	ps	1	
Serial Output Intrinsic Jitter	t_{IJ}	Pseudo-random and pathological HD signal	-	90	125	ps	1	
	t_{IJ}	Pseudo-random and pathological SD signal	-	270	350	ps	1	
Serial Output Duty Cycle Distortion		HD	-	10	-	%	1	
		SD (270Mb/s)	-	20	-	%	1	
Parallel Clock Frequency	f_{PCLK}		13.5	-	148.5	MHz	1	
Parallel Clock Duty Cycle			40	50	60	%	3	
Input Data Setup Time	t_{SU}	50% levels	1.5	-	-	ns	3	
Input Data Hold Time	t_{IH}	50% levels	-	-	1.5	ns	3	
GSPI Input Clock Frequency	$f_{GSPICLK}$		-	-	6.6	MHz	1	
GSPI Input Clock Duty Cycle	DS		40	50	60	%	3	
GSPI Data Setup Time	t_{SUGSPI}		0	-	-	ns	3	
GSPI Data Hold Time	$t_{HOLDGSPI}$		-	-	1.43	ns	3	

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

2.4 INPUT/OUTPUT CIRCUITS

All resistors in ohms, all capacitors in farads, unless otherwise shown.

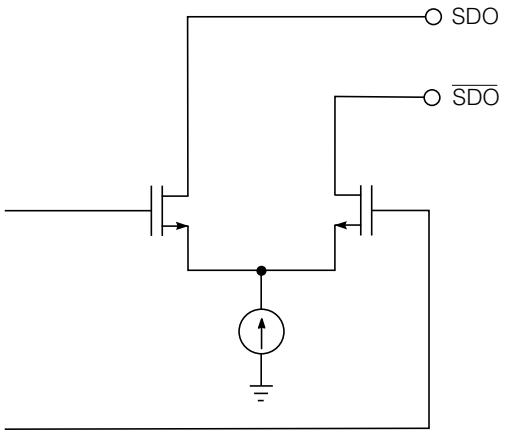


Fig. 2 Serial Digital Output

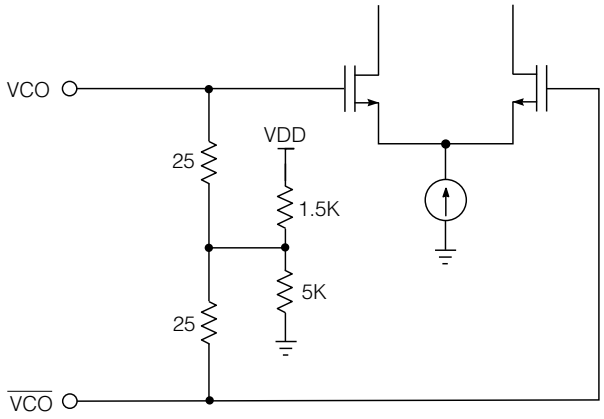


Fig. 3 VCO Input

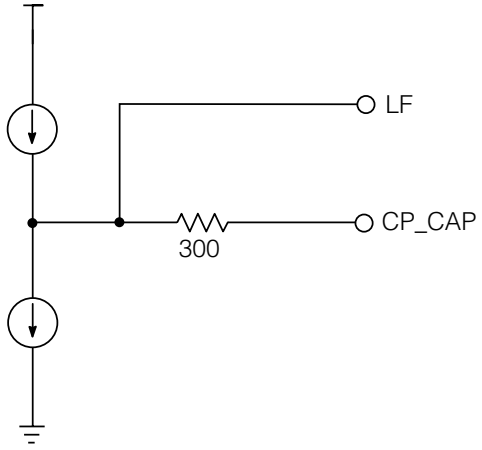


Fig. 4 VCO Control Output & PLL Lock Time Capacitor

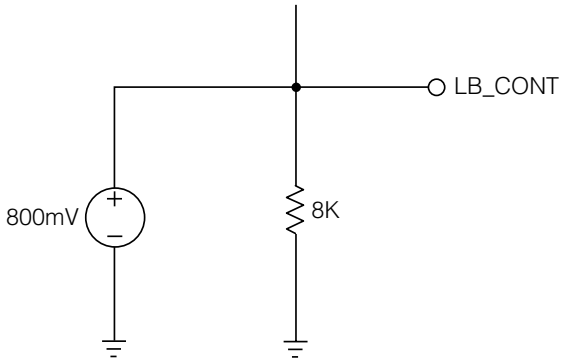


Fig. 5 PLL Loop Bandwidth Control

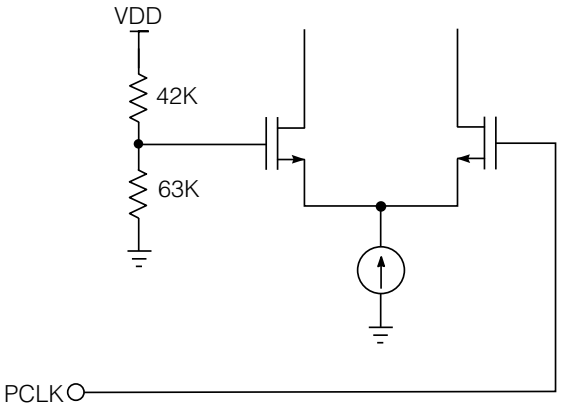


Fig. 6 PCLK Input

2.5 HOST INTERFACE

Table: 1 Host Interface Description

REGISTER NAME	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
IOPROC_DISABLE	Not Used		000	15-9		
	H_CONFIG	Horizontal sync timing input configuration. Set LOW when the H input timing is based on active line blanking. Set HIGH when the H input timing is based on the H bit of the TRS words. See Figure 15.		8		
	Not Used			7		
	352M_INS	SMPTE352M packet insertion. In HD mode, inserts the 352M packet in the Y channel only when the four VIDEO_FORMAT registers are programmed with non-zero values and when IOPROC_EN/$\overline{\text{DIS}}$ is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH. This bit must be set LOW.		6	R/W	0
	ILLEGAL_REMAP	Illegal Code Re-mapping. Detection and correction of illegal code words within the active picture area (AP). Set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin and $\overline{\text{SMPTE\_BYPASS}}$ pin must be set HIGH.		5	R/W	0 (enabled)
	EDH_CRC_INS	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction. In SD mode the GS1532 will generate and insert EDH packets. Set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin and $\overline{\text{SMPTE\_BYPASS}}$ pin must be set HIGH.		4	R/W	0 (enabled)
	ANC_CSUM_INS	Ancillary Data Check-sum insertion. Set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin and $\overline{\text{SMPTE\_BYPASS}}$ pin must be set HIGH.		3	R/W	0 (enabled)
	CRC_INS	Y and C line based CRC insertion. In HD mode, inserts line based CRC words in both the Y and C channels. Set HIGH to disable The IOPROC_EN/$\overline{\text{DIS}}$ pin and $\overline{\text{SMPTE\_BYPASS}}$ pin must be set HIGH.		2	R/W	0 (enabled)
	LNUM_INS	Y and C line number insertion. In HD mode set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin and $\overline{\text{SMPTE\_BYPASS}}$ pin must be set HIGH.		1	R/W	0 (enabled)
	TRS_INS	Timing Reference Signal Insertion. Only occurs when IOPROC_EN/$\overline{\text{DIS}}$ is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH. This bit must be set LOW.		0	R/W	0 (disable)
Not Used			001	15-0		

Table 2: Host Interface Description

REGISTER NAME	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
EDH_FLAG	Not Used		002	15		
	ANC-UES	Ancillary Unknown Error Status will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		14	R/W	
	ANC-IDA	Ancillary Internal device error Detected Already will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		13	R/W	
	ANC-IDH	Ancillary Internal device error Detected Here will be generated and inserted when IOPROC_EN//$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		12	R/W	
	ANC-EDA	Ancillary Error Detected Already will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		11	R/W	
	ANC-EDH	Ancillary Error Detected Here will be generated and inserted when IOPROC_EN//$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		10	R/W	
	FF-UES	Full Field Unknown Error will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		9	R/W	
	FF-IDA	Full Field Internal device error Detected Already will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		8	R/W	
	FF-IDH	Full Field Internal device error Detected will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		7	R/W	
	FF-EDA	Full Field Error Detected Already will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		6	R/W	
	FF-EDH	Full Field Error Detected Here will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		5	R/W	

Table 2: Host Interface Description (Continued)

REGISTER NAME	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
EDH_FLAG	AP-UES	Active Picture Unknown Error Status will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.	002	4	R/W	
	AP-IDA	Active Picture Internal device error Detected Already will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		3	R/W	
	AP-IDH	Active Picture Internal device error Detected Here will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		2	R/W	
	AP-EDA	Active Picture Error Detected Already will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		1	R/W	
	AP-EDH	Active Picture Error Detected Here will be generated and inserted when IOPROC_EN/$\overline{DIS}$ and $\overline{SMPTE\_BYPASS}$ pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only.		0	R/W	

Table 3: Host Interface Description

REGISTER NAME	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Not Used			003	15-0		
VIDEO_STANDARD	Not Used		004	15		
	VD_STD[4:0]	Video Data Standard (see Table 7)		14-10	R	0
	INT_PROG	Interlace/Progressive: Set LOW if detected video standard is PROGRESSIVE and is set HIGH if it is INTERLACED.		9	R	0
	STD_LOCK	Standard Lock: Set HIGH when flywheel has achieved full synchronization.		8	R	0
	Not Used			7-0		

Table 4: Host Interface Description

REGISTER NAME	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Not Used			005	15-0		
Not Used			006	15-0		
Not Used			007	15-0		
Not Used			008	15-0		
Not Used			009	15-0		
VIDEO_FORMAT	SMPTE 352M Byte 2	SMPTE 352M Byte 2 information must be programmed in this register when 352M_INS = LOW	010	15-8	R/W	0
	SMPTE 352M Byte 1	SMPTE 352M Byte 1 information must be programmed in this register when 352M_INS = LOW		7-0	R/W	0
	SMPTE 352M Byte 4	SMPTE 352M Byte 4 information must be programmed in this register when 352M_INS = LOW	011	15-8	R/W	0
	SMPTE 352M Byte 3	SMPTE 352M Byte 3 information must be programmed in this register when 352M_INS = LOW		7-0	R/W	0
Not Used			012	15-0		
Not Used			013	15-0		

Table 5: Host Interface Description

REGISTER NAME	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
RASTER_STRUCTURE	Not Used		014	15-12		
	RASTER_STRUCTURE_1 [11:0]	Words Per Active Line		11-0	R	0
	Not Used		015	15-12		
	RASTER_STRUCTURE_2 [11:0]	Words Per Total Line.		11-0	R	0
	Not Used		016	15-11		
	RASTER_STRUCTURE_3 [10:0]	Total Lines Per Frame		10-0	R	0
	Not Used		017	15-11		
	RASTER_STRUCTURE_4 [10:0]	Active Lines Per Field		10-0	R	0

Table 6: Host Interface Description

REGISTER NAME	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
AP_LINE_START_F0	Not Used		018	15-10		
	AP_LINE_START_F0 [9:0]	Field 0 Active Picture start line data used to set EDH calculation range outside of RP 165 values.		9-0	R/W	0
AP_LINE_END_F0	Not Used		019	15-10		
	AP_LINE_END_F0 [9:0]	Field 0 Active Picture end line data used to set EDH calculation range outside of RP 165 values.		9-0	R/W	0
AP_LINE_START_F1	Not Used		020	15-10		
	AP_LINE_START_F1 [9:0]	Field 1 Active Picture start line data used to set EDH calculation range outside of RP 165 values.		9-0	R/W	0
AP_LINE_END_F1	Not Used		021	15-10		
	AP_LINE_END_F1 [9:0]	Field 1 Active Picture end line data used to set EDH calculation range outside of RP 165 values.		9-0	R/W	0
FF_LINE_START_F0	Not Used		022	15-10		
	FF_LINE_START_F0 [9:0]	Field 0 Full Field start line data used to set EDH calculation range outside of RP 165 values.		9-0	R/W	0
FF_LINE_END_F0	Not Used		023	15-10		
	FF_LINE_END_F0 [9:0]	Field 0 Full Field end line data used to set EDH calculation range outside of RP 165 values.		9-0	R/W	0
FF_LINE_START_F1	Not Used		024	15-10		
	FF_LINE_START_F1 [9:0]	Field 1 Full Field start line data used to set EDH calculation range outside of RP-165 values.		9-0	R/W	0
FF_LINE_END_F1	Not Used		025	15-10		
	FF_LINE_END_F1	Field 1 Full Field end line data used to set EDH calculation range outside of RP-165 values.		9-0	R/W	0
Not Used			026	15-0		
LINE_0_352M	Not Used		027	15-11		
	LINE_0_352M[10:0]	Data bit 10 of first line where SMPTE352M packet is inserted. This line number overrides the standard line number.		10-0	R/W	0
LINE_1_352M	Not Used		028	15-11		
	LINE_1_352M[10:0]	Second line where SMPTE352M packet is inserted. This line number overrides the standard line number.		10-0	R/W	0

Table 7: Supported Video Standards (VD_STD)

SMPTE STANDARD	ACTIVE VIDEO AREA	LENGTH OF HANC	LENGTH OF ACTIVE VIDEO	TOTAL SAMPLES	SMPTE 352M LINES	VD_STD[4:0]
260M (HD)	1920x1035/60 (2:1)	268	1920	2200	10, 572	15h
295M (HD)	1920x1080/50 (2:1)	444	1920	2376	10, 572	14h
274M (HD)	1920x1080/60 (2:1) or 1920x1080/30 (PsF)	268	1920	2200	10, 572	0Ah
	1920x1080/50 (2:1) or 1920x1080/25 (PsF)	708	1920	2640	10, 572	0Ch
	1920x1080/30 (1:1)	268	1920	2200	18	0Bh
	1920x1080/25 (1:1)	708	1920	2640	18	0Dh
	1920x1080/24 (1:1)	818	1920	2750	18	10h
	1920x1080/24 (PsF)	818	1920	2750	10, 572	11h
	1920x1080/25 (1:1) - EM	324	2304	2640	18	0Eh
	1920x1080/25 (PsF) - EM	324	2304	2640	10, 572	0Fh
	1920x1080/24 (1:1) - EM	338	2400	2750	18	12h
	1920x1080/24 (PsF) - EM	338	2400	2750	10, 572	13h
296M (HD)	1280x720/30 (1:1)	2008	1280	3300	13	02h
	1280x720/30 (1:1) - EM	408	2880	3300	13	03h
	1280x720/50 (1:1)	688	1280	1980	13	04h
	1280x720/50 (1:1) - EM	240	1728	1980	13	05h
	1280x720/25 (1:1)	2668	1280	3960	13	06h
	1280x720/25 (1:1) - EM	492	3456	3960	13	07h
	1280x720/24 (1:1)	2833	1280	4125	13	08h
	1280x720/24 (1:1) - EM	513	3600	4125	13	09h
	1280x720/60 (1:1)	358	1280	1650	13	00h
	1280x720/60 (1:1) - EM	198	1440	1650	13	01h
125M (SD)	1440x487/60 (2:1)(Or dual link progressive)	268	1440	1716	3, 276	16h
	1440x507/60 (2:1)	268	1440	1716	3, 276	17h
	525-line 487 generic	-	-	1716	3, 276	19h
	525-line 507 generic	-	-	1716	3, 276	1Bh
ITU-R BT.656 (SD)	1440x576/50 (2:1)	268	1440	1716	3, 276	18h
	625-line generic (EM)	-	-	1728	9, 322	1Ah
Unknown HD	SD/$\overline{HD}$ = 0	-	-	-	-	1Dh
Unknown SD	SD/$\overline{HD}$ = 1	-	-	-	-	1Eh
Reserved						1Ch, 1Fh

HOST INTERFACE MAP

HOST Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line 1 352M[10:0]	28	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Line 0 352M[10:0]	27	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	26	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
FF_LINE_END_F1[9:0]	25	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[9:0]	24	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[9:0]	23	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[9:0]	22	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[9:0]	21	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[9:0]	20	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[9:0]	19	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[9:0]	18	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE _4[10:0]	17	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE _3[10:0]	16	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE _2[11:0]	15	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE _1[11:0]	14	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RESERVED	13	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
RESERVED	12	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
VIDEO_FORMAT(4,3)[[7:0][7:0]	11	VF4-b7	VF4-b6	VF4-b5	VF4-b4	VF4-b3	VF4-b2	VF4-b1	VF4-b0	VF3-b7	VF3-b6	VF3-b5	VF3-b4	VF3-b3	VF3-b2	VF3-b1	VF3-b0
VIDEO_FORMAT(2,1)[[7:0][7:0]	10	VF2-b7	VF2-b6	VF2-b5	VF2-b4	VF2-b3	VF2-b2	VF2-b1	VF2-b0	VF1-b7	VF1-b6	VF1-b5	VF1-b4	VF1-b3	VF1-b2	VF1-b1	VF1-b0
	9	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
	8	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
	7	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
	6	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
	5	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
VIDEO_STANDARD	4	Not Used	VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0	Not Used	STD_LOCK	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
	3	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
EDH_FLAG_REGISTER	2	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	1	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
I/O PROCESSING	0	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	H_CONFIG	Not Used	352M _INS	ILLEGAL _REMAP	EDH_CRC _INS	ANC_CSUM _INS	Not Used	Not Used	TRS _INS

HOST INTERFACE MAP (READ ONLY REGISTERS)

HOST Table Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	28																
	27																
	26																
	25																
	24																
	23																
	22																
	21																
	20																
	19																
	18																
RASTER_STRUCTURE_4[10:0]	17						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE_3[10:0]	16						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE_2[11:0]	15					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE_1[11:0]	14					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	13																
	12																
	11																
	10																
	9																
	8																
	7																
	6																
	5																
VIDEO_STANDARD	4		VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0		STD_LOCK								
	3																
	2																
	1																
	0																

HOST INTERFACE MAP (R/W CONFIGURABLE REGISTERS)

HOST Table Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line 1 352M[10:0]	28						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Line 0 352M[10:0]	27						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	26																
FF_LINE_END_F1[10:0]	25							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	24							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	23							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	22							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	21							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	20							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	19							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	18							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	17																
	16																
	15																
	14																
	13																
	12																
VIDEO_FORMAT(4,3)[[7:0][7:0]	11	VF4-b7	VF4-b6	VF4-b5	VF4-b4	VF4-b3	VF4-b2	VF4-b1	VF4-b0	VF3-b7	VF3-b6	VF3-b5	VF3-b4	VF3-b3	VF3-b2	VF3-b1	VF3-b0
VIDEO_FORMAT(2,1)[[7:0][7:0]	10	VF2-b7	VF2-b6	VF2-b5	VF2-b4	VF2-b3	VF2-b2	VF2-b1	VF2-b0	VF1-b7	VF1-b6	VF1-b5	VF1-b4	VF1-b3	VF1-b2	VF1-b1	VF1-b0
	9																
	8																
	7																
	6																
	5																
	4																
	3																
EDH_FLAG_REGISTER	2		ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	1																
IOPROC_DISABLE_REGISTER	0								H_CONFIG		352M _INS	ILLEGAL _REMAP	EDH_CRC _INS	ANC_CSUM _INS			TRS _INS

3. DETAILED DESCRIPTION

3.1 GSPI - APPLICATION LAYER HOST INTERFACE

The GSPI, or Gennum Serial Peripheral Interface is a 4-wire interface provided to allow the application layer to access additional status information through configuration registers in the GS1532.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided.

When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled. When JTAG/$\overline{HOST}$ is HIGH, the JTAG interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin is a high-impedance output allowing multiple devices to be connected. The interface is illustrated in the Figure 7.

All read or write access to the GS1532 is initiated and terminated by the application host processor. Each access always begins with a command / address word followed by a data read or write to/from the GS1532.

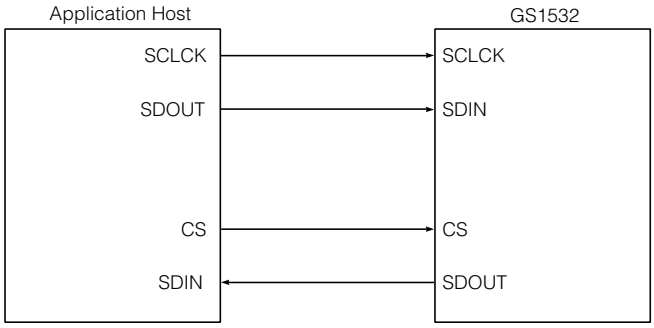


Fig. 7 GSPI Application Interface Connection

3.1.1 Command Word Description

The command word consists of a 16-bit word transmitted MSB first and contains a read/write bit, nine reserved bits and a 6-bit address.

Command words are clocked into the deserializer on the rising edge of the serial clock SCLK, which operates in a burst fashion. The chip select $\overline{CS}$ signal must be active low for at least 1.5ns (t_0 in Figure 10) before the first clock edge to ensure proper operation.

R/W: Read command if R/W='1', write command if R/W='0'.

RSV: Reserved for additional functionality

[A5:A0]: Address

Each command word must be followed by only one data word to ensure proper operation.

3.1.2 Data Read or Write Access

Serial data is transmitted or received MSB first synchronous with the rising edge of the serial clock SCLK. The chip select $\overline{CS}$ signal must be active low for at least 1.5ns (t_0 in Figure 10) before the first clock edge to ensure proper operation. The first bit (MSB) of the serial output SDOUT is available 12ns (t_4 in Figure 11) following the last falling SCLK edge of the read command word, the remaining bits are clocked out on the negative edges of SCLK. Figures 10 and 11 illustrate the interface timing.

The device will not drive any signal out during the power up phase or when the external $\overline{RESET\_TRST}$ pin is asserted LOW.

Fig. 8 Command Word Format

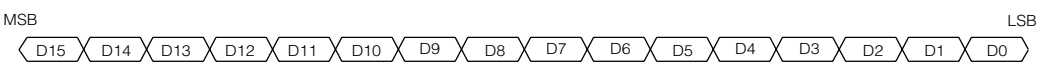


Fig. 9 Data Word Format

3.1.3 GSPI Timing

Write and read mode timing for the GSPI interface is as shown in the following diagrams.

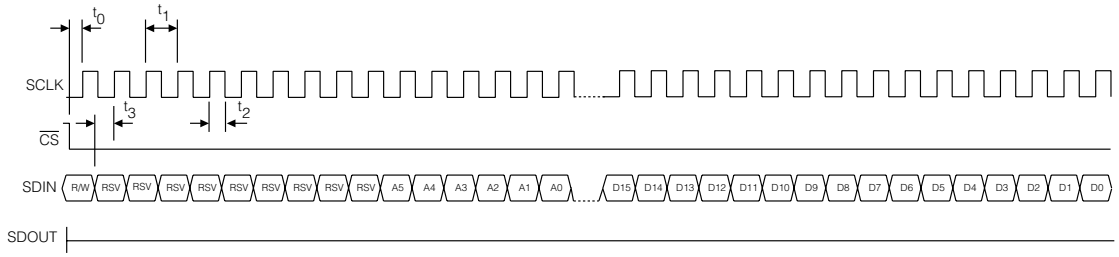


Fig. 10 Write Mode

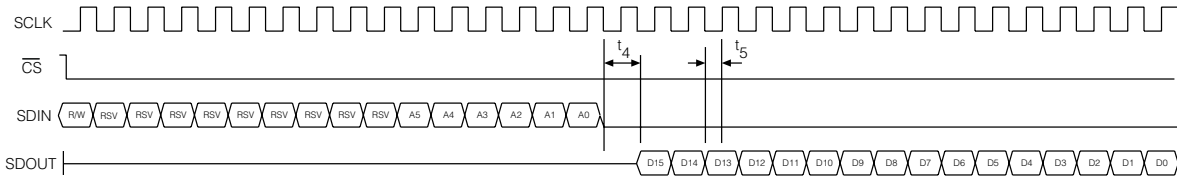


Fig. 11 Read Mode

3.1.4 Configuration and Status Register Description

The GS1532 provides status and configuration registers. These registers may be used to enable additional features of the device and/or to provide additional status information.

The GS1532 contains the following registers:

- 4 VIDEO_FORMAT registers
- 4 RASTER_STRUCTURE registers
- 1 EDH_CALCULATION_RANGE register
- 2 DATA_FORMAT registers
- 1 IOPROC_DISABLE_MASK register

All of these registers are available to the application layer via the host interface and are all individually addressable.

Where status registers contain less than the full 16 bits of information however, two or more registers may be combined at a single logical address.

3.2 JTAG TEST

When the JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port will be configured for JTAG test operation. In this mode the SCLK, SDIN, SDOUT and $\overline{\text{CS}}$ become TCK, TDI, TDO and TMS. In addition, the $\overline{\text{TRST}}$ pin become active.

Boundary scan testing using the JTAG interface will be enabled in this mode.

There are two methods in which JTAG can be used on the GS1532:

(1) as a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly, or

(2) under control of the host for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ signal. This is shown in Figure 12.

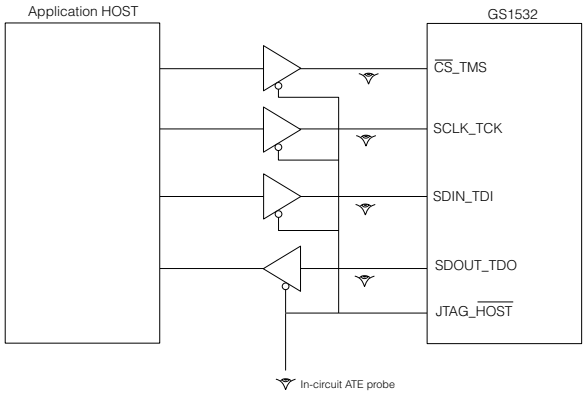


Fig. 12 In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the host may still control the JTAG/$\overline{\text{HOST}}$ signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 13.

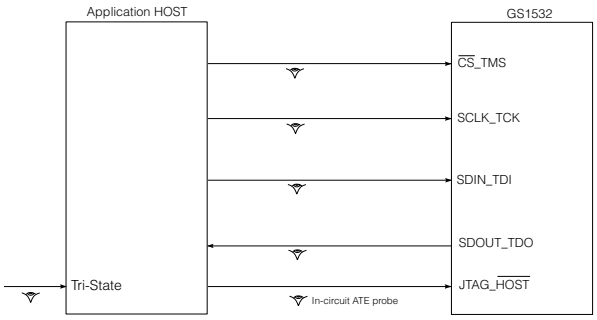


Fig. 13 System JTAG

3.3 PARALLEL DATA INPUTS DIN[19:10] AND DIN[9:0]

Data outputs leave the device on the rising edge of PCLK as shown in Figure 14.

The data may be scrambled or unscrambled, framed or unframed and may be presented in 20-bit or 10-bit format. The output data format is defined by the setting of external pins 20bit/$\overline{\text{10bit}}$, $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI.

Table 8 lists the output signal formats according to the external selection pins for the GS1560. It should be noted that DVB-ASI output will always be in 10-bit format, regardless of the setting of the 20bit/$\overline{\text{10bit}}$ pin.

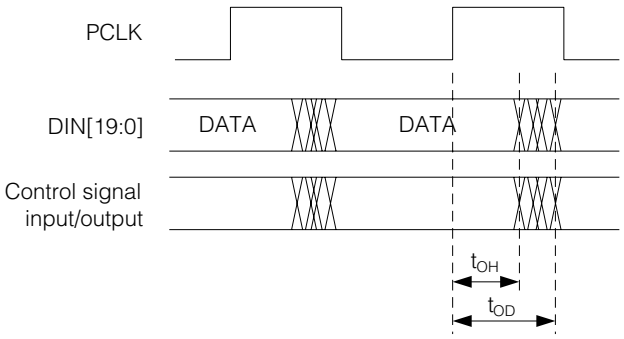


Fig. 14 PCLK to Data and Control Signal Input Timing

Table 8: Input Data Format Selections

OUTPUT Data Format	Pin Settings				DIN[9:0]	DIN[19:10]
	20bit/$\overline{\text{10bit}}$	SD/$\overline{\text{HD}}$	$\overline{\text{SMPTE\_BYPASS}}$	DVB_ASI		
20-bit demultiplexed HD format	HIGH	LOW	HIGH	Don't Care	Chroma	Luma
20-bit data Input HD format	HIGH	LOW	LOW	Don't Care	DATA	DATA
20-bit demultiplexed SD format	HIGH	HIGH	HIGH	LOW	Chroma	Luma
20-bit data input SD format	HIGH	HIGH	LOW	LOW	DATA	DATA
20-bit ASI input SD format	HIGH	HIGH	LOW	HIGH	High Impedance	DVB-ASI data
10-bit multiplexed HD format	LOW	LOW	HIGH	Don't Care	High Impedance	Luma/Chroma
10-bit data input HD format	LOW	LOW	LOW	Don't Care	High Impedance	DATA
10-bit multiplexed SD format	LOW	HIGH	HIGH	LOW	High Impedance	Luma/Chroma
10-bit data input SD format	LOW	HIGH	LOW	LOW	High Impedance	DATA
10-bit ASI input SD format	LOW	HIGH	LOW	HIGH	High Impedance	DVB-ASI data

For all data input format cases DIN[19] represents the most significant bit of the input data.

3.3.1 Input Data Format in SMPTE Mode

When the device is operating in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH), data is presented to the input bus in either multiplexed or demultiplexed form depending on the setting of the 20bit/$\overline{\text{10bit}}$ pin.

When operating in 20-bit mode (20bit/$\overline{\text{10bit}}$ = HIGH), the input data format will be (word aligned), demultiplexed Luma and Chroma data.

When operating in 10-bit mode (20bit/$\overline{10bit}$ = LOW), the input data format will be (word aligned), multiplexed Luma and Chroma data. In this mode, the data will be presented on the DIN[19:10] pins, with DIN[9:0] being high impedance.

3.3.2 Input Data Format in Data Through Mode

Data through mode is enabled when both the $\overline{SMPTE\_BYPASS}$ and DVB_ASI pins are LOW.

In this mode data at the input bus is passed to the serial output without any coding, scrambling or word-alignment taking place. The input data width is controlled by the setting of the 20bit/$\overline{10bit}$ pin as shown in Table 8.

3.3.3 Input Data Format in DVB-ASI Mode

The DVB-ASI mode of the GS1532 will be enabled when the SMPTE_BYPASS pin is LOW, the DVB_ASI pin is HIGH, and the SD/$\overline{HD}$ pin is HIGH.

In this mode, all SMPTE processing features are disabled, and the device will accept 8-bit transport stream data on the DIN[19:10] port, which will be configured as follows:

DIN19 = INSSYNCIN

DIN18 = KIN

DIN17~10 = HIN ~ AIN where AIN is the least significant bit of the transport stream data.

DIN[9:0] will be set as high impedance in this mode.

3.3.4 PCLK Output DOUT [19:10] and DOUT [9:0]

The frequency of the PCLK input signal of the GS1532 is determined by the input data format.

Table 9 lists the input signal formats according to the external selection pins for the GS1532.

Table 9: PCLK Output Rates

OUTPUT DATA FORMAT	PIN SETTINGS				PCLK RATE
	20bit/$\overline{10bit}$	SD/$\overline{HD}$	$\overline{SMPTE\_BYPASS}$	DVB_ASI	
20-bit demultiplexed HD format	HIGH	LOW	HIGH	Don't Care	74.25 or 74.25/1.001MHz
20-bit data input HD format	HIGH	LOW	LOW	Don't Care	74.25 or 74.25/1.001MHz
20-bit demultiplexed SD format	HIGH	HIGH	HIGH	LOW	13.5MHz
20-bit data input SD format	HIGH	HIGH	LOW	LOW	13.5MHz
20-bit ASI input SD format	HIGH	HIGH	LOW	HIGH	27MHz
10-bit multiplexed HD format	LOW	LOW	HIGH	Don't Care	148.5 or 148.5/1.001MHz
10-bit data input HD format	LOW	LOW	LOW	Don't Care	148.5 or 148.5/1.001MHz
10-bit multiplexed SD format	LOW	HIGH	HIGH	LOW	27MHz
10-bit data input SD format	LOW	HIGH	LOW	LOW	27MHz
10-bit ASI input SD format	LOW	HIGH	LOW	HIGH	27MHz

3.4 FLYWHEEL

The GS1532 has an internal flywheel, which may be used to generate internal timing.

The flywheel will be locked to the externally provided H:V:F signals (DETECT_TRS = LOW), or from embedded TRS signals in the input data stream (DETECT_TRS = HIGH).

TRS signals from the Luma channel only will be used to lock the flywheel when DETECT_TRS is HIGH and the device is operating in HD mode (SD/$\overline{HD}$ = LOW).

When operating in SD mode, TRS code words will be extracted from the multiplexed Y and Cr/Cb data.

NOTE: Both 8-bit and 10-bit TRS code words will be identified by the device.

The flywheel is only active in SMPTE mode of operation ($\overline{SMPTE\_BYPASS}$ = HIGH).

The main function of the flywheel is to 'learn' the required video standard by storing parameters about the line and field/frame rate. From this information internal timing and control signals may be generated.

The flywheel consists of a number of counters and comparators operating at video pixel and video line rates. These counters maintain information about the total line length, active line length, total number of lines per field/frame and total active lines per field/frame for the received video standard.

The flywheel 'learns' the video standard by timing the horizontal and vertical reference information contained in the TRS ID's of the received video data. It will there for take one video frame to obtain full synchronization of the flywheel to the received video standard.

Once synchronization has been achieved, the flywheel will continue to monitor the received TRS timing or the supplied H:V:F timing information to maintain synchronization.

3.5 H:V:F TIMING SIGNAL GENERATION

As discussed in Section 3.5, the internal flywheel may be locked to supplied H:V:F signals when DETECT_TRS = LOW.

Horizontal blanking period / active line (H), Vertical blanking period (V), and Field odd / even (F) timing are presented to the device on the H:V:F input pins.

Using the host interface register H_CONFIG, the H signal input timing can be selected as one of the following:

1) Active line blanking (H_CONFIG = LOW) - the H input should be HIGH for all the horizontal blanking period, including the EAV and SAV TRS words.

2) TRS based blanking (H_CONFIG = HIGH) - the H input should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the TRS words. The timing of these signals is shown in Figure 15.

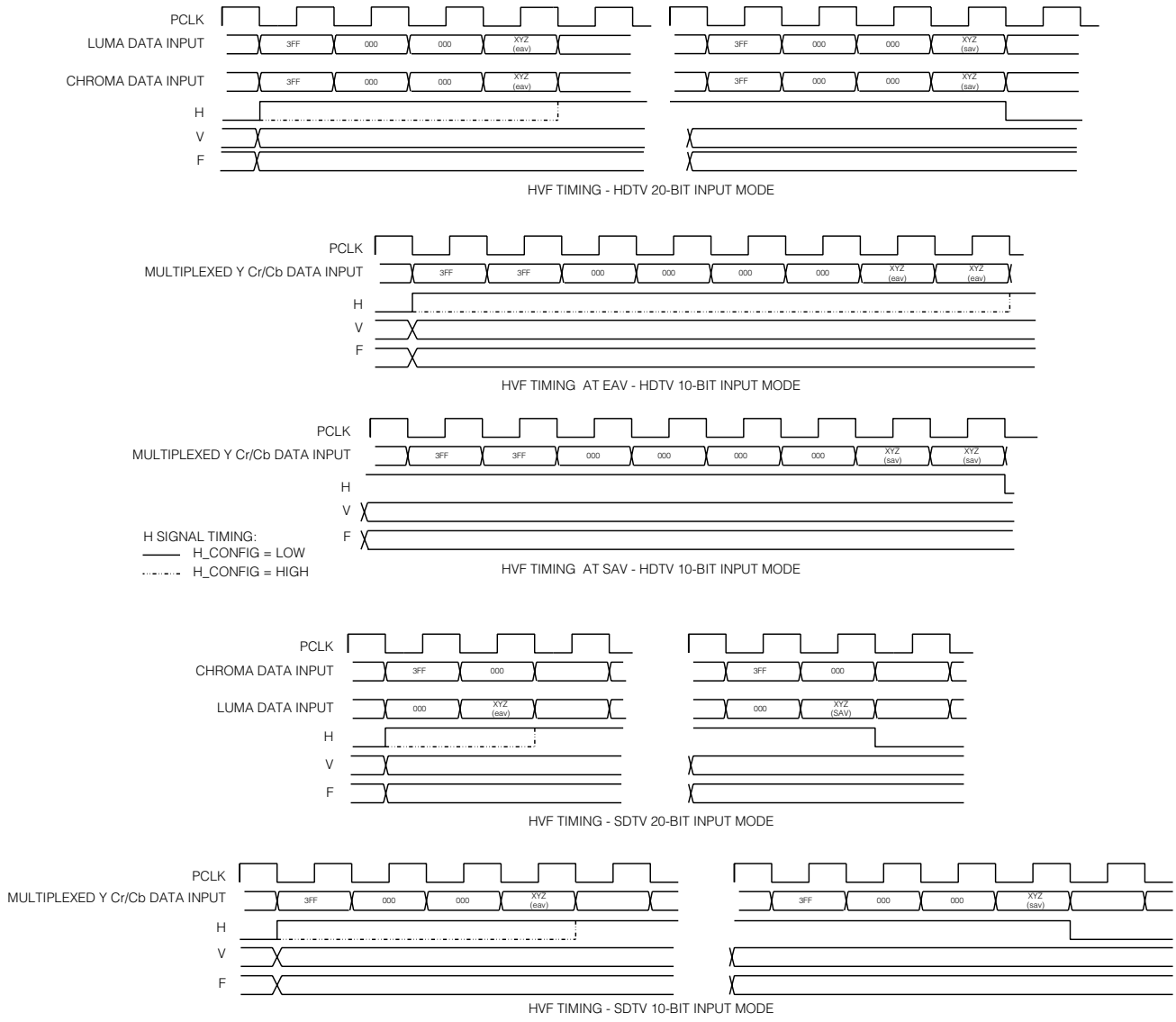
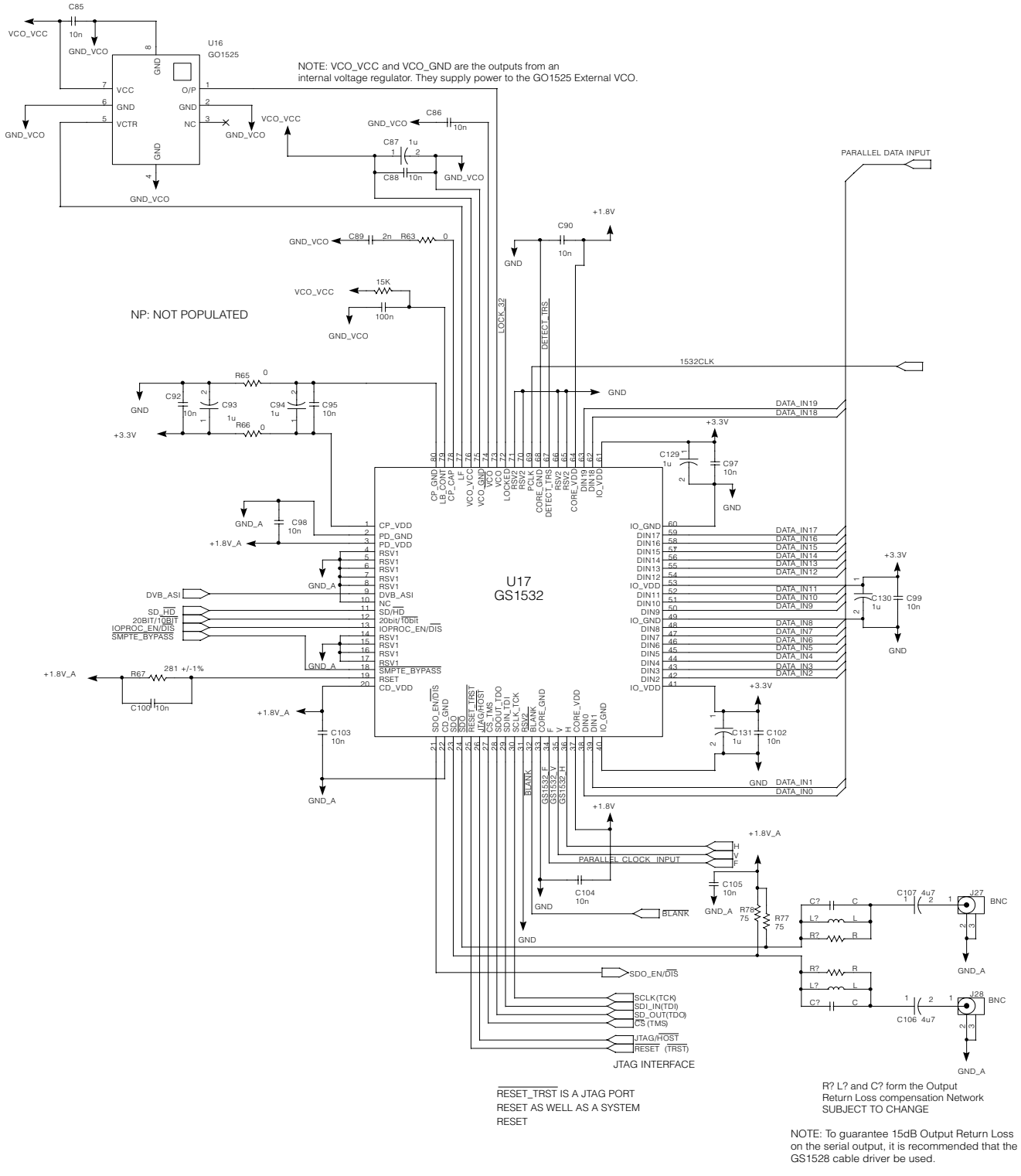


Fig. 15 HVF Output Timing

4. APPLICATION REFERENCE DESIGN

4.1 TYPICAL APPLICATION CIRCUIT



5. REFERENCES & RELEVANT STANDARDS

Compliant with SMPTE 292M and SMPTE 259M-C.

6. PACKAGE & ORDERING INFORMATION

6.1 PACKAGE DIMENSIONS

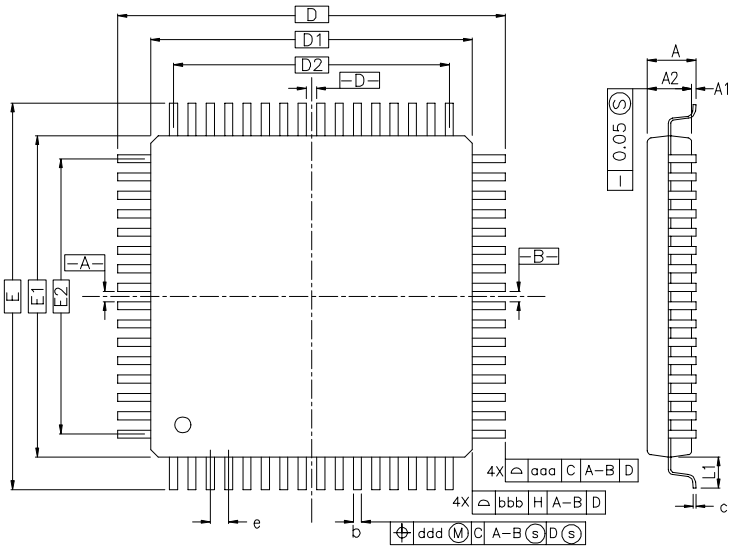
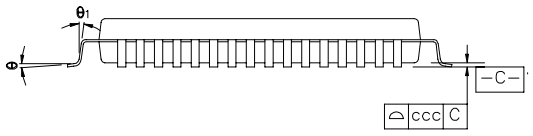


Table X

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

CONTROL DIMENSIONS ARE IN MILLIMETERS.



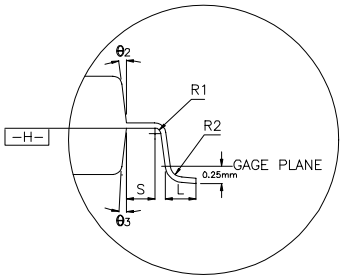


Table Y

SYMBOL	80L					
	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
b	0.22	0.30	0.38	0.009	0.012	0.015
e	0.65 BSC			0.026 BSC		
D2	12.35			0.486		
E2	12.35			0.486		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.13			0.005		

NOTES:
Diagram shown is representative only. Table X is fixed for all pin sizes, and Table Y is specific to the 80-pin package.

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

6.2 ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE
TBD	80-pin LQFP	0°C to 70°C

7. REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
A	119528	December 2001	New Document.
B	120387	February 2002	Updated pin designation information. Remove all BGA package references. Package drawing added.
C	121914	April 2002	Update to document tables and information. Inserted HOST Interface Register Maps and Descriptions and GSPI data. Document title changed.
D	123775	June 2002	Added PCLK & Input Data Format Tables, Flywheel description and H:V:F timing charts. Corrected several symbols in the AC Electrical Characteristic Table.
0	125508	August 2002	Update document to PDS and reformat. Changed AC/DC parameters from design goals to preliminary characterization/test results. Correct descriptions of pins 9, 13, 21, 23/24, 72, and 77. New reflow profile. Edit front page device description.

DOCUMENT IDENTIFICATION
PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change without notice.

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GENNUM CORPORATION

MAILING ADDRESS:
P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

SHIPPING ADDRESS:
970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5

GENNUM JAPAN CORPORATION
C-101, Miyamae Village, 2-10-42 Miyamae, Suginami-ku
Tokyo 168-0081, Japan
Tel. +81 (03) 3334-7700 Fax. +81 (03) 3247-8839

GENNUM UK LIMITED
25 Long Garden Walk, Farnham, Surrey, England GU9 7HX
Tel. +44 (0)1252 747 000 Fax +44 (0)1252 726 523