HD-LINX™ GS1508
HDTV Cable Driver

DATA SHEET

FEATURES

- **SMPTE 292M compliant**
- **dual cable driving outputs optimized for driving data up to 1.485Gb/s**
- **±7% tolerance output**
- **>17dB output return loss**
- **minimum external components**
- **seamless interface with the HD-LINX™ family of products**
- **low power**
- **standard packaging**

APPLICATIONS

1.485Gb/s HDTV Serial Digital Receiver Interfaces for: Routers, Distribution Amplifiers, Switchers, and other transmitting equipment.

DESCRIPTION

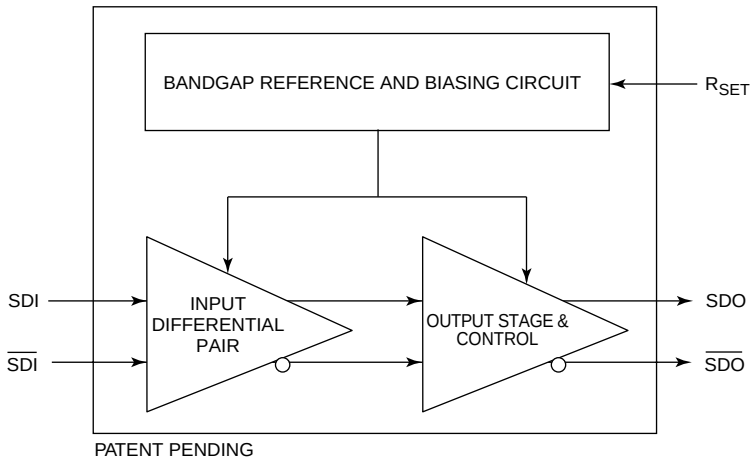
The GS1508 is a first generation very high speed bipolar integrated circuit designed to drive two 75Ω co-axial cables. The GS1508 is a SMPTE 292M compliant cable driver that directly interfaces with other Gennum HDTV devices and can also be used as a general purpose high speed cable driver.

The GS1508 features two complementary outputs whose amplitude is controlled within a precise ±7% variation. The output amplitude can be varied by adjusting the R_{SET} resistor value.

The serial inputs can be AC coupled. The GS1508 is a low power device that does not require external pull down resistors. The GS1508 is packaged in an 8 pin SOIC and operates from a single 5V power supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS1508-CKA	8 pin SOIC	0°C to 70°C
GS1508-CTA	8 pin Tape and Reel	0°C to 70°C



PATENT PENDING

BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise indicated

PARAMETER	VALUE
Supply Voltage	5.5V
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Storage Temperature	-65°C to 150°C
Power Dissipation	300mW
Lead Temperature (soldering, 10 sec)	260°C
Input ESD Voltage	2000V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 0°C to 70°C unless otherwise shown.
Specifications assume 800mV output amplitude level settings into end terminated 75Ω transmission lines. Data Rate = 1485Mb/s unless otherwise shown.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Supply Voltage		V_{CC}	4.75	5.00	5.25	V		1
System Power Consumption	Driving two 75Ω cables	P_D	-	215	265	mW		1
Supply Current		I_S	-	43	54	mA		1
Common Mode Input Voltage Range		$V_{CM,IN}$	2.5+($V_{DIFF/2}$)	-	V_{CC}-($V_{DIFF/2}$)	V		2
Common Mode Output Voltage Range		$V_{CM,OUT}$	-	V_{CC}-V_{OUT}	-	V		2

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 0°C to 70°C unless otherwise shown.
Specifications assume 800mV output amplitude levels into end terminated 75Ω transmission lines. Data Rate = 1485Mb/s unless otherwise shown.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Serial Digital Rate			DC	1485	-	Mb/s		1
Additive Jitter	1485Mb/s		-	5	-	ps_{RMS}	1	3
Differential Input		V_{DIFF}	150	-	800	mV	diff p-p	2
Differential Output		V_{OUT}	750	800	850	mV	p-p	1
Output Rise/Fall Times	(20% - 80%)	t_R, t_F	-	120	250	ps	2	1
Mismatch in Output Rise/Fall Times			-	15	30	ps		4
Overshoot			-	1	8	%		4
Duty Cycle Distortion			-	15	30	ps		1
Output Return Loss	5MHz to 1485MHz		-	17	-	dB	2	4

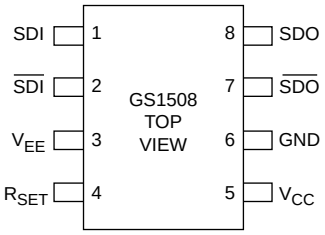
NOTES:

1. RMS additive jitter measured using Pseudo Random bit sequence (2^{23} - 1).
2. Measured with Gennum Evaluation Board (EB1508).

TEST LEVELS:

1. 100% tested at 25°C.
2. Guaranteed by design.
3. Correlated Value.
4. Tested with EB1508

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1, 2	SDI, $\overline{SDI}$	I	Serial data inputs (non-inverting and inverting).
3	V_{EE}	P	Most negative supply voltage.
4	R_{SET}	I	Output amplitude control resistor.
5	V_{CC}	P	Most positive supply voltage.
6	GND	P	Not connected internally. Connect to Ground. Used for isolation.
7, 8	$\overline{SDO}$, SDO	O	Serial data outputs (non-inverting and inverting).

INPUT / OUTPUT CIRCUITS

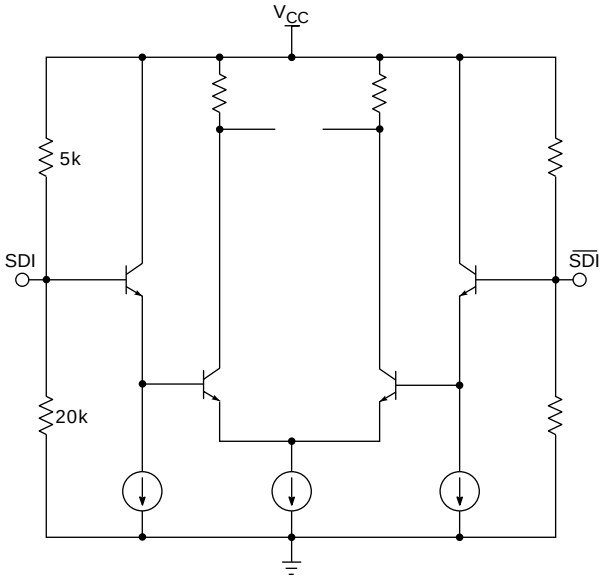


Fig. 1 (Pins 1 and 2)

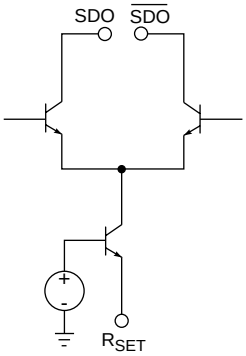


Fig. 2 (Pins 7 and 8)

DETAILED DESCRIPTION

INPUT INTERFACING

SDI/$\overline{\text{SDI}}$ are high impedance differential inputs. (*See Figure 1 for equivalent input circuit*).

Several conditions must be observed when interfacing to these inputs:

1. The differential input signal amplitude must be between 150 and 800mVpp.
2. The common mode voltage range must be as specified in the DC Characteristics table. For a 400mV input from the GS1504 HD cable equalizer, this corresponds to a common mode voltage range of between 2.7 and 4.8 volts.
3. For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GS1508 inputs are self biased, allowing for simple AC coupling to the device. For serial digital HDTV, a minimum capacitor value of 4.7µF should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

OUTPUT INTERFACING

The GS1508 outputs are current mode, and will drive 800mV into a 75 ohm load. These outputs are protected from accidental static damage with internal static protection diodes.

The SMPTE 292M standard requires that the output of a cable driver have a source impedance of 75Ω and a return loss of at least 15dB between 5Mhz and 1.485GHz.

In order for an HD SDI output circuit using the GS1508 to meet this specification, the output circuit shown in the Typical Application Circuit is recommended.

The values of L_{COMP} and C_{COMP} will vary depending on PCB layout, but typical values are 12nH and 0.5pF respectively. The small value of C_{COMP} can be easily swamped by parasitic PCB capacitance, so it is recommended that the ground plane be removed under the GS1508 output circuitry (*see the Application Information section in this data sheet for further details*). A 4.7µF capacitor is used for AC coupling the output of the GS1508. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring.

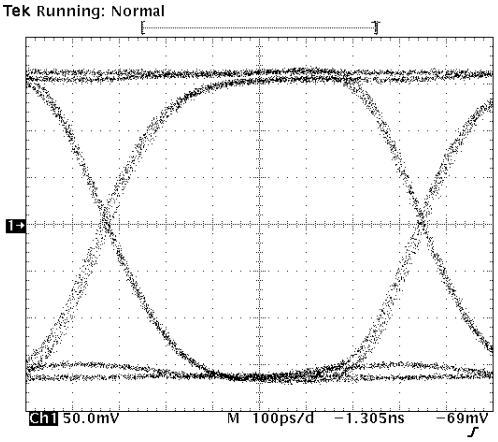


Fig. 3 Output Optimized for Waveform Symmetry
L=8.2nH, R=75 (Typical ORL=13.5dB)

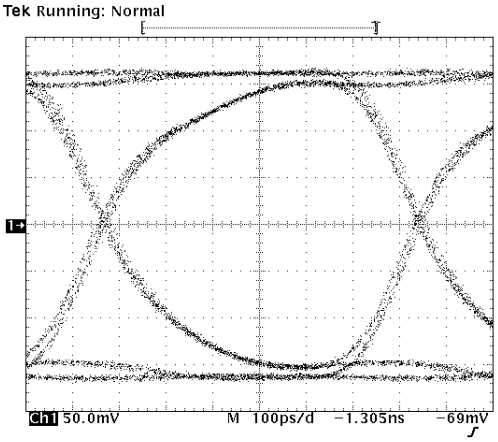


Fig. 4 Output Optimized for Return Loss
L=12nH, C=0.5pF, R=75 (Typical ORL=18dB)

Figures 3 and 4 show the eye diagram of the GS1508 output for two different output compensation conditions.

Figure 4 shows the GS1508 output optimized for wideband return loss of 18dB. Figure 3 shows the GS1508 output optimized for output waveform symmetry. In this case the output may not exhibit a return loss of 15dB.

When measuring return loss at the GS1508 output it is necessary to take the measurement for both a logic high and a logic low output condition. This is because the output protection diodes act as a varactor (voltage controlled capacitor) as shown in Figure 5.

Consequently, the output capacitance of the GS1508 is dependent on the logic state of the output.

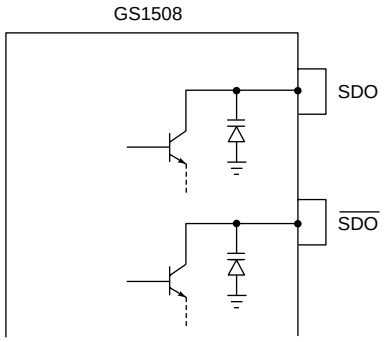


Fig. 5 Static Protection Diodes

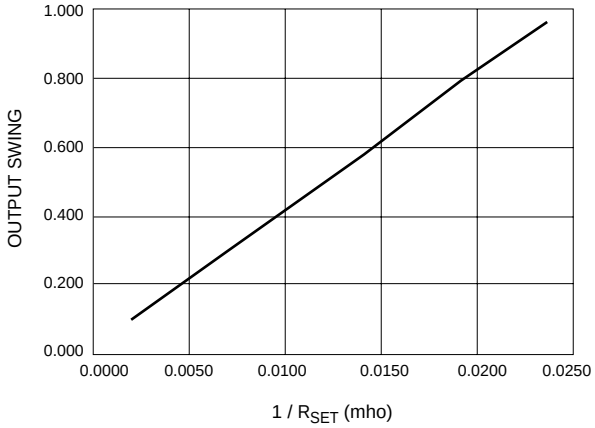


Fig. 6 GS1508 Output Amplitude vs. $1/R_{SET}$

OUTPUT RETURN LOSS MEASUREMENT

To perform a practical return loss measurement, it is necessary to force the GS1508 output to a DC high or low condition. The actual measured return loss will be based on the outputs being static at V_{CC} or V_{CC}-1.6V. Under normal operating conditions the outputs of the GS1508 swing between V_{CC}-0.4V and V_{CC}-1.2V, so the measured value of return loss will not represent the actual operating return loss.

A simple method of calculating the values of actual operating return loss is to interpolate the two return loss measurements. In this way, the values of return loss are estimated at V_{CC}-0.4V and V_{CC}-1.2V based on the measurements at V_{CC} and V_{CC}-1.6V.

The two values of return loss (high and low) will typically differ by several decibels. If the measured return loss is R_H for logic high and R_L for logic low, then the two values can be interpolated as follows:

$$R_{IH} = R_H - (R_H - R_L)/4 \text{ and}$$

$$R_{IL} = R_L + (R_H - R_L)/4$$

where R_{IH} is the interpolated logic high value and R_{IL} is the interpolated logic low value.

For example, if R_H = -18dB and R_L = -14dB, then the interpolated values are R_{IH} = -17dB and R_{IL} = -15dB.

OUTPUT AMPLITUDE ADJUSTMENT

The output amplitude of the GS1508 can be adjusted by changing the value of the R_{SET} resistor as shown in Figure 6 and Table 1. For an 800mV_{p-p} output with a nominal ±7% tolerance, a value of 53.6% is required. A ±1% SMT resistor should be used.

The R_{SET} resistor is part of the high speed output circuit of the GS1508. The resistor should be placed as close as possible to the R_{SET} pin. In addition, PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

TABLE 1: R_{SET} vs V_{OUT}

R_{SET} R	$1/R_{SET}$	OUTPUT SWING
500.0	0.0020	0.095
150.0	0.0067	0.298
75.0	0.0133	0.575
53.6	0.0187	0.785
43.2	0.0231	0.937

NOTE: For reliable operation of the GS1508 over the full temperature range, do not use an R_{SET} value below 49.9Ω.

TYPICAL APPLICATION CIRCUIT

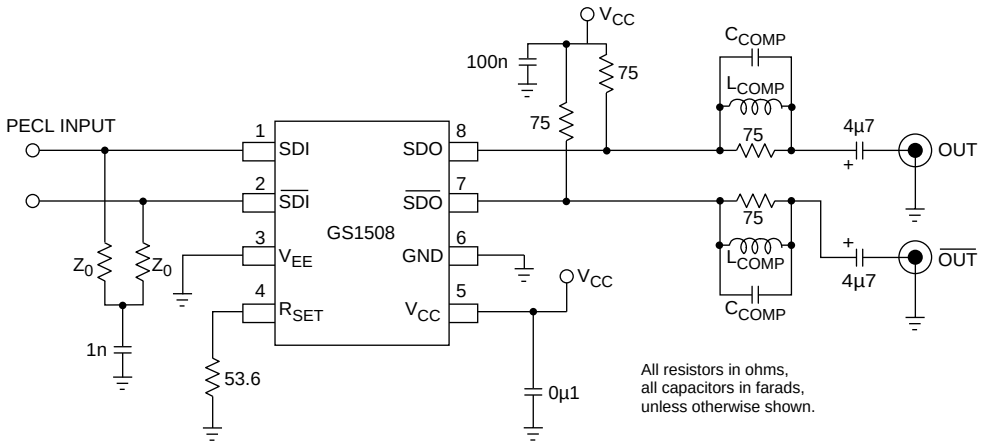


TABLE 2: Typical Application Circuit Component Values

COMPONENT	VALUE	COMMENT
R_{SET}	53.6	For 800mV Output
Z_0	50Ω	For 50Ω PCB trace impedance
L_{COMP}	12nH	Typical value. Component value will vary depending on PCB layout.
C_{COMP}	0.5pF	Typical value. Component value will vary depending on PCB layout.

APPLICATION INFORMATION

PCB LAYOUT

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. Figures 8 through 11 show the artwork for a four layer printed circuit evaluation board for the GS1508. The schematic is shown in Figure 7. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance

The PCB ground plane is removed under the GS1508 output components to minimize parasitic capacitance.

The PCB ground plane is removed under the GS1508 R_{SET} pin and resistor to minimize parasitic capacitance

Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via High speed traces are curved to minimize impedance changes due to change of PCB trace width.

GS1508 EVALUATION BOARD

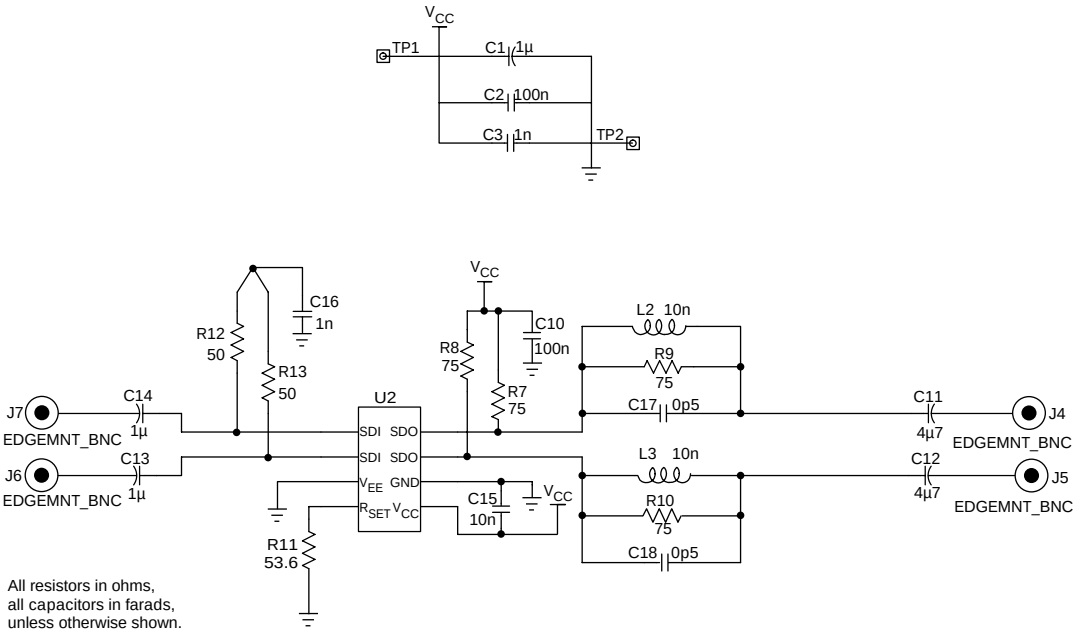


Fig. 7 Schematic Diagram for the GS1508 Evaluation Board

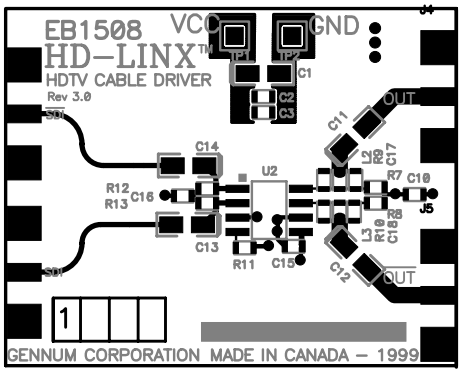


Fig. 8 Top Layer of EB1508 PCB Layout

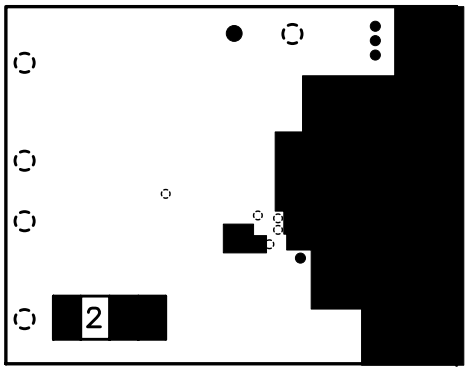


Fig. 10 Ground Layer of EB1508 PCB Layout

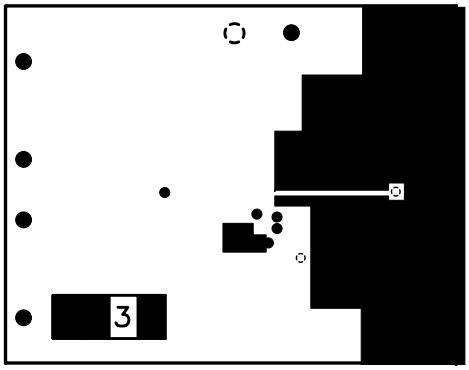


Fig. 9 Power Layer of EB1508 PCB Layout

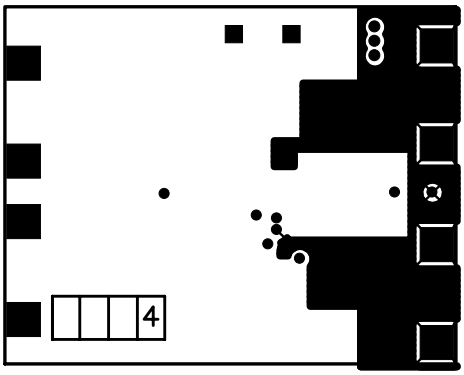
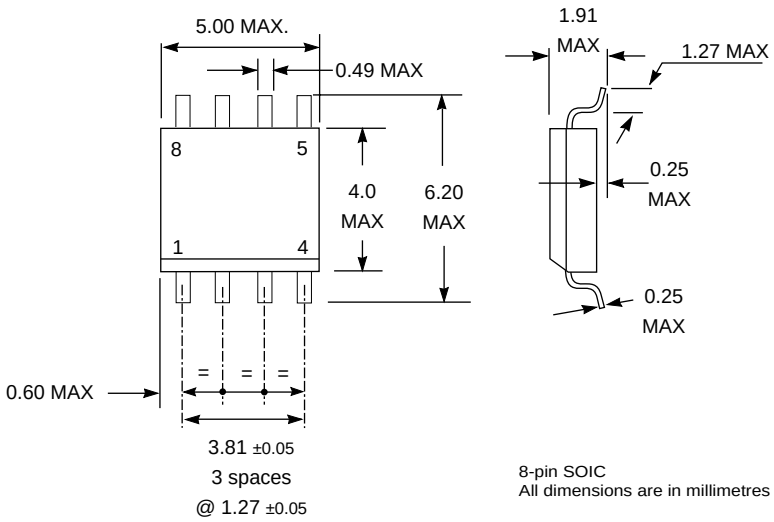


Fig. 11 Bottom Layer of EB1508 PCB Layout

PACKAGE DIMENSIONS



8-pin SOIC
All dimensions are in millimetres

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

Document type changed to data sheet.

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