# *HD-LINX*™ GS1500
# HDTV Serial Digital Deformatter with ANC FIFOs

DATA SHEET

## KEY FEATURES

- **SMPTE 292M compliant**
- **standards detection/indication for SMPTE 292M levels A/B,C,D/E,F,G/H,I,J/K,L/M**
- **NRZI decoding and SMPTE descrambling with BYPASS option**
- **line CRC calculation, comparison**
- **selectable line based CRC re-insertion**
- **H, V, F timing reference signal (TRS) extraction**
- **selectable flywheel for noise immune H, V, F extraction**
- **selectable automatic switch line handling**
- **selectable TRS and line number re-insertion**
- **selectable active picture illegal code re-mapping**
- **ANC data position indication**
- **ANC data extraction via internal FIFOs (1024 bytes on Y and C channels)**
- **configurable FIFO LOAD pulse**
- **20 bit 3.3V CMOS input data bus**
- **optimized input interface to GS1545 or GS1540**
- **single +3.3V power supply**
- **5V tolerant I/O**

## APPLICATIONS

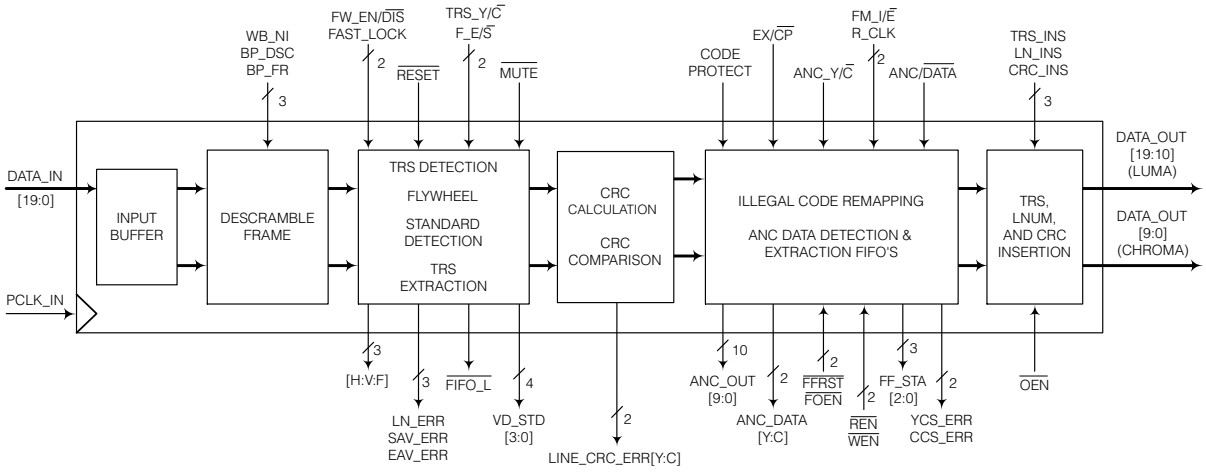
- SMPTE 292M Serial Digital Interfaces

## DESCRIPTION

When interfaced to the Gennum GS1545 HDTV Equalizing Receiver or GS1540 Non-Equalizing Receiver, the GS1500 performs the final conversion to word aligned data. The device performs NRZI decoding and de-scrambling as per SMPTE 292M and word-aligns to the incoming data stream. Line based CRCs are calculated on the incoming data stream and are compared against the CRCs embedded within the data stream.

HVF timing information is extracted from the data stream. A selectable internal HVF flywheel provides superior noise immunity against TRS signal errors. The device also detects and indicates the input video signal standard.

The GS1500 can detect and re-map illegal code words contained within the active portion of the video signal. The positions of the embedded ANC data are indicated and the ANC data may be extracted and accessed by the user through an internal FIFO interface. Prior to exiting the device, TRS, Line Numbers and CRCs based on internal calculations may be re-inserted into the data stream.




GS1500 FUNCTIONAL BLOCK DIAGRAM



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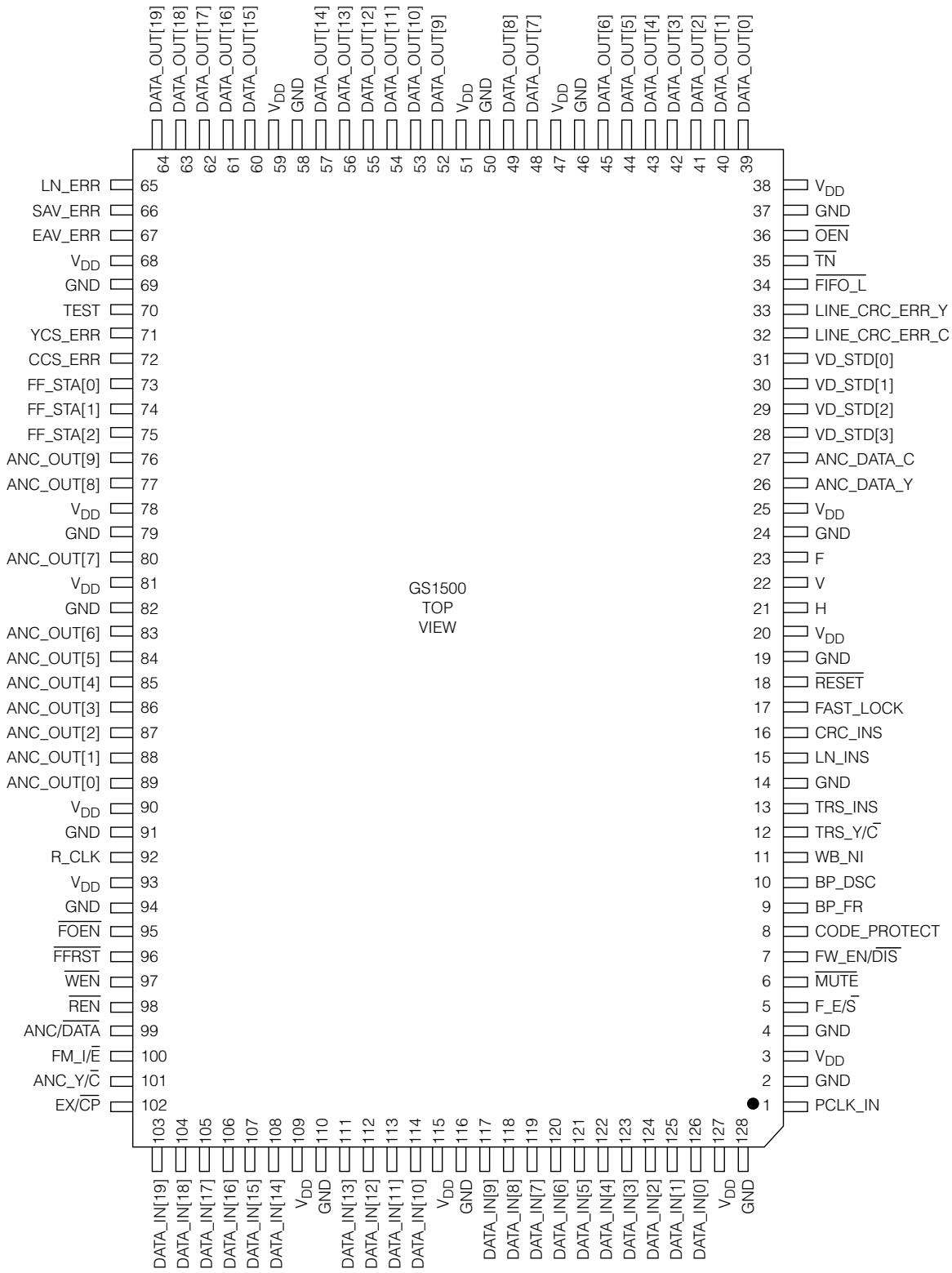
# 1. PIN OUT

## 1.1 PIN ASSIGNMENT



### 1.2 PIN DESCRIPTIONS

| PIN NUMBER | NAME | TIMING | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | PCLK_IN | Synchronous wrt PCLK_IN | Input | **Input Clock.** The device uses PCLK_IN for clocking the input data stream into DATA_IN[19:0]. This clock is generated by the GS1545 or GS1540. |
| 2, 4, 14, 19, 24, 37, 46, 50, 58, 69, 79, 82, 91, 94, 110, 116, 128 | GND | | GND | Ground power supply connections. |
| 3, 20, 25, 38, 47, 51, 59, 68, 78, 81, 90, 93, 109, 115, 127 | $V_{DD}$ | | Power | Positive power supply connections. |
| 5 | F_E/$\overline{S}$ | Non-synchronous | Input | **Control Signal Input.** Used to control where the $\overline{FIFO\_L}$ signal is generated. When F_E/$\overline{S}$ is high, the GS1500 generates $\overline{FIFO\_L}$ signal at EAV. When F_E/$\overline{S}$ is low, the GS1500 generates $\overline{FIFO\_L}$ signal at SAV. See Fig. 4 for timing information. |
| 6 | $\overline{MUTE}$ | Synchronous wrt PCLK_IN | Input | **Control Signal Input.** Used to enable or disable blanking of the LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT[9:0]). When $\overline{MUTE}$ is low, the device sets the accompanying LUMA and CHROMA data to their appropriate blanking levels. When $\overline{MUTE}$ is high, the LUMA and CHROMA data streams pass through this stage of the device unaltered. |
| 7 | FW_EN/$\overline{DIS}$ | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable the internal flywheel. When FW_EN/$\overline{DIS}$ is high, the internal flywheel is enabled. When FW_EN/$\overline{DIS}$ is low, the internal fly-wheel is disabled. |
| 8 | CODE_PROTECT | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable re-mapping of out-of -range words contained in the active portion of the video signal. When this signal is high, the device re-maps out-of-range words contained within the active portion of the video signal into CCIR-601 compliant words. Values between 000-003 are re-mapped to 004. Values between 3FC and 3FF are re-mapped to 3FB. When this signal is low, out-of-range words in the active video region pass through the device unaltered. |
| 9 | BP_FR | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable word boundary framing. When BP_FR is low, internal framing is enabled. When BP_FR is high, internal framing is bypassed. |
| 10 | BP_DSC | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable the SMPTE 292M descrambler. When BP_DSC is low, the internal SMPTE 292M de-scrambler is enabled. When BP_DSC is high, the internal SMPTE 292M de-scrambler is bypassed. |
| 11 | WB_NI | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable noise immune operation of the word boundary framer. When WB_NI is high, noise-immune word boundary alignment is enabled. The device switches to a new word boundary only when it has detected two consecutive identical new TRS positions. When WB_NI is low, the device re-aligns the word boundary position at every instance of a TRS. |
| 12 | TRS_Y/$\overline{C}$ | Non-synchronous | Input | **Control Signal Input.** Used to control whether LUMA or CHROMA TRS ID's are detected and used. When TRS_Y/$\overline{C}$ is high, the device detects and uses TRS signals embedded in the LUMA channel. When TRS_Y/$\overline{C}$ is low, the device detects and uses TRS signals embedded in the CHROMA channel. |

### 1.2 PIN DESCRIPTIONS (Continued)

| PIN NUMBER | NAME | TIMING | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 13 | TRS_INS | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable re-insertion of the TRS into the data stream. When TRS_INS is high, the device re-inserts TRS into the incoming data stream based on the internal calculation. The original TRS packets are set to the blanking levels. If the flywheel is enabled, TRS calculated by the flywheel is used for insertion. When TRS_INS is low, the device will not re-insert TRS even if errors in TRS signals are detected. |
| 15 | LN_INS | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable re-insertion of the line number into the data stream. When LN_INS is high, the device re-inserts the line number into the incoming data stream based on the internal calculation. The original line number packets are set to the blanking levels. If the flywheel is enabled, the line number calculated by the flywheel is used for insertion. When LN_INS is low, the device will not re-insert the line number. |
| 16 | CRC_INS | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable re-insertion of the CRC into the data stream. When CRC_INS is high, the device is enabled to re-insert line CRCs based on the internal calculation. When CRC_INS is low, the device will not re-insert the CRCs. |
| 17 | FAST_LOCK | Synchronous wrt PCLK_IN | Input | **Control Signal Input.** Used to control the flywheel synchronization when a switch line occurs. When a low to high transition occurs on the FAST_LOCK signal, the internal flywheel will immediately re-synchronize to the next valid EAV or SAV TRS in the incoming data stream. See Fig. 5 for timing information. |
| 18 | $\overline{\text{RESET}}$ | Non-synchronous | Input | **Control Signal Input.** Used to reset the system state registers to their default 720p parameters. When $\overline{\text{RESET}}$ is high, the fly wheel, TRS Detection, and ANC Detection operate normally. When $\overline{\text{RESET}}$ is low, the flywheel, TRS Detection, and ANC Detection are reset to the 720p parameters after a rising edge on PCLK_IN. The read and write counters are not affected. |
| 21 | H | Synchronous wrt PCLK_IN | Output | **Control Signal Output.** This signal indicates the Horizontal blanking period of the video signal. Refer to Fig. 2 for timing information of H relative to DATA_OUT[19:10] and DATA_OUT[9:0], LUMA and CHROMA respectively. |
| 22 | V | Synchronous wrt PCLK_IN | Output | **Control Signal Output.** This signal indicates the Vertical blanking period of the video signal. Refer to Fig. 2 for timing information of V relative to DATA_OUT[19:10] and DATA_OUT[9:0], LUMA and CHROMA respectively. |
| 23 | F | Synchronous wrt PCLK_IN | Output | **Control Signal Output.** This signal indicates the ODD/EVEN field of the video signal. Refer to Fig. 2 for timing information of F relative to DATA_OUT[19:10] and DATA_OUT[9:0], LUMA and CHROMA respectively. When locked and the input signal is of a progressive scan nature, F stays low at all times. |
| 26 | ANC_DATA_Y | Synchronous wrt PCLK_IN | Output | **Control Signal Output.** This signal indicates the position of the embedded ANC data in the outgoing LUMA (DATA_OUT [19:10]) data stream. ANC_DATA_Y goes high for the entire time that an ANC_DATA packet is present in the LUMA (DATA_OUT[19:10]) data stream whether it be in the active video area or the ANC area. Refer to Fig. 17 for timing of ANC_DATA_Y relative to LUMA (DATA_OUT[19:10]). During detection of ANC data, any errors in the data count (DC) packet will consequently cause errors in the duration of the flags. Bit errors in an ANC header will prevent the packet from being detected. |

### 1.2 PIN DESCRIPTIONS (Continued)

| PIN NUMBER | NAME | TIMING | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 27 | ANC_DATA_C | Synchronous wrt PCLK_IN | Output | **Control Signal Output.** This signal indicates the position of the embedded ANC data in the outgoing CHROMA (DATA_OUT[9:0]) data stream. ANC_DATA_C goes high for the entire time that an ANC_DATA packet is present in the CHROMA (DATA_OUT[9:0]) data stream whether it be in the active video area or the HANC area. Refer to Fig. 17 for timing of ANC_DATA_C relative to CHROMA (DATA_OUT[9:0]). During detection of ANC data, any errors in the data count (DC) packet will consequently cause errors in the duration of the flags. Bit errors in an ANC header will prevent the packet from being detected. |
| 28, 29, 30, 31 | VD_STD[3:0] | Synchronous wrt PCLK_IN | Output | **Control Signal Output.** VD_STD[3:0] indicates which input video standard the device has detected. The GS1500 will indicate all of the formats in SMPTE292M (see Table 3) plus it will indicate an unknown interlace or progressive scan format. |
| 32 | LINE_CRC_ERR_C | Synchronous wrt PCLK_IN | Output | **Status Signal Output.** Indicates a difference in the calculated versus embedded CRC in the CHROMA channel. When LINE_CRC_ERR_C is high, it indicates that the GS1500 has detected a difference between the line based CRCs it calculates for the CHROMA channel and the line based CRCs embedded within the CHROMA channel. When LINE_CRC_ERR_C is low, the embedded and calculated CRC's match. Refer to Fig. 19 for timing information of LINE_CRC_ERR_C. |
| 33 | LINE_CRC_ERR_Y | Synchronous wrt PCLK_IN | Output | **Status Signal Output.** Indicates a difference in the calculated versus embedded CRC in the LUMA channel. When LINE_CRC_ERR_Y is high, it indicates that the GS1500 has detected a difference between the line based CRCs it calculates for the LUMA channel and the line based CRCs embedded within the LUMA channel. When LINE_CRC_ERR_Y is low, the embedded and calculated CRC's match. Refer to Fig. 19 for timing information of LINE_CRC_ERR_Y. |
| 34 | $\overline{\text{FIFO\_L}}$ | Synchronous wrt PCLK_IN | Output | **Control Signal Output.** Used to control an external FIFO(s). $\overline{\text{FIFO\_L}}$ is normally high, but is set low for the EAV or SAV word depending on the state of F_E/$\overline{\text{S}}$. Refer to Fig. 4 for timing information of $\overline{\text{FIFO\_L}}$ relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT[9:0]). |
| 35 | $\overline{\text{TN}}$ | | TEST | **Test Pin.** Used for test purposes only. This pin must be connected to $V_{DD}$ for normal operation |
| 36 | $\overline{\text{OEN}}$ | Non-synchronous | Input | **Control Signal Input.** Used to enable the DATA_OUT[19:0] output bus or set it in a high Z state. When $\overline{\text{OEN}}$ is low, the LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]) busses are enabled. When $\overline{\text{OEN}}$ is high, these busses are in a high Z state. |
| 52, 49, 48, 45, 44, 43, 42, 41, 40, 39 | DATA_OUT[9:0] (CHROMA channel) | Synchronous wrt PCLK_IN | Output | **CHROMA Output Data Bus.** DATA_OUT [9] is CHROMA_OUT[9] which is the MSB of the CHROMA output signal (pin 52). DATA_OUT [0] is CHROMA_OUT[0] which is the LSB of the CHROMA output signal (pin 39). |
| 64, 63, 62, 61, 60, 57, 56, 55, 54, 53 | DATA_OUT[19:10] (LUMA channel) | Synchronous wrt PCLK_IN | Output | **LUMA Output Data Bus.** DATA_OUT [19] is LUMA_OUT[9] which is the MSB of the LUMA output signal. (pin 64) DATA_OUT [10] is LUMA_OUT[0] which is the LSB of the LUMA output signal (pin 53). |

### 1.2 PIN DESCRIPTIONS (Continued)

| PIN NUMBER | NAME | TIMING | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 65 | LN_ERR | Synchronous wrt PCLK_IN | Output | **Status Signal Output.** Used to indicate a Line Number error or a mismatch between the embedded line number and the flywheel line number when the flywheel is enabled. When LN_ERR is high, a line number error is detected or the internal flywheel indicates mismatching line numbers. Refer to Fig. 3 for timing information of LN_ERR relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]) Since LN_ERR depends on the sequence of line numbers, a line number error will actually cause LN_ERR to go high for two lines. |
| 66 | SAV_ERR | Synchronous wrt PCLK_IN | Output | **Status Signal Output.** Indicates a TRS error or a mismatch between the embedded TRS and the flywheel TRS when the flywheel is enabled. This signal is set high when an error in the SAV TRS is detected or when the internal flywheel indicates there is a mismatching SAV TRS. Refer to Fig. 3 for timing information of SAV_ERR relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]). |
| 67 | EAV_ERR | Synchronous wrt PCLK_IN | Output | **Status Signal Output.** Indicates a TRS error or a mismatch between the embedded TRS and the flywheel TRS when the flywheel is enabled. This signal is set high when an error in the EAV TRS is detected or when the internal flywheel indicates there is a mismatching EAV TRS. Refer to Fig. 3 for timing information of EAV_ERR relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]). |
| 70 | TEST | | TEST | **Test Pin.** Used for test purposes only. This pin must be connected to GND for normal operation. |
| 71 | YCS_ERR | Synchronous wrt PCLK_IN | Output | **Status Signal Output.** Indicates a checksum error or a mismatch between the embedded checksum and the calculated checksum for the LUMA (DATA_OUT[19:10]) channel. When YCS_ERR is high, an error in the checksum is detected. Refer to Fig. 18 for timing information of YCS_ERR relative to LUMA (DATA_OUT[19:10]). |
| 72 | CCS_ERR | Synchronous wrt PCLK_IN | Output | **Status Signal Output.** Indicates a checksum error or a mismatch between the embedded checksum and the calculated checksum for the CHROMA (DATA_OUT[9:0]) channel. When CCS_ERR is high, an error in the checksum is detected. Refer to Fig. 18 for timing information of CCS_ERR relative to CHROMA (DATA_OUT [9:0]). |
| 75, 74, 73 | FF_STA[2:0] | | Output | **Control Signal Output.** FF_STA[2:0] is the FIFO status output to indicate the content level of the internal FIFOs.<br>FF_STA[2:0]=000: Error flag, FIFO is under run .<br>FF_STA[2:0]=001: FIFO is empty.<br>FF_STA[2:0]=010: FIFO is almost empty; 32 bytes filled<br>FF_STA[2:0]=011: FIFO is ready.<br>FF_STA[2:0]=100: FIFO is half full.<br>FF_STA[2:0]=101: FIFO is almost full; 992 bytes filled<br>FF_STA[2:0]=110: FIFO is full.<br>FF_STA[2:0]=111: Error flag, FIFO is over run.<br>When ANC_Y/$\overline{C}$ is high, FF_STA[2:0] indicates the status of the LUMA ANC data FIFO. When ANC_Y/$\overline{C}$ is low, FF_STA[2:0] indicates the status of the CHROMA ANC data FIFO. See Fig. 6 to Fig. 15 for timing information. |
| 76, 77, 80, 83, 84, 85, 86, 87, 88, 89 | ANC_OUT[9:0] | Synchronous wrt PCLK_IN | Output | **ANC Data Output Bus.** ANC_OUT[9] is the MSB and ANC_OUT[0] is the LSB. When ANC_Y/$\overline{C}$ is high, ANC_OUT[9:0] presents ANC data from the LUMA FIFO. When ANC_Y/$\overline{C}$ is low, ANC_OUT[9:0] presents ANC data from the CHROMA FIFO. |

### 1.2 PIN DESCRIPTIONS (Continued)

| PIN NUMBER | NAME | TIMING | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 92 | R_CLK | N/A | Input | **Input Clock Signal.** Used to read information from the internal FIFO(s). On the rising edge of R_CLK, the device will extract the next word from the internal LUMA/CHROMA channel data FIFO, depending on the status of the ANC_Y/$\overline{C}$ signal. |
| 95 | $\overline{FOEN}$ | Non-synchronous | Input | **Control Signal Input.** Used to enable or disable the internal FIFO outputs. When $\overline{FOEN}$ is low, the FIFO ANC_OUT[9:0] and FF_STA[2:0] are enabled. When $\overline{FOEN}$ is high, the FIFO ANC_OUT[9:0] and FF_STA[2:0] outputs are in a high Z state. Note that the internal read address pointers are updated independently of $\overline{FOEN}$. |
| 96 | $\overline{FFRST}$ | Synchronous wrt PCLK_IN | Input | **Control Signal Input.** $\overline{FFRST}$ is used to supply synchronous reset signals to the FIFO. When $\overline{FFRST}$ is low, the FIFO is reset and all internal read and write address pointers are set to their starting locations. |
| 97 | $\overline{WEN}$ | Synchronous wrt PCLK_IN | Input | **Control Signal Input.** Used to enable or disable extracting data into the internal FIFO. When $\overline{WEN}$ is low, extracting data into the internal FIFO is enabled. When $\overline{WEN}$ is high, extracting data into the internal FIFO is disabled. |
| 98 | $\overline{REN}$ | Synchronous wrt R_CLK | Input | **Control Signal Input.** Used to enable or disable reading data from the internal FIFO. When $\overline{REN}$ is low, reading from the internal FIFO is enabled. When $\overline{REN}$ is high, reading from the internal FIFO is disabled. |
| 99 | ANC/$\overline{DATA}$ | Non-synchronous | Input | **Control Signal Input.** Used to control copying of ANC data packets into the internal FIFOs. When ANC/$\overline{DATA}$ is high, the device extracts/copies only ANC data packets into the internal FIFO buffers. When ANC/$\overline{DATA}$ is low, the device extracts/copies all data words within the horizontal blanking period regardless of their status (i.e. ANC data or not) and places these words into the internal FIFO buffers. |
| 100 | FM_I/$\overline{E}$ | Non-synchronous | Input | **Control Signal Input.** When FM_I/$\overline{E}$ is high, the device operates in a mode where the FIFO reset and write enable signals are generated internally. In this mode, the device limits the data extraction to the HANC region of the video stream. The extracted ANC data are to be accessed during the active video period using $\overline{REN}$. When FM_I/$\overline{E}$ is low, the device operates in another mode where the FIFO reset and write enable signals are generated externally by the user and supplied to the device via the $\overline{FFRST}$ and $\overline{WEN}$ control signal inputs. |
| 101 | ANC_Y/$\overline{C}$ | Synchronous wrt PCLK_IN | Input | **Control Signal Input.** Used to control extraction of ANC data from the video data stream into the LUMA or CHROMA FIFO. When ANC_Y/$\overline{C}$ is high, data is extracted from the luma data stream into the internal LUMA FIFO. When ANC_Y/$\overline{C}$ is low, data is extracted from the chroma data stream into the internal CHROMA FIFO. |
| 102 | EX/$\overline{CP}$ | Non-synchronous | Input | **Control Signal Input.** Used to control if the ANC Data is extracted or copied into the internal FIFO buffers. When EX/$\overline{CP}$ is high, the device extracts ANC data from the incoming data stream into the internal FIFO buffers and replaces any extracted words with appropriate blanking levels. When EX/$\overline{CP}$ is low, the device makes a copy of ANC data from the incoming data stream into the internal FIFO buffers. |
| 103,104,105, 106, 107, 108, 111, 112, 113, 114, 117, 118, 119,120, 121, 122, 123, 124, 125, 126 | DATA_IN [19:0] | Synchronous wrt PCLK_IN | Input | **Input Data Bus.** DATA_IN [19] is the MSB of the signal (pin 103). DATA_IN [0] is the LSB of the signal (pin 126). This data is typically scrambled and not word aligned. |

## 2. ELECTRICAL CHARACTERISTICS

### 2.1 ABSOLUTE MAXIUMUM RATINGS

| PARAMETER | VALUE |
|---|---|
| Supply Voltage | -0.5V to +4.6V |
| Input Voltage Range (any input) | $-0.5V < V_{IN} < 5.5V$ |
| Operating Temperature Range | $0°C \le T_A \le 70°C$ |
| Storage Temperature Range | $-40°C \le T_S \le 125°C$ |
| Lead Temperature (soldering 10 seconds) | 260°C |

### 2.2 DC ELECTRICAL CHARACTERISTICS

$V_{DD}$= 0.3 to 3.6V, $T_A$= 0°C to 70°C, unless otherwise shown

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Positive Supply Voltage | $V_{DD}$ | | 3.0 | 3.3 | 3.6 | V | |
| Supply Current | $I_{DD}$ | $f$ = 74.25MHz, $T_A$ = 25°C | - | 413 | 480 | mA | |
| Input Logic LOW Voltage | $V_{IL}$ | $I_{LEAKAGE}$ < 10µA | - | - | 0.8 | V | |
| Input Logic HIGH Voltage | $V_{IH}$ | $I_{LEAKAGE}$ < 10µA | 2.1 | 3.3 | 5.0 | V | |
| Output Logic LOW Voltage | $V_{OL}$ | $V_{DD}$ = 3.0 to 3.6V, $I_{OL}$= 4mA | - | 0.3 | 0.4 | V | |
| Output Logic HIGH Voltage | $V_{OH}$ | $V_{DD}$ = 3.0 to 3.6V, $I_{OH}$= -4mA | 2.6 | - | - | V | |

### 2.3 AC ELECTRICAL CHARACTERISTICS

$V_{DD}$= 0.3 to 3.6V, $T_A$= 0°C to 70°C, unless otherwise shown

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Clock Input Frequency | $f_{HSCI}$ | | - | 74.25 | 80 | MHz | Also supports 74.25/ 1.001MHz |
| Input Data Setup Time | $t_{SU}$ | | 2.5 | - | - | ns | 50% levels |
| Input Data Hold Time | $t_{IH}$ | | 1.5 | - | - | ns | 50% levels |
| Input Clock Duty Cycle | | | 40 | - | 60 | % | |
| Output Data Hold Time | $t_{OH}$ | With 15pF load | 2.0 | - | - | ns | Note 3 |
| Output Enable Time | $t_{OEN}$ | With 15pF load | - | - | 8 | ns | |
| Output Disable Time | $t_{ODIS}$ | With 15pF load | - | - | 10 | ns | |
| Output Data Delay Time | $t_{OD}$ | With 15pF load | - | - | 10 | ns | Note 2 |
| Output Data Rise/Fall Time | $t_{ROD}/t_{FOD}$ | With 15pF load | - | - | 2.75 | ns | 20% to 80% levels |
| FIFO Input Data Setup Time | $t_{FSU}$ | | 8.0 | - | - | ns | Note 1 |
| FIFO Input Data Hold Time | $t_{FIH}$ | | 4.0 | - | - | ns | Note 1 |

NOTES:

1. The following signals need to adhere to this timing: ANC_Y/$\overline{C}$, $\overline{REN}$, $\overline{WEN}$, $\overline{FFRST}$
2. Timing of the FF_STA[2:0] outputs may be greater than specified.
3. Output timing characteristics also apply to FIFO outputs.

## 3. DETAILED DESCRIPTION

### 3.1 DATA INPUT AND OUTPUTS

Data enters and exits the device on the rising edge of PCLK_IN as shown in Figures 1 and 2. This data can be scrambled or unscrambled and framed or unframed.

### 3.2 DESCRAMBLER AND FRAMER

Both the descrambler and framer can be enabled or disabled independently to allow the input to remain scrambled or unscrambled. If the data is unscrambled, it can be word aligned (framed) or pass through unaltered.

### 3.3 STANDARDS INDICATION

VD_STD[3:0] indicates the standard that the device has detected. The states of VD_STD[3:0] are shown Tables 1 and 2.

TABLE 1: Progressive Scan Standards Indication (VD_STD[3]=0)

| VD_STD[3:0] | DESCRIPTION |
|---|---|
| 0000 | 720p (60 & 60/1.001Hz → L/M) [SMPTE296M] |
| 0001 | Reserved |
| 0010 | 1080p (30 & 30/1.001Hz → G/H) [SMPTE274M] |
| 0011 | Reserved |
| 0100 | 1080p (25Hz → I) [SMPTE274M] |
| 0101 | Reserved |
| 0110 | 1080p (24 & 24/1.001Hz → J/K) [SMPTE274M] |
| 0111 | Unknown Progressive with F = 0 always. |

TABLE 2: Interlaced Standards Indication (VD_STD[3]=1)

| VD_STD[3:0] | DESCRIPTION |
|---|---|
| 1000 | 1080i (30 & 30/1.001Hz → D/E) [SMPTE274M] |
| 1001 | Reserved |
| 1010 | 1080i (25Hz → F) [SMPTE274M] |
| 1011 | Reserved |
| 1100 | 1080i (25Hz → C) [SMPTE295M] |
| 1101 | Reserved |
| 1110 | 1035i (30 & 30/1.001Hz → A/B) [SMPTE260M] |
| 1111 | Unknown Interlaced with F switching 0/1 |

Note the following in the above Standards Indication Tables:

- SMPTE260M is 1125 lines/frame
- SMPTE274M is 1125 lines/frame
- SMPTE295M is 1250 lines/frame
- SMPTE296M is 750 lines/frame

*See Table 3 for more details on the source format parameters.*

### 3.4 FLY WHEEL OPERATION

The flywheel logic checks the incoming video data for valid video lines. If the incoming data represents a valid line, the flywheel remains in sync with the incoming data. If the incoming data represents an invalid line, the flywheel uses the stored timing information for the past valid line to generate the output HVF timing signals. When three consecutive lines having identical timing are detected, this new timing information is saved and the flywheel operation is updated to this new timing. Mismatches between the HVF information decoded from the data stream and that indicated by the flywheel will trigger the EAV_ERR and SAV_ERR signals as shown in Figure 3. HVF output timing is shown in Figure 2.

### 3.5 AUTOMATIC SWITCH LINE LOCK HANDLING

The automatic switch line lock is based on the assumption that switching occurs between video sources of the same format. In other words, the switching of video sources causes only the H signal to be out of alignment whereas V and F signals remain in sync. Therefore, when in the automatic switch line lock mode (FAST_LOCK transitions for low to high), the flywheel positive H signal transition aligns with the detected positive H signal transition. Timing for the FAST_LOCK signal is shown in Figure 5.

### 3.6 FIFO

The device does not flag transmission errors which might exist in the ANC data packages. The internal FIFO is 1024 words deep for each of LUMA and CHROMA channels. For those formats where the HANC region is greater than 1024 words, the user must take steps to ensure the FIFO does not overflow, otherwise data may be lost. The GS1500 provides status signals to indicate the current content level of the internal FIFO buffers, as described in section 6.1.

#### 3.6.1 FIFO Status Bits

The device provides status output signals FF_STA[2:0] that indicate the state of the current content level of the internal FIFO buffers. If the extracted ANC data have completely filled the internal FIFO buffer, FF_STA[2:0] outputs 110. When the internal FIFO is full, any attempt to write data into the FIFO will cause the FIFO to overrun. The device flags this overrun state by setting FF_STA[2:0]=111 and no more data will be extracted from the video stream.

If all ANC data in the FIFO is accessed by the user through the FIFO interface and the internal FIFO becomes empty, then FF_STA[2:0] outputs 001. When the internal FIFO is empty, any attempt to read data from the FIFO will cause the FIFO to under run. The device flags this under run state by setting FF_STA[2:0]=000.

When ANC_Y/$\overline{C}$ is high, FF_STA indicates the status of the LUMA FIFO buffer. When ANC_Y/$\overline{C}$ is low, FF_STA indicates the status of the CHROMA FIFO buffer.

The FIFO status flags must be up-to-date. Therefore, certain FIFO status flags are synchronized with respect to R_CLK, and others are synchronized with respect to PCLK_IN. During a write cycle, status flags controlled by R_CLK experience a three-cycle latency with respect to R_CLK. During a read cycle, status flags controlled by PCLK_IN experience a three-cycle latency with respect to PCLK_IN. *See Table 4 and Figures 6 to 15.*

NOTE: If a simultaneous FIFO read and write operation is to be performed, the FF_STA[2:0] outputs should not be used as they may indicate incorrect FIFO status.

#### 3.6.2 ANC/DATA Extraction

When the control signal ANC/$\overline{DATA}$ is high and $\overline{WEN}$ is low, the device detects the ANC data header and extracts the ANC data (including the header) when these data are present in the video streams. When ANC/$\overline{DATA}$ and $\overline{WEN}$ are both low, the device extracts all original video data into the FIFO. To ensure ANC data extraction from the LUMA or CHROMA channels, empty (unload) the ANC data from the respective FIFO buffer during the active video portion of the data streams. ANC data is extracted from a video stream and written into the corresponding internal FIFO buffer until it is completely full. When a FIFO buffer is full, the FF_STA[2:0] signal is set to 110.

The device provides ANC data copying capability as an alternative to extraction. When EX/$\overline{CP}$ is high, the extraction function is enabled. The device replaces the extracted data in the video streams with their respective blanking levels. If EX/$\overline{CP}$ is low, the copy function is enabled. All the original data remain in the video stream after copying them into the FIFO buffer.

To extract ANC data from the HANC region only, the device provides an automated extraction mode. When the control signal FM_I/$\overline{E}$ is high, the FIFO control signals $\overline{FFRST}$ and $\overline{WEN}$ cannot be used.

In this mode of operation, the device generates reset and enable signals internally, which allows an automated extraction of ANC data from HANC region of the incoming LUMA and CHROMA data streams. The user must supply a proper $\overline{REN}$ signal to enable the access of ANC data stored in the FIFO. These data should be read out of the FIFO during the active video period. Once all words have been read from the FIFO, the FF_STA signal is set to 001. If the user has not emptied the FIFO by the time the next HANC period begins, all data within the FIFO is discarded and the FIFO resets so that read and write address pointers are at their starting position.

When the control signal FM_I/$\overline{E}$ is low, the user has full control over reading from and writing to the FIFO, including the FIFO reset ($\overline{FFRST}$) and FIFO write enable ($\overline{WEN}$).

The ANC data output ANC_OUT[9:0] can be set to a high Z state with the $\overline{FOEN}$ control signal. When $\overline{FOEN}$ is low, the ANC_OUT[9:0] outputs are enabled. When $\overline{FOEN}$ is high, the ANC_OUT[9:0] outputs are in a high Z state. Internal read address pointers are incremented regardless of the state of $\overline{FOEN}$ when $\overline{REN}$ is low.

#### 3.6.3 FIFO Read Control

The FIFO control signal $\overline{REN}$ is the read enable signal used to access ANC data in the internal FIFO through the FIFO interface. The user can access only one of the two internal FIFO buffers at a time. The LUMA FIFO can be read when ANC_Y/$\overline{C}$ is high. The CHROMA FIFO can be read when ANC_Y/$\overline{C}$ is low.

When the internal FIFO is not in the empty or underrun states, it is ready to provide ANC data to the user. At this point, the user should read up to 1024 data words from each FIFO through the FIFO interface. When $\overline{REN}$ is low and a rising edge on R_CLK is detected, the device outputs the next word stored in the FIFO. Each time R_CLK is toggled while $\overline{REN}$ is low, the internal read address pointer (LUMA or CHROMA) is incremented. When $\overline{REN}$ is high, the read address pointer is not incremented.

#### 3.6.4 FIFO Write Control

The FIFO control signal $\overline{WEN}$ is the write enable signal. It enables the ANC data extraction from either the LUMA or the CHROMA video streams into the internal respective FIFO buffers. When $\overline{WEN}$ is LOW, the write address pointer increments with the internal clock at the video data rate. When $\overline{WEN}$ is HIGH, the write address pointer does not increment. To reset both address pointers for read and write to their starting positions, toggle the FIFO reset signal $\overline{FFRST}$ from high to low.

#### 3.6.5 FIFO External Reset

In external FIFO control mode, the internal FIFO address pointers are reset to zero (0) using $\overline{FFRST}$. A recommended external reset process is shown in Figure 16.

### 3.7 READING CRC ERROR FLAGS

The GS1500 provides error flags which track the Cyclic Redundancy Code embedded in each line of LUMA and CHROMA video streams (LINE_CRC_ERR_Y and LINE_CRC_ERR_C, respectively).

NOTE: For users monitoring the status of the CRC error flags, it is strongly recommended that they are read only when $\overline{FOEN}$ is low.

TABLE 3: Source Format Parameters

| Reference SMPTE Standard | 260M | 260M | 295M | 274M | 274M | 274M | 274M | 274M | 274M | 274M | 274M | 296M | 296M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format ID | A | B | C | D | E | F | G | H | I | J | K | L | M |
| Lines/Frame | 1125 | 1125 | 1250 | 1125 | 1125 | 1125 | 1125 | 1125 | 1125 | 1125 | 1125 | 750 | 750 |
| Words/Active Line (each channel Y, Cb/Cr) | 1920 | 1920 | 1920 | 1920 | 1920 | 1920 | 1920 | 1920 | 1920 | 1920 | 1920 | 1280 | 1280 |
| Total Active Lines | 1035 | 1035 | 1080 | 1080 | 1080 | 1080 | 1080 | 1080 | 1080 | 1080 | 1080 | 720 | 720 |
| Words/Total Line (each channel Y, Cb/Cr) | 2200 | 2200 | 2376 | 2200 | 2200 | 2640 | 2200 | 2200 | 2640 | 2750 | 2750 | 1650 | 1650 |
| Frame Rate (Hz) | 30 | 30/M | 25 | 30 | 30/M | 25 | 30 | 30/M | 25 | 24 | 24/M | 60 | 60/M |
| Fields /Frame | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Data Rate Divisor | 1 | M | 1 | 1 | M | 1 | 1 | M | 1 | 1 | M | 1 | M |

NOTE: M=1.001 in the above table.

TABLE 4: FIFO Status Indicator

| FF_STA[2:0] | DESCRIPTION | SYNCHRONIZED TO |
|---|---|---|
| 000 | ERROR Flag; FIFO is under run | R_CLK |
| 001 | FIFO is empty | R_CLK |
| 010 | FIFO is almost empty; <= 32 bytes filled | R_CLK |
| 011 | FIFO is ready | - |
| 100 | FIFO is half full | PCLK_IN |
| 101 | FIFO is almost full; >= 992 bytes filled | PCLK_IN |
| 110 | FIFO is full | PCLK_IN |
| 111 | ERROR Flag; FIFO is over run | PCLK_IN |

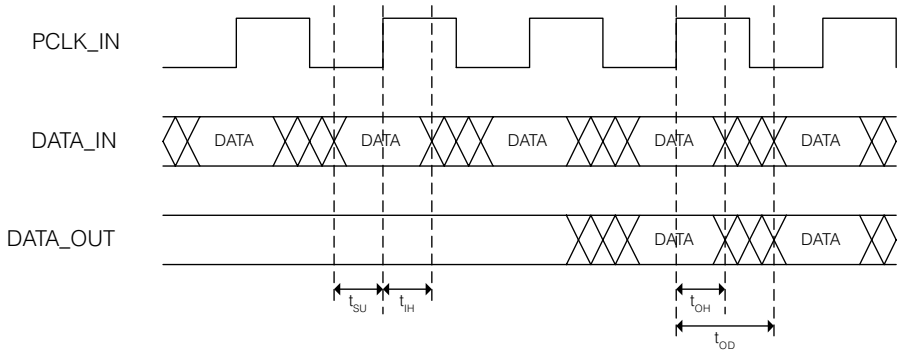



Fig. 1 Synchronous I/O Timing

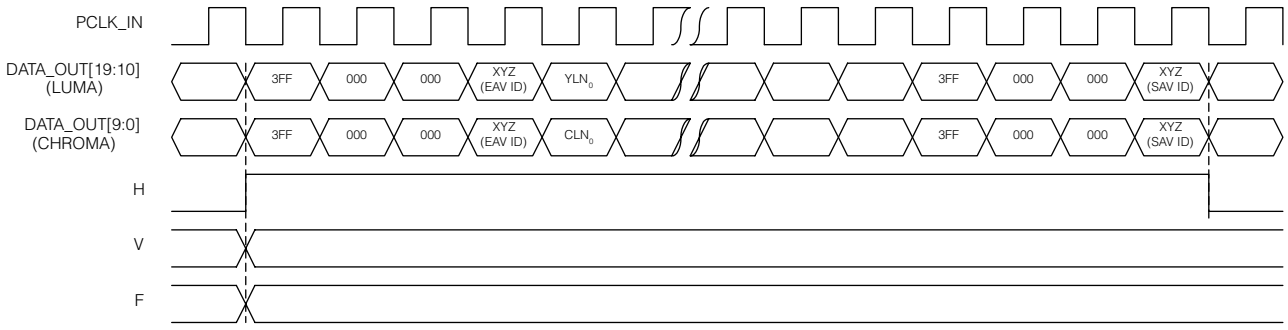



Fig. 2 HVF Timing

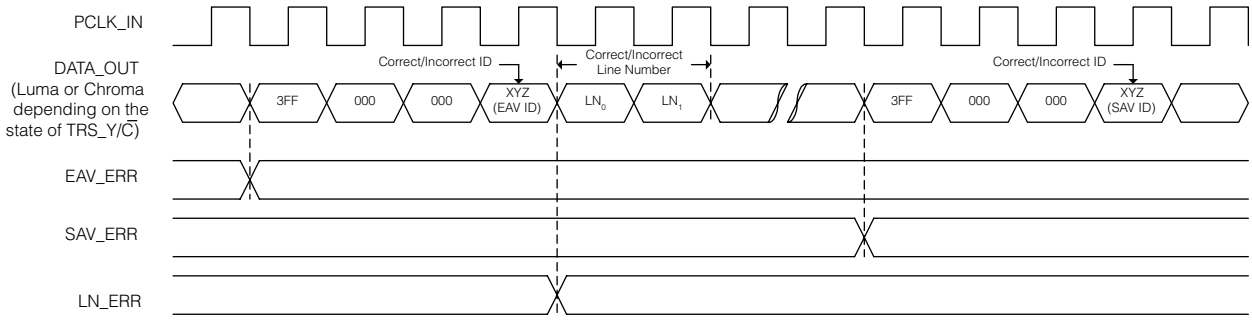



Fig. 3 EAV_ERR, SAV_ERR and LN_ERR Timing

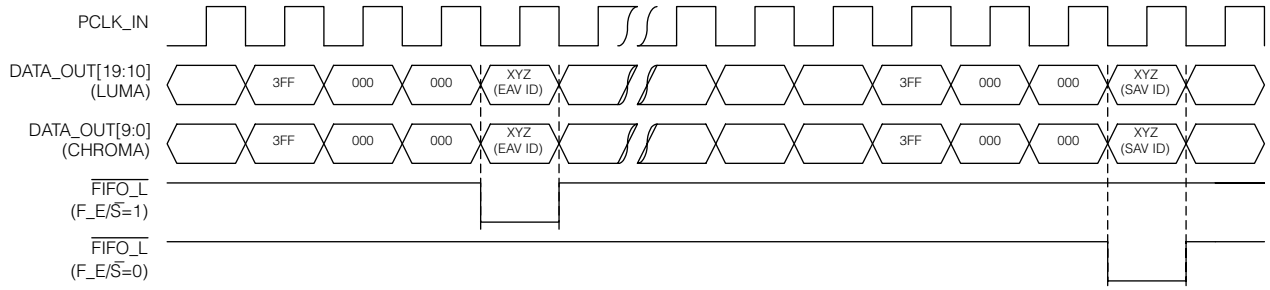



Fig. 4 $\overline{\text{FIFO\_L}}$ Timing

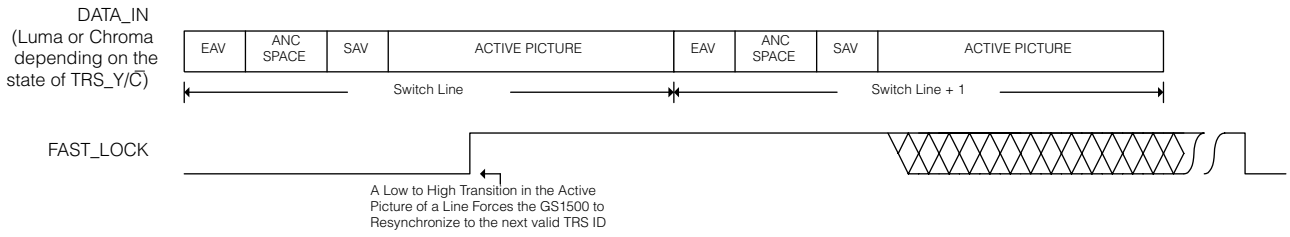



Fig. 5 FAST_LOCK Timing

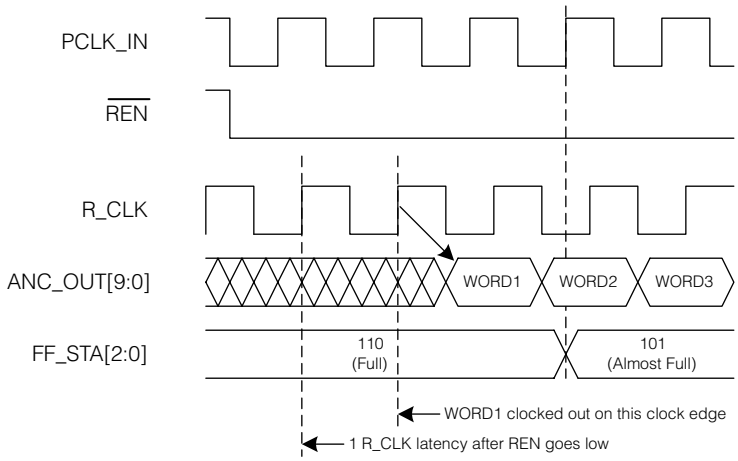



Fig. 6 FIFO Full to Almost Full Read Timing

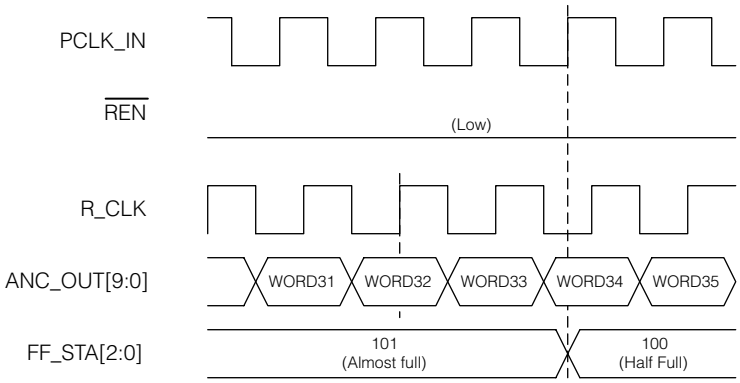



Fig. 7 FIFO Almost Full to Half Full Read Timing

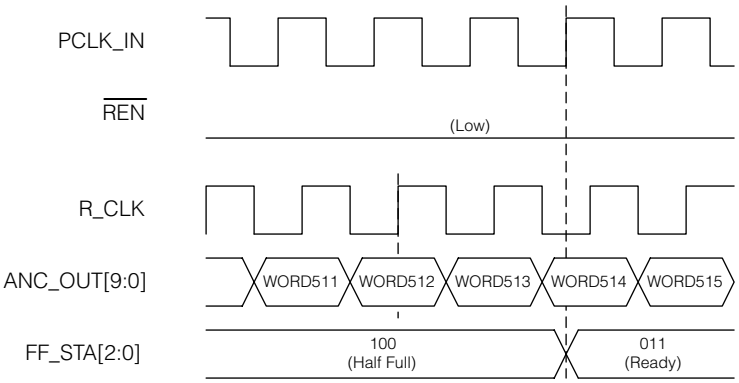



Fig. 8 FIFO Half Full to Ready Read Timing

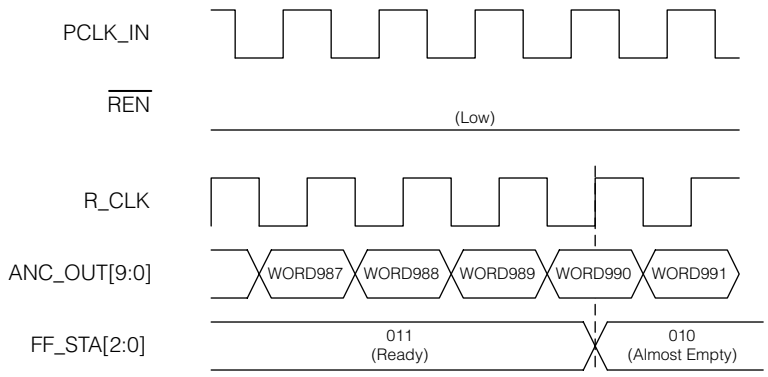



Fig. 9 FIFO Ready to Almost Empty Read Timing

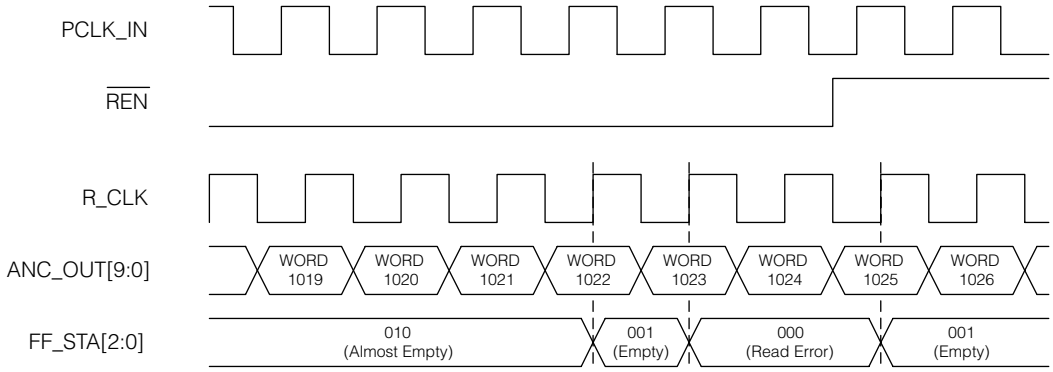



Fig. 10 FIFO Almost Empty to Empty to Read Error Read Timing

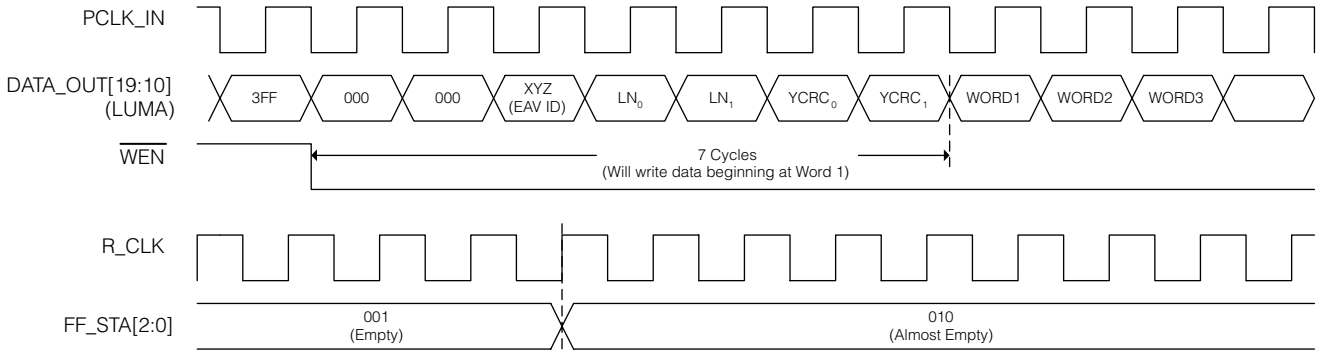



Fig. 11 FIFO Empty to Almost Empty Write Timing

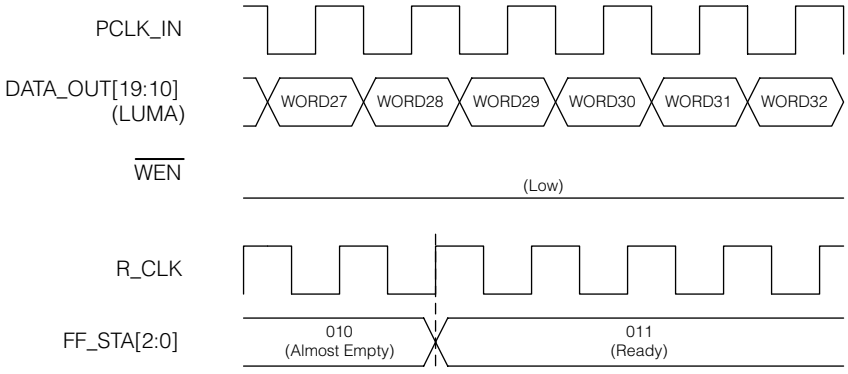



Fig. 12 FIFO Almost Empty to Ready Write Timing

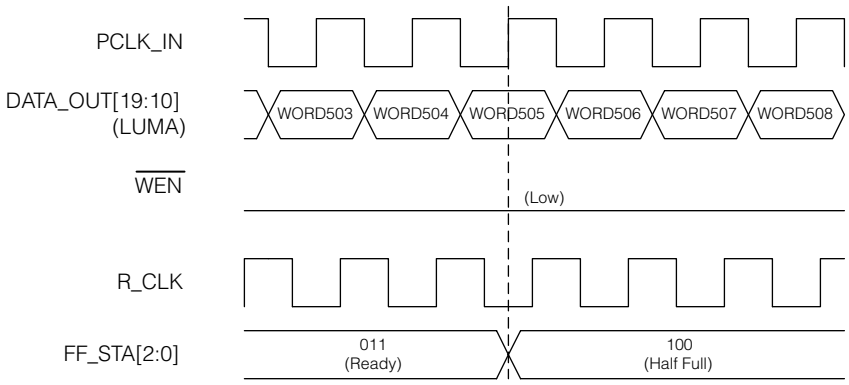



Fig. 13 FIFO Ready to Half Full Write Timing

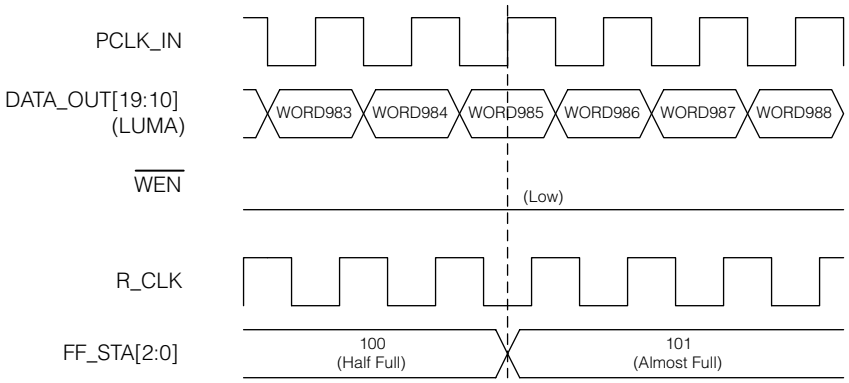



Fig. 14 FIFO Half Full to Almost Full Write Timing

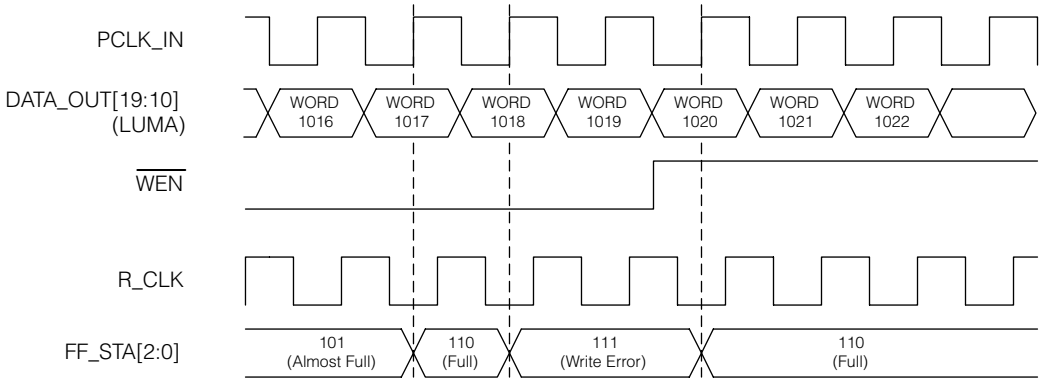



Fig. 15 FIFO Almost Full to Full to Write Error Timing

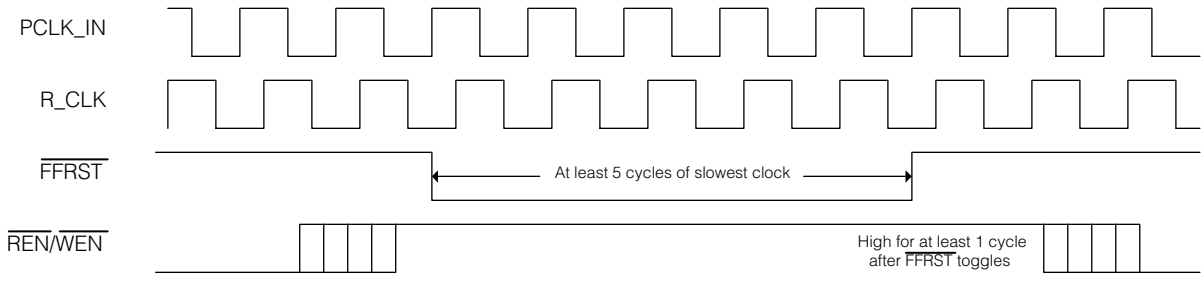



Fig. 16 Recommended External FIFO Reset Process

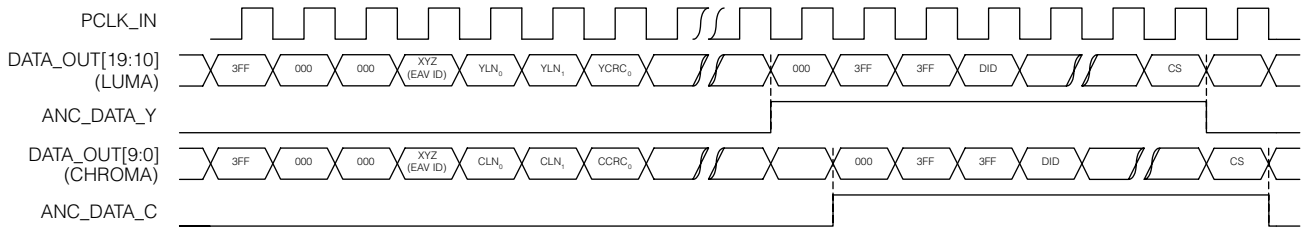



Fig. 17 ANC_DATA_Y and ANC_DATA_C Timing

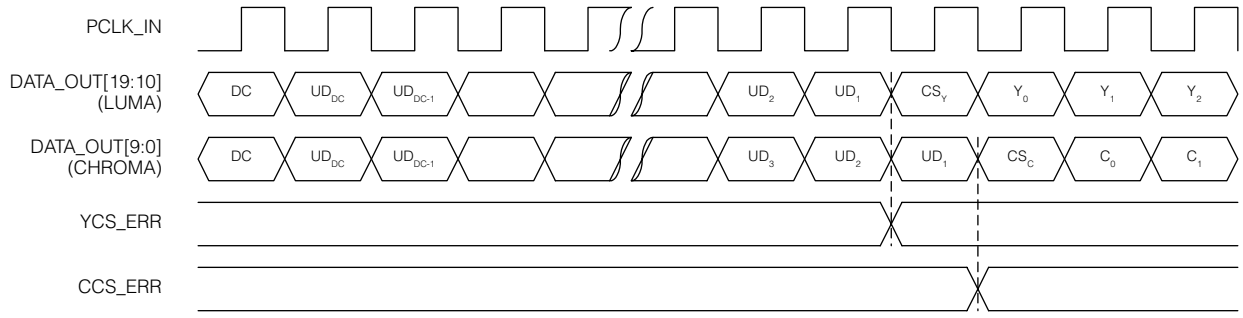



Fig. 18 YCS_ERR and CCS_ERR Timing

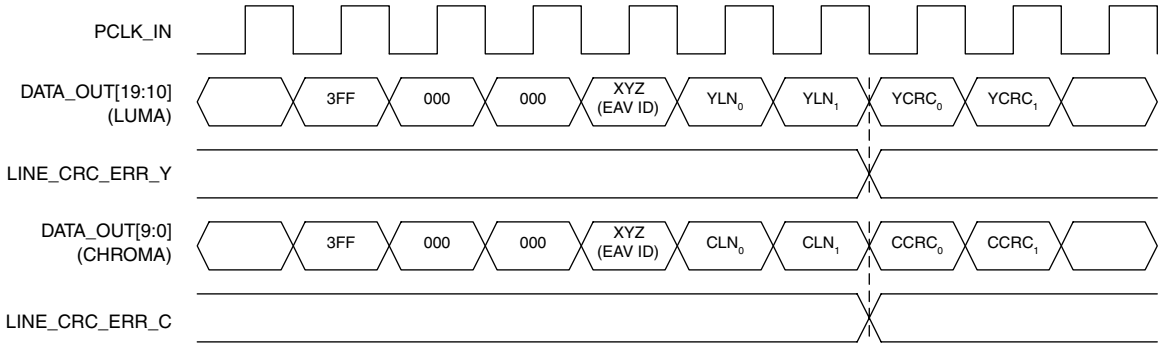


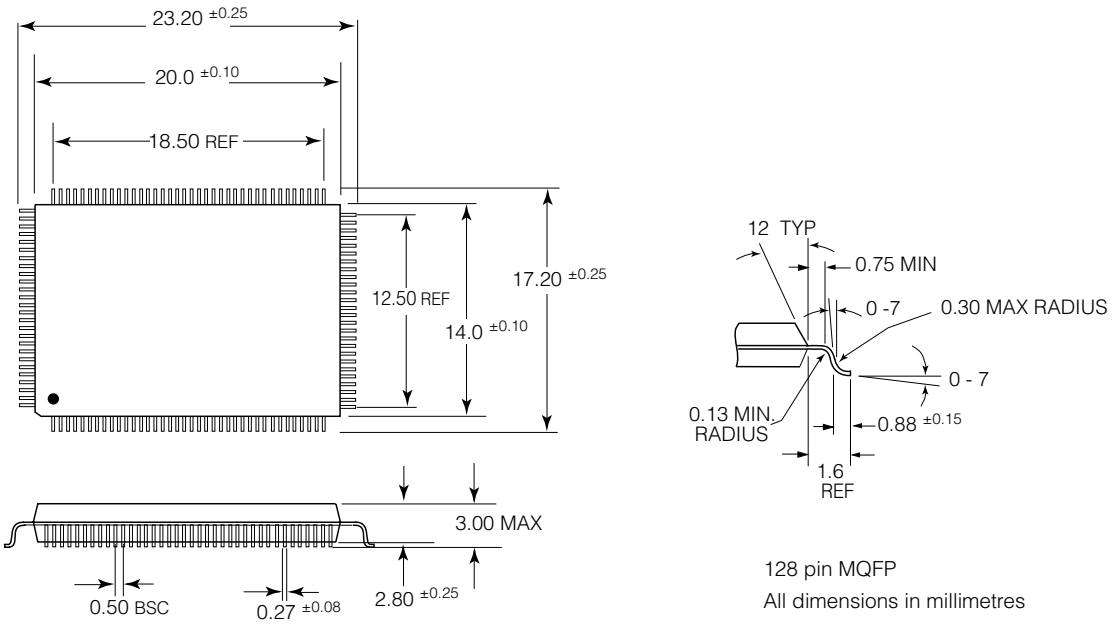

Fig. 19 Luma and Chroma LINE_CRC_ERR Timing

## 4. REFERENCES

Compliant with SMPTE 292M.

## 5. PACKAGE & ORDERING INFORMATION

### 5.1 PACKAGE DIMENSIONS




128 pin MQFP

All dimensions in millimetres

### 5.2 ORDERING INFORMATION

| PART NUMBER | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| GS1500-CQR | 128 pin MQFP | 0°C to 70°C |

**CAUTION**

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

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