Genesys Logic, Inc.

GL422/GL423

USB 2.0 +SD/MMC-controller Combo Solution

Datasheet
Revision 1.00
Aug. 16, 2006

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Revision History

Revision	Date	Description
0.95	09/02/2005	First formal release
0.96	10/18/2005	1.Modify Block Diagram,Ch1 2.Add “56-Pin QFN Package” 3.Add “USB CONTROLLER STRUCTURE”,Ch3 4.Add QFN-56 Package Diagram,Ch4.2 5.Modify “PAD/PIN Descruption”,Ch4.6 6.Add “D.C.Characteristics”, Ch5.3
1.00	08/16/2006	1. Remove 54-Pin LGA Package 2. Add 54-Pin VFBGA Package

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL DESCRIPTION

Genesys Logic's GL422/GL423 controller is an single-chip controllers support both USB2.0 and MMC4.0/SD1.1 specifications. While USB controller and SD/MMC card controller are integrated as a combo-function single chip, this chip provides an enhanced combo solution of USB2.0 and SD/MMC card.

GL422/GL423 is designed based on USB2.0 and MMC4.0/SD1.1 specification. Its unique RAM based firmware strategy provides flexibility for fast compatibility and performance improvement, therefore, give customers strong support to win in today's fast-changing market.

GL422/GL423 manages interface protocol, data storage and retrieval, error detection and correction, defect handling and diagnostic, as well as power management. With a built-in flash management algorithm, GL422/GL423 is applicable for most types of flash in the market: SAMSUNG, MICRON, ST, TOSHIBA, HYNIX and RENESAS.

GL422/GL423 is packaged QFN-56 and VFBGA-54. Both die and QFN/VFBGA package are available and completely meet SD and MMC memory card mechanical thickness requirement. The pin assignment that fits to card sockets provides easy PCB layout.

GL422/GL423 die has a dual channel flash access interface, which remarkably speed up read/write performance. QFN-56 packaged GL422/GL423 supports SD1.1 only. VFBGA-54 packaged GL422/GL423 supports both SD1.1 and MMC4.0.
Figure 1.1 is the block diagram of VFBGA422/GL423.

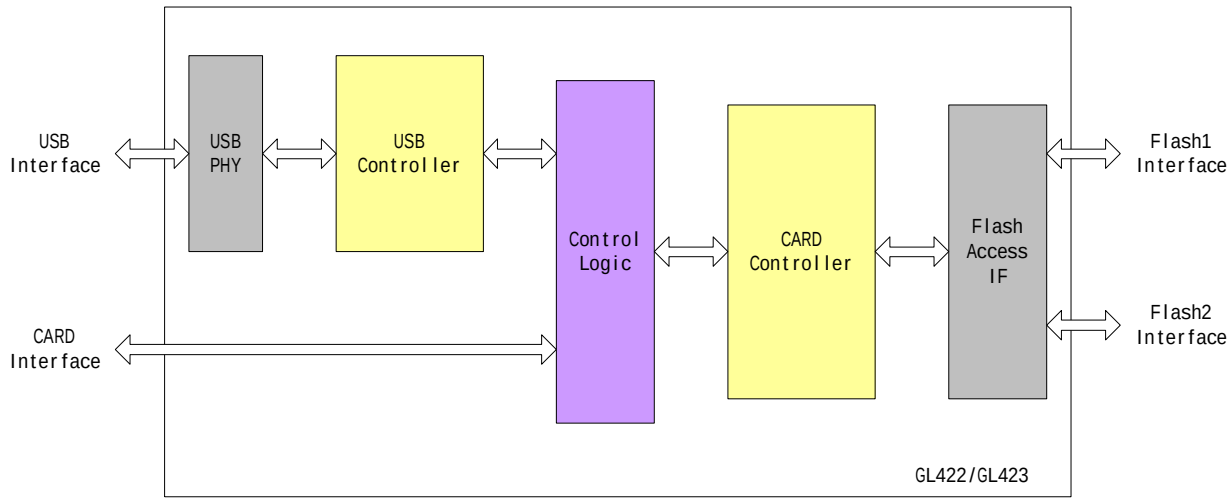


Figure 1.1 - GL422/GL423 Block Diagram

1.1 USB Interface

The USB controller, complied with USB2.0 and USB1.1 specification, explains commands from USB host and transfers data as a USB application.

1.2 CARD Interface

The card controller, complied with SD1.1/MMC4.0 specification, explains commands from SD/MMC host and transfers data between SD/MMC host and flash.

1.3 Flash Access Interface

The flash access interface communicates with CPU. It also manages two channels of flash, based on flash commands. Moreover, it implements defect processing, ECC, and address mapping, etc.

1.4 Control Logic

The control logic module switches the command and data between the USB host and SD/MMC host. By this module, the chip operates in different mode.

1.5 Embedded CPU

Embedded CPU performs arithmetic and logical operations. In addition, it extracts instruction from ROM and SRAM, decodes and executes them. It also manages control and status signals between flash access interface and itself.

CHAPTER 2 FEATURES

2.1 USB 2.0 Interface

- Complies with Universal Serial Bus Specification Version 2.0
- Complies with USB Mass Storage Class Specification Version 1.0
- Integrated USB 2.0 Transceiver Macro-cell (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Supports one USB device address and up to 5 endpoints, including one control, one interrupt and 2 bulk IN/OUT endpoint pairs
- Embedded 8051 micro-controller operates at 60MHz clock
- 64 / 512 bytes Data Payload for full / high speed Bulk Endpoint
- Supports USB 2.0 TEST mode features

2.2 SD Host Interface

- Complies with SD Specification Version 1.1
- Backward compatible with SD Specification, Version 1.0
- Supports SPI mode and CPRM functions
- Supports clock rate up to 25 MHZ for SD1.0
- Supports clock rate up to 52MHz for SD1.1
- Buffers for multi-block flash memory programming
- DMA operation between buffers and flash memory
- Supports automatic CRC16 generation and verification on DATA 3-0

2.3 MMC Host Interface

- Complies with MultiMediaCard System Specification, Version 4.0
- Backward compatible with MultiMediaCard System Specification, Version 3.3
- Supports SPI mode and CPRM functions
- Supports clock rate up to 25 MHZ for MMC 3.3
- Supports clock rate up to 52MHz for MMC 4.0
- Buffers for multi-block flash memory programming
- DMA operation between buffers and flash memory
- Supports automatic CRC16 generation and verification on DATA 7-0

2.4 Flash Memory Interface

- Direct interface to NAND/AND flash chips (SAMSUNG / TOSHIBA / HITACHI / RENESAS / MICRON / ST / HYNIX)
- Direct interface to NOR/OR Flash chips (die only)
- Supports dual-channel, 16 bits flash (die only)
- Drives up to 4 flash memory chips, respectively (die only)
- Supports 64 Mb / 128 Mb / 256 Mb / 512 Mb /1Gb / 2Gb / 4Gb / 8Gb flash chips
- Embedded firmware support for flash file system (FTL)
- Built-in flash management algorithm
- Powerful ECC for error detection and correction up to 6 bytes per 512 bytes

2.5 Micro Controller and Analog System

- RISC core with fast speed and less code size
- Flexibility to update system code
- Ability to add customers' own feature

2.6 Product Packages

- 56-pin QFN package
- 54-pin VFBGA package

2.7 Technology

- 0.18um process

2.8 Manufacture

- Easy firmware development environment
- Supports firmware upgrade tool via PC

CHAPTER 3 PIN ASSIGNMENT

3.1 Function description

3.1.1 USB specification compliance

- Confirms to USB 480Mbps Specification, version 2.0.
- Backward compatible with USB 12Mbps Specification, version 1.1.
- Support one USB device address and up to 5 endpoints, including one control, one interrupt and 2 bulk IN / OUT endpoint pairs

3.1.2 Integrated USB building blocks

- USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)

3.1.3 Embedded 8051 micro-controller

- Operates at 60 MHz clock, 12 clocks per instruction cycle
- Embedded 48K Byte mask ROM and internal 256 byte SRAM
- Embedded 4K Byte external SRAM

3.1.4 3.3V power source

3.1.5 Memory Stick TM interface

- Compliant with Memory Stick interface specification
- Hardware support BS/SDIO/SCLK signals
- Support INS signal
- Support automatic CRC16 generation and verification

3.1.6 Secure Digital (SD) and Multi Media Card (MMC)

- Compliant with Secure Digital / MMC interface specification
- Support both SD / MMC mode access CLK/CMD/DAT0/DAT1/DAT2/DAT3
- Command transmit and response receive can be enabled separately
- Automatic CRC7 generation for command and CRC7 verification for response on CMD
- Support automatic CRC16 generation and verification on DAT3-0
- In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
- Process data in block or byte

3.1.7 High efficient hardware engine

- Automatic data read / write with card by hardware engine
- Easier firmware development
- Media interface signals output low automatically when suspend

3.1.8 Inter-Media transfer capability

- Support copy data between flash cards or within same flash card

3.2 Block diagram

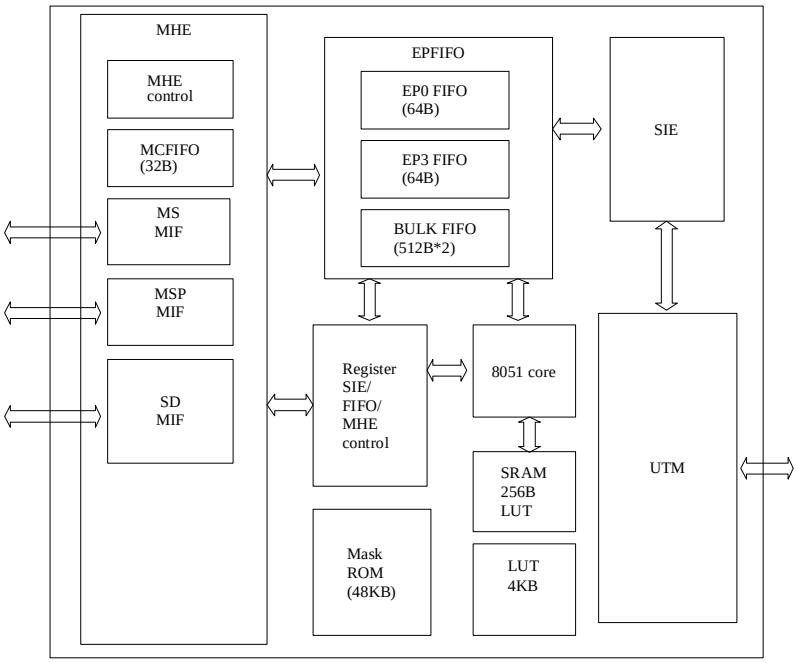


Figure 3.1 - USB Controller diagram

3.2.1 UTM

USB2.0 Transceiver Macro

3.2.2 SIE

Serial Interface Engine

3.2.3 EPFIFO

Endpoint FIFO: it includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFO)

3.2.3.1 Control FIFO FIFO of control endpoint 0.

It is 64-byte FIFO, and it is used for endpoint 0 data transfer.

3.2.3.2 Interrupt FIFO 64-byte-depth FIFO of endpoint 3 for status interrupt.

3.2.3.3 Bulk In/Out FIFO

It can be in the TX mode or RX mode:

- It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
- It can be directly accessed by micro controller
- Support SIE won't transmit data filled before micro controller check data integrity complete.
- It can be used to copy data block from source to destination in the same card or from one card to other card.

3.2.4 MHE

It contains 3 MIF (Media Interface), control and MCFIFO

3.2.4.1 MIFs

- SD / MMC MIF
- Memory Stick MIF
- Memory Stick-PRO MIF

3.2.4.2 MCFIFO

32-byte FIFO shared by Memory Stick, Memory Stick-PRO, SD/MMC MIF.

- Memory Stick and Memory Stick-PRO MIF can use MCFIFO as command FIFO.
- SD/MMC MIF use MCFIFO for command and response.

CHAPTER 4 COMBO STRUCTURE

4.1 Die Diagram

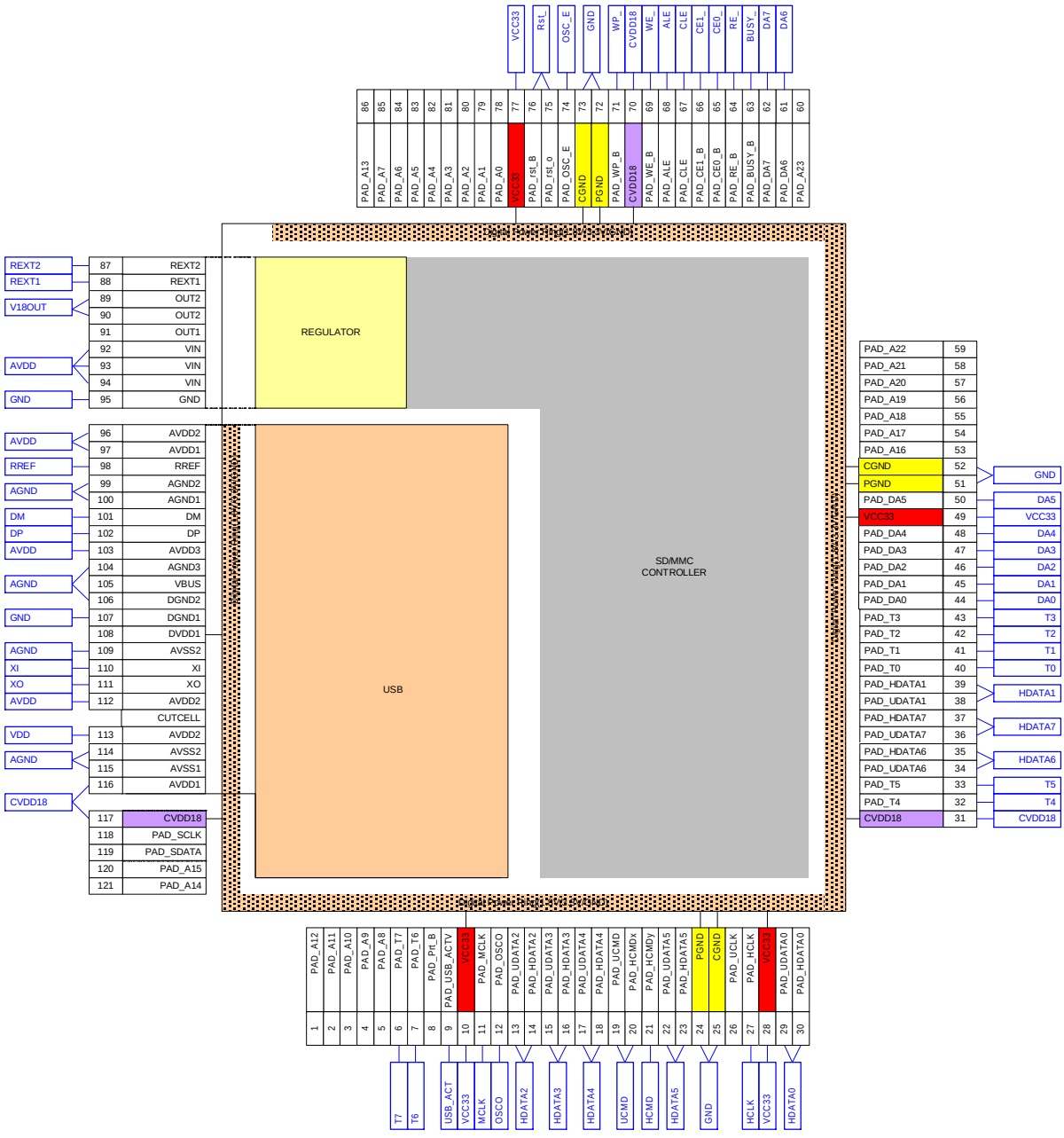


Figure 4.1 - GL422/GL423 Die Diagram

4.2 Die to QFN -56 Package Diagram

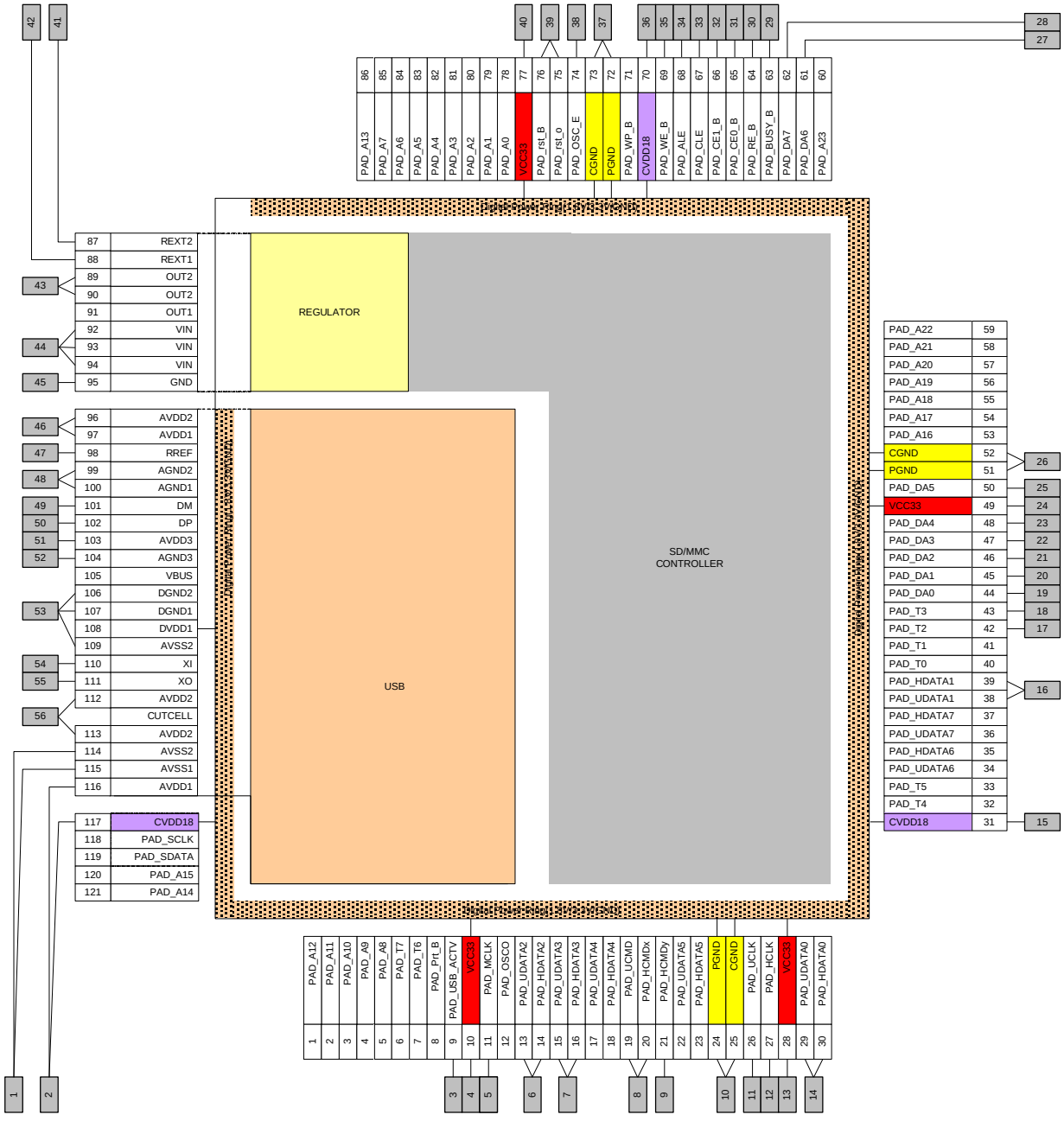


Figure 4.2 - GL422/GL423 Die to QFN-56 Package Diagram

4.3 QFN -56 Package Top View

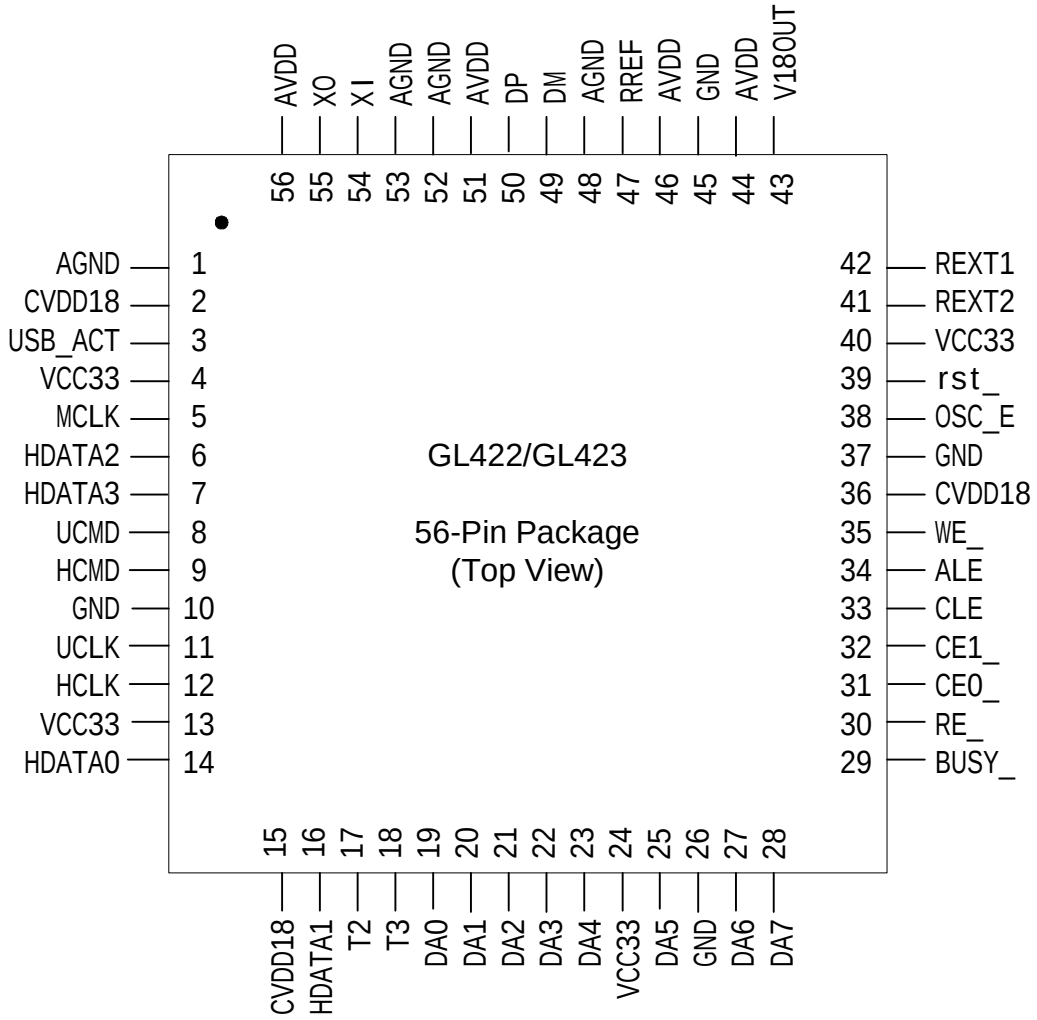


Figure 4.3 - GL422/GL423 QFN 56 Package Top View

4.4 Die to VFBGA -54 Package Diagram

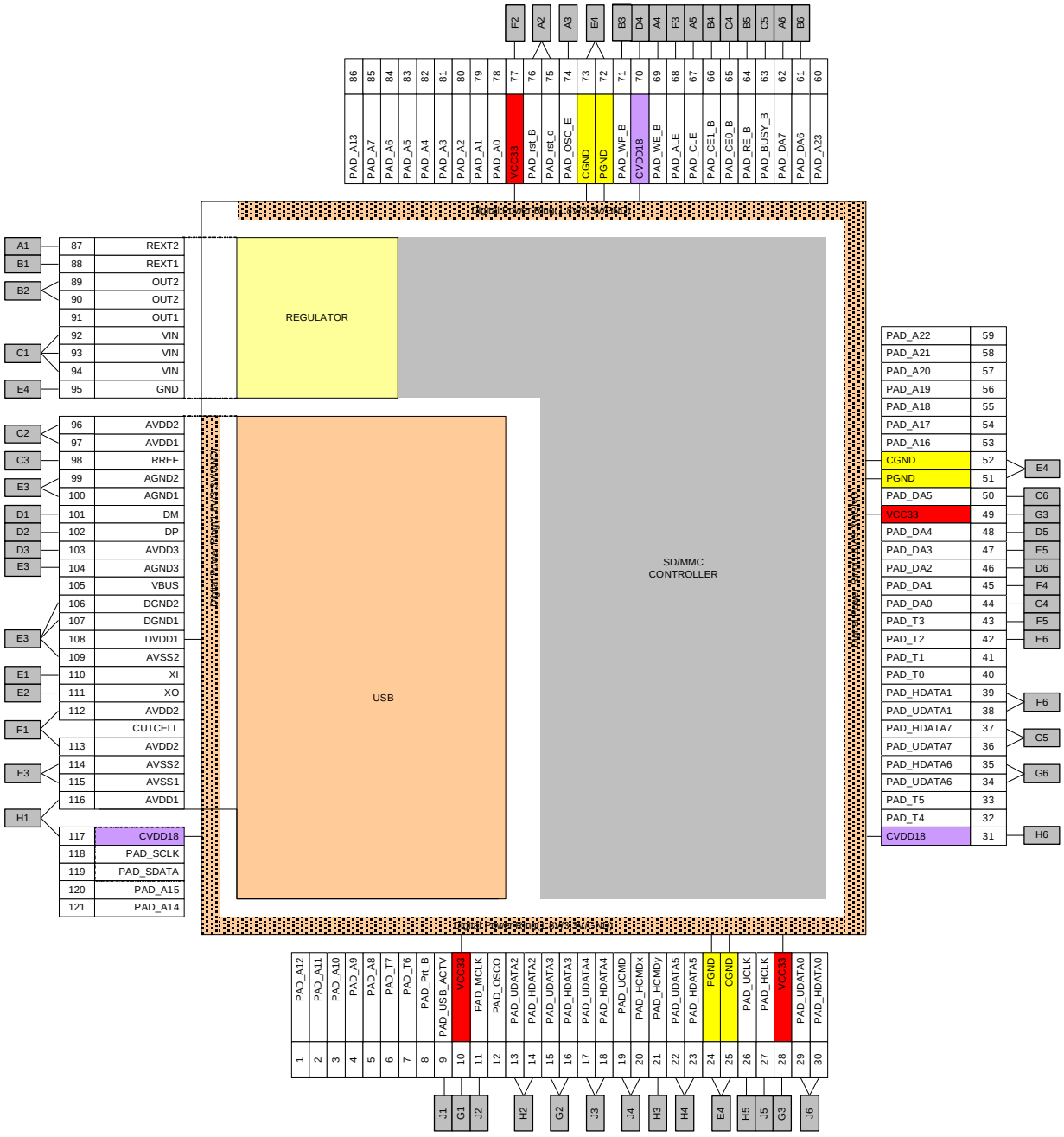


Figure 4.4 - GL422/GL423 VFBGA54 Package Diagram

4.5 VFBGA -54 Package Top View

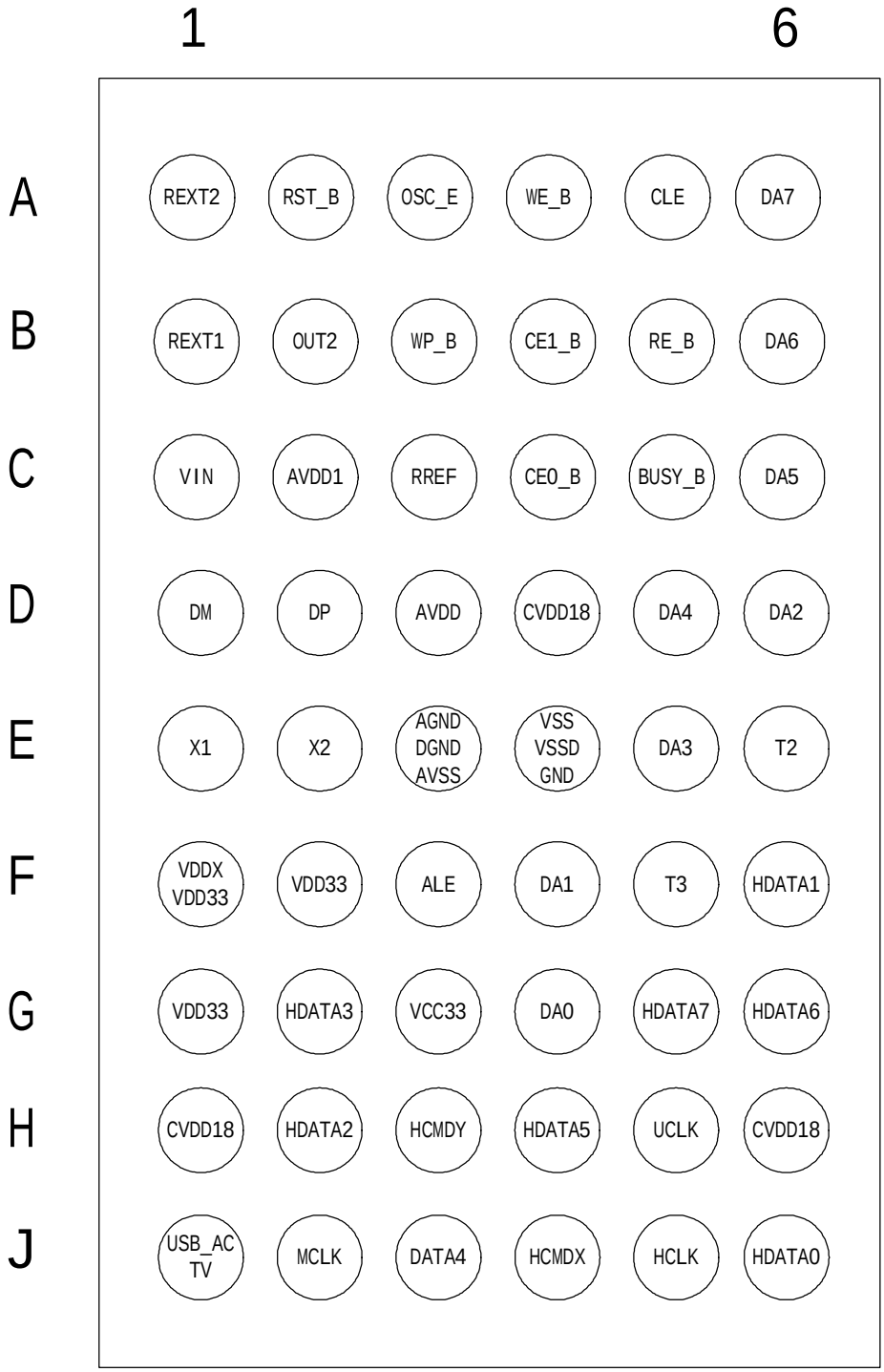


Figure 4.5 - GL422/GL423 VFBGA 54 Package Top View

4.6 PAD/PIN Descripton

4.6.1 USB Interface

Table 4.1- USB Interface

QFN56 Pin#	VFBGA54 Pin#	Pin Name	Pad#	Pad Name	Type	Description
46	C2	AVDD	96	AVDD2	P	Analog 3.3V power (Double Bonding)
			97	AVDD1	P	Analog 3.3V power (Double Bonding)
47	C3	RREF	98	RREF	A	Reference resistor, normal 680ohm (1%) between RREF and GND
48	E3	AGND	99	AGND2	P	Analog ground (Double Bonding)
			100	AGND1	P	Analog ground (Double Bonding)
49	D1	DM	101	DM	B	USB D-
50	D2	DP	102	DP	B	USB D+
51	D3	AVDD	103	AVDD3	P	Analog 3.3V power
52	E3	AGND	104	AGND3	P	Analog ground
NC	NC	—	105	VBUS	P	(No Bonding)
53	E3	AGND	106	DGND2	P	Digital ground. (Tri-bonding)
53	E3	AGND	107	DGND1	P	Digital ground. (Tri-bonding)
NC	NC	—	108	DVDD1	P	Digital power (No Bonding)
53	E3	AGND	109	AVSS2	P	Analog ground (Tri-bonding)
54	E1	XI	110	XI	I	Crystal driver input
55	E2	XO	111	XO	O	Crystal driver output
56	F1	AVDD	112	AVDD2	P	Analog 3.3V power (Double Bonding)
-	-	-	-	CUTCELL	-	(No Bonding)

56	F1	VDD	113	AVDD2	P	Analog 3.3V power (Double Bonding)
1	E3	AGND	114	AVSS2	P	Analog ground (Double Bonding)
			115	AVSS1	P	Analog ground (Double Bonding)
2	H1	CVDD18	116	AVDD1	P	1.8V power supply (Double Bonding)
			117	CVDD18	P	1.8V power supply (Double Bonding)

4.6.2 Regulator Interface

Table 4.2 – Regulator Interface

QFN56 Pin#	VFBGA54 Pin#	Pin Name	Pad#	Pad Name	Type	Description
NC	NC	—	91	OUT1	O	1.8V output (Max.40mA) (No Bonding)
43	B2	V18OUT	89	OUT2	O	1.8V output (Max.100mA) (Double Bonding)
			90	OUT2	O	Regulator 1.8V output (Double Bonding)
44	C1	AVDD	92	VIN	P	Analog 3.3V power (Tri-bonding)
			93	VIN	P	Analog 3.3V power (Tri-bonding)
			94	VIN	P	Analog 3.3V power (Tri-bonding)
45	E4	GND	95	GND	P	Analog ground
42	B1	REXT1	88	REXT1	A	External Resistor pad
41	A1	REXT2	87	REXT2	A	External Resistor pad

4.6.3 Card Interface

Table 4.3 – Card Interface

QFN56 Pin#	VFBGA 54 Pin#	Pin Name	Pad#	Pad Name	Type	Description
11	H5	UCLK	26	PAD_UCLK	B	Controller clock signal from USB reader to card (rising edge)
12	J5	HCLK	27	PAD_HCLK	B	Controller clock signal from HOST Only to card (rising edge)
8	J4	UCMD	19	PAD_UCMD	B	SD/MMC mode: HCMD from/to USB reader SPI mode: Data-in signal from USB reader(Double Bonding)
			20	PAD_HCMDx	B	SD/MMC mode: HCMD from/to HOST SPI mode: Data-in signal from HOST (Double Bonding)
9	H3	HCMD	21	PAD_HCMDy	B	SD/MMC mode: HCMD from/to HOST SPI mode: Data-in signal from HOST
14	J6	HDATA0	29	PAD_UDATA0	B	SD/MMC mode: HDATA0 from/to USB reader SPI mode: Data-out signal to USB reader (Double Bonding)
			30	PAD_HDATA0	B	SD/MMC mode: HDATA0 from/to HOST. SPI mode: Data-out signal to HOST (Double Bonding)
16	F6	HDATA1	38	PAD_UDATA1	B	SD/MMC mode: HDATA1 from/to USB reader. SPI mode: not connected (Double Bonding)

			39	PAD_HDATA1	B	SD/MMC mode: HDATA1 from/to HOST. SPI mode: not connected (Double Bonding)
6	H2	HDATA2	13	PAD_UDATA2	B	SD/MMC mode: HDATA2 from/to USB reader. SPI mode: not connected (Double Bonding)
			14	PAD_HDATA2	B	SD/MMC mode: HDATA2 from/to HOST. SPI mode: not connected (Double Bonding)
7	G2	HDATA3	15	PAD_UDATA3	B	SD/MMC mode: HDATA3 from/to USB reader. SPI mode: CS signal (Double Bonding)
			16	PAD_HDATA3	B	SD/MMC mode: HDATA3 from/to HOST. SPI mode: CS signal (Double Bonding)
NC	J3		17	PAD_UDATA4	B	MMC mode: HDATA4 from/to USB reader. (Double Bonding)
			18	PAD_HDATA4	B	MMC mode: HDATA4 from/to HOST. (Double Bonding)
NC	H4		22	PAD_UDATA5	B	MMC mode: HDATA5 from/to USB reader. (Double Bonding)
			23	PAD_HDATA5	B	MMC mode: HDATA5 from/to HOST. (Double Bonding)
NC	G6		34	PAD_UDATA6	B	MMC mode: HDATA6 from/to USB reader. (Double Bonding)

			35	PAD_HDATA6	B	MMC mode: HDATA6 from/to HOST. (Double Bonding)
NC	G5		36	PAD_UDATA7	B	MMC mode: HDATA7 from/to USB reader. (Double Bonding)
			37	PAD_HDATA7	B	MMC mode: HDATA7 from/to HOST. (Double Bonding)

4.6.4 Flash Interface

The flash interface is used to access AND/NAND flash, defined as Table 4.4. It is also shared with USB test interface, refers to Table 4.7.

Table 4.4 – Flash Interface

QFN56 Pin#	VFBGA 54 Pin#	Pin Name	Pad#	Pad Name	Type	Description
31	C4	CE0_	65	PAD_CE0_B	B	'0' for FLASH chip 0 to select active (low-active).
32	B4	CE1_	66	PAD_CE1_B	B	'0' for FLASH chip 1 to select active (low-active).
33	A5	CLE	67	PAD_CLE	B	FLASH command latch enable
34	F3	ALE	68	PAD_ALE	B	FLASH address latch enable
30	B5	RE_	64	PAD_RE_B	B	FLASH read enable (low active)
35	A4	WE_	69	PAD_WE_B	B	FLASH write enable (low active)
29	C5	BUSY_	63	PAD_BUSY_B	B	FLASH ready when high, busy when low.
NC	B3	WP_	71	PAD_WP_B	B	FLASH write protect (low active)
19	G4	DA0	44	PAD_DA0	B	FLASH bus bit0
20	F4	DA1	45	PAD_DA1	B	FLASH bus bit1
21	D6	DA2	46	PAD_DA2	B	FLASH bus bit2
22	E5	DA3	47	PAD_DA3	B	FLASH bus bit3

23	D5	DA4	48	PAD_DA4	B	FLASH bus bit4
25	C6	DA5	50	PAD_DA5	B	FLASH bus bit5
27	B6	DA6	61	PAD_DA6	B	FLASH bus bit6
28	A6	DA7	62	PAD_DA7	B	FLASH bus bit7

4.6.5 System Interface

Table 4.5 – System Interface

QFN56 Pin#	VFBGA 54 Pin#	Pin Name	Pad#	Pad Name	Type	Description
39	A2	rst_	76	PAD_rst_B	I	Power-on reset input, low active (Double Bonding)
			75	PAD_rst_o	O	Power-on reset output (Double Bonding)
3	J1	USB_ACT	9	PAD_USB_ACTV	B	USB active
NC	NC	—	8	PAD_Prt_B	B	Protect (No Bonding)
NC	NC	—	118	PAD_SCLK	B	Test port CLK. (No Bonding)
NC	NC	—	119	PAD_SDATA	B	Test port Data. (No Bonding)
NC	NC	—	12	PAD_OSCO	O	Clock output for test
5	J2	MCLK	11	PAD_MCLK	I	Main clock input. (No Bonding)
38	A3	OSC_E	74	PAD_OSC_E	I	Oscillator enable
40	F2	VCC33	77	VCC33	P	Digital 3.3V power supply
24	G3	VCC33	49	VCC33	P	Digital 3.3V power supply
13	G3	VCC33	28	VCC33	P	Digital 3.3V power supply
4	G1	VCC33	10	VCC33	P	Digital 3.3V power supply
36	D4	CVDD18	70	CVDD18	P	Digital 1.8V power supply
15	H6	CVDD18	31	CVDD18	P	Digital 1.8V power supply

37	E4	GND	73	CGND	P	Digital Ground (Double Bonding)
			72	PGND	P	Digital Ground (Double Bonding)
26	E4	GND	52	CGND	P	Digital Ground (Double Bonding)
			51	PGND	P	Digital Ground (Double Bonding)
10	E4	GND	25	CGND	P	Digital Ground (Double Bonding)
			24	PGND	P	Digital Ground (Double Bonding)

4.6.6 Test Interface

Table 4.6 – Test Interface

QFN56 Pin#	VFBGA 54 Pin#	Pin Name	Pad#	Pad Name	Type	Description
NC	NC	—	40	PAD_T0	B	Dual channel flash2 bus bit0 to bit7. (on-chip pulled-up). When power-on or hardware reset, T[3:0] is: 4'b0000: USB CPU Test (CPUTST = 1) 4'b0001: USB UTM Scan Mode (UTMSCANM = 1) 4'b0010: USB Scan Mode (SCANMOD = 1) 4'b0011: USB UTM Test (UTMTEST = 1) others: SD Controller Test Mode (T[7:4],T[1:0] no bonding)
NC	NC	—	41	PAD_T1	B	
17	E6	T2	42	PAD_T2	B	
18	F5	T3	43	PAD_T3	B	
NC	NC	—	32	PAD_T4	B	
NC	NC	—	33	PAD_T5	B	
NC	NC	—	7	PAD_T6	B	
NC	NC	—	6	PAD_T7	B	

4.6.7 Use Flash Interface as USB Test Interface

This interface is shared with Flash Interface. This is only for testing. In test mode, the flash interface will be used for USB test patterns:

Table 4.7 –Use Flash Interface as USB Test Interface

Pin Name	Pad#	Pad Name	Type	SCAN MOD	UTM TEST	UTM SCANM	CPU TEST
CE0_	65	PAD_CE0_B	B	DO4	TERM	DO4	
CE1_	66	PAD_CE1_B	B	DO7	SUSP	DO7	
CLE	67	PAD_CLE	B		OP1		
ALE	68	PAD_ALE	B		OP0		
RE_	64	PAD_RE_B	B	DO6	RXERR	DO6	
WE_	69	PAD_WE_B	B	DO1	RXV	DO1	
BUSY_	63	PAD_BUSY_B	B	SCANTEST	TXVH	SCANTEST	
WP_	71	PAD_WP_B	B				
DA0	44	PAD_DA0	B		VMI		
DA1	45	PAD_DA1	B		VPI		
DA2	46	PAD_DA2	B		RXACT		
DA3	47	PAD_DA3	B		TXV		
DA4	48	PAD_DA4	B	DO2	PLLDIS	DO2	
DA5	50	PAD_DA5	B		DataO_Sel		
DA6	61	PAD_DA6	B	DO0	TXRDY	DO0	
DA7	62	PAD_DA7	B				

4.6.8 Use Card Interface as USB Test Interface

This interface is shared with card interface. This is only for testing. In test mode, the card interface will be also used for USB test patterns:

Table 4.8 – Use Card Interface as USB Test Interface

Pin Name	Pad#	Pad Name	Type	SCAN MOD	UTM TEST	UTM SCANM	CPU TEST
UCLK	26	PAD_UCLK	B	SCAN_EN			
UCMD	19	PAD_UCMD	B	DO5	SPEED	DO5	
HDATA0	29	PAD_UDATA0	B	DI0	D0	DI0	P1.0
HDATA1	38	PAD_UDATA1	B	DI1	D1	DI1	P1.1
HDATA2	13	PAD_UDATA2	B	DI2	D2	DI2	P1.2
HDATA3	15	PAD_UDATA3	B	DI3	D3	DI3	P1.3
HDATA4	17	PAD_UDATA4	B	DI4	D4	DI4	P1.4
HDATA5	22	PAD_UDATA5	B	DI5	D5	DI5	P1.5
HDATA6	34	PAD_UDATA6	B	DI6	D6	DI6	P1.6
HDATA7	36	PAD_UDATA7	B	DI7	D7	DI7	P1.7

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Table 5.1 – Absolute Maximum Ratings

Parameter	Symbol	Min	Max.	Unit	Remark
Supply Voltage	V_{DD}	2.0	3.6	V	CMD0, 15,55, ACMD41
Supply Voltage Differentials (V_{ss1}, V_{ss2})		-0.3	0.3	V	
Storage Temperature		-40	85	°C	
Junction Temperature			95	°C	

5.2 Bus Operating Conditions

Table 5.2 – Bus Operating Conditions

Parameter	Symbol	Min	Max.	Unit	Remark
Peak Voltage on all Lines	V_{DD}	2.6	3.6	V	
Ground Voltage		0		V	
Operation Temperature		-25	85	°C	
Operation Moisture and Corrosion			95%		Rel. humidity

5.3 D.C. Characteristics

Table 5.3 – D.C. Characteristics

Parameter	Symbol	Condition	Min	Type	Max	Unit
Supply voltage	V_{CC}		2.0	3.3	3.6	V
Input Leakage Current (HCLK, HCMD and HDATA2-0 to Ground)	I_I	$0< V_{IN} < V_{CC}$	0.2	-	0.3	µA
Input Leakage Current (HCLK, HCMD and HDATA2-0 to V_{DD})	I_I	$0< V_{IN} < V_{CC}$	0.2	-	0.3	µA

Input Leakage Current at HDATA3 to Ground	I_I	$0< V_{IN} < V_{CC}$	-	-	0.43	µA
Output High Voltage at HCMD	V_{OH}	Clock = 20MHZ	-	-	3588	mV
Output High Voltage at HDATA	V_{OH}	Clock = 20MHZ	-	-	3586	mV
Output Low Voltage at HCMD	V_{OL}	Clock = 20MHZ	39	-	-	mV
Output Low Voltage at HDATA	V_{OL}	Clock = 20MHZ	39	-	-	mV
Read/Write Current	I_{CC}		-	-		mA

CHAPTER 6 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (28)	0.75 (30)	0.80 (32)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3		0.20 (8) REF	
b	0.18 (7)	0.25 (10)	0.30 (12)
D		8.00 (315) BSC	
E		8.00 (315) BSC	
D2	6.50 (256)	6.65 (262)	6.80 (268)
E2	6.50 (256)	6.65 (262)	6.80 (268)
e		0.50 (20) BSC	
L	0.35 (14)	0.40 (16)	0.45 (18)
y	---	0.08 (3)	---

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

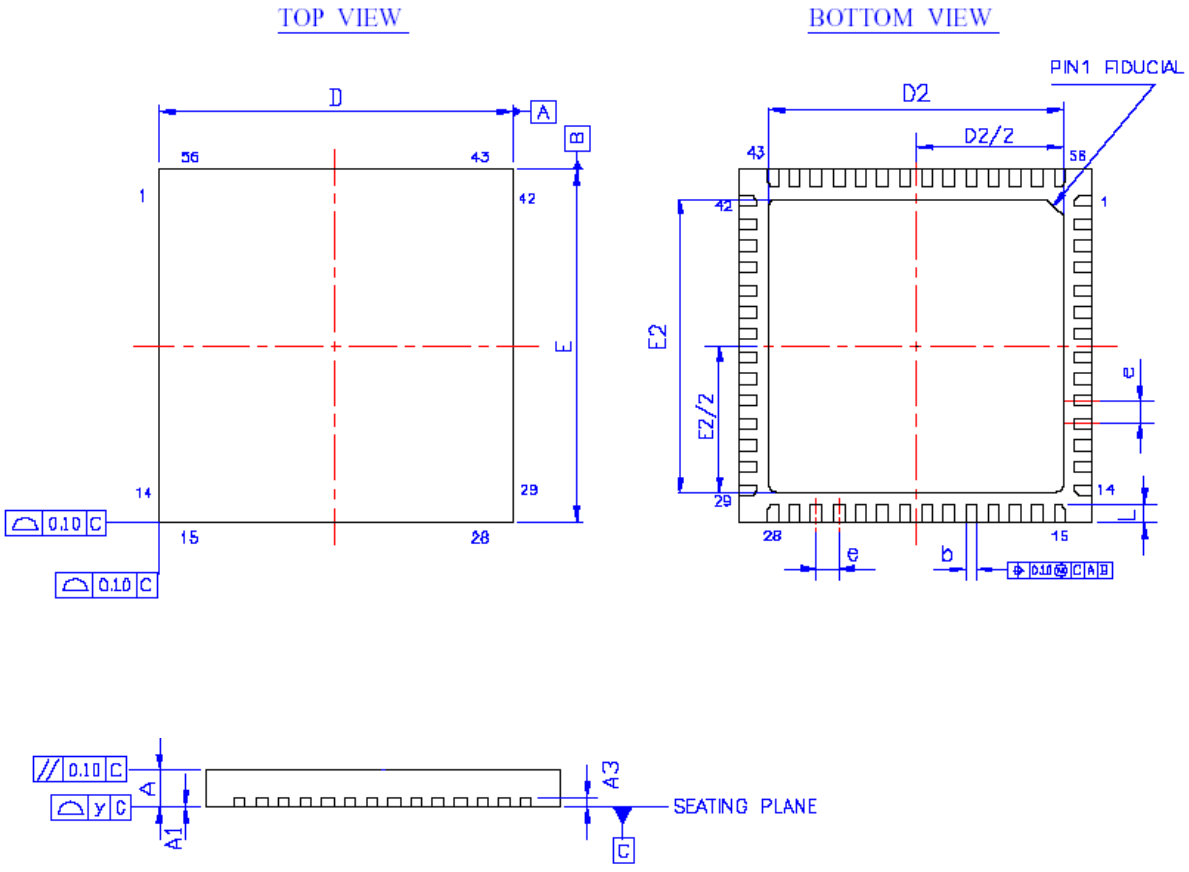
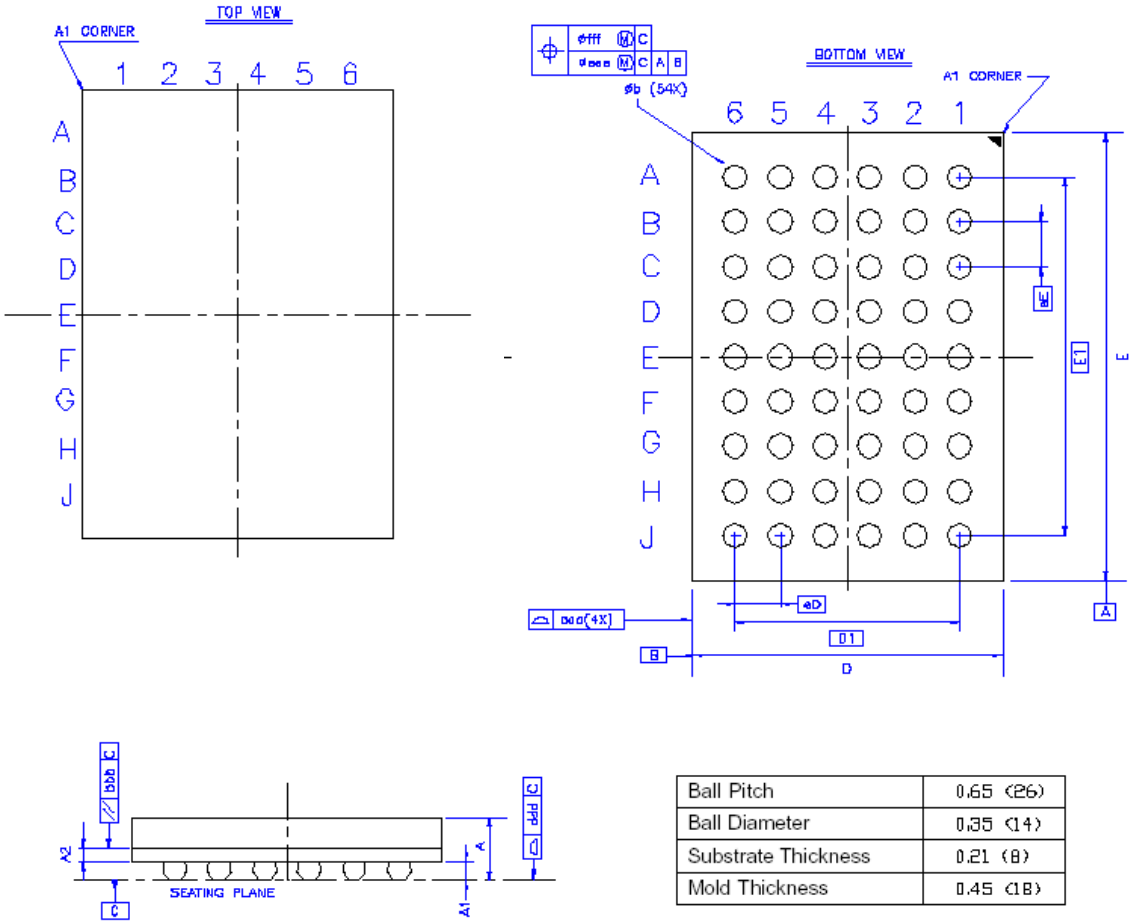


Figure 6.1 – GL422/GL423 56 Pin QFN Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.00 (39)
A1	0.22 (9)		0.32 (13)
A2		0.21 (8)	
b	0.32 (13)		0.42 (17)
D		4.5 (177)	
E		6.5 (256)	
eD	0.65 (26) BSC		
D1	3.25 (128) BSC		
eE	0.65 (26) BSC		
E1	5.20 (205) BSC		
aaa	0.10 (4)		
bbb	0.10 (4)		
ddd	0.08 (3)		
eee	0.15 (6)		
fff	0.08 (3)		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.



Ball Pitch	0.65 (26)
Ball Diameter	0.35 (14)
Substrate Thickness	0.21 (8)
Mold Thickness	0.45 (18)

Figure 6.2 – GL422/GL423 54 Pin VFBGA Package

