1  Brief Description

A Cartesian Loop improves the efficiency and linearity of transmitters for non-constant envelope modulation systems.

The CMX998 is an integrated solution for a Cartesian Feedback Loop based linear transmitter. Acting as a direct conversion quadrature mixer from I and Q to RF output, it provides the capability to linearize the Power Amplifier (PA) via feedback from the PA's output. Included are forward and feedback paths; local oscillator circuitry including loop phase control; an instability detector and uncommitted op-amps for input signal conditioning.

The device operates from a single 3.3V supply over a temperature range of -40°C to +85°C and is available in a 64-pin VQFN (Q1) package.
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</tbody>
</table>
2 Block Diagram

Figure 1 Block Diagram
## 3 Signal List

<table>
<thead>
<tr>
<th>Package Q1 Pin No.</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A2QO</td>
<td>Amplifier 2 output (Q Channel)</td>
</tr>
<tr>
<td>2</td>
<td>EAQP</td>
<td>Error Amplifier Input Positive (Q Channel)</td>
</tr>
<tr>
<td>3</td>
<td>EAQN</td>
<td>Error Amplifier Input Negative (Q Channel)</td>
</tr>
<tr>
<td>4</td>
<td>EAQO</td>
<td>Error Amplifier Output (Q Channel)</td>
</tr>
<tr>
<td>5</td>
<td>MODQP</td>
<td>Modulator Input (Q Channel)</td>
</tr>
<tr>
<td>6</td>
<td>MODQN</td>
<td>Modulator input reference (Q Channel)</td>
</tr>
<tr>
<td>7</td>
<td>VEEQTX</td>
<td>Analogue Ground for Q Channel Modulator</td>
</tr>
<tr>
<td>8</td>
<td>MON</td>
<td>Modulator Output Negative</td>
</tr>
<tr>
<td>9</td>
<td>MOP</td>
<td>Modulator Output Positive</td>
</tr>
<tr>
<td>10</td>
<td>VEEITX</td>
<td>Analogue Ground for I Channel Modulator</td>
</tr>
<tr>
<td>11</td>
<td>MODIN</td>
<td>Modulator input reference (I Channel)</td>
</tr>
<tr>
<td>12</td>
<td>MODIP</td>
<td>Modulator Input (I Channel)</td>
</tr>
<tr>
<td>13</td>
<td>EAIO</td>
<td>Error Amplifier Output (I Channel)</td>
</tr>
<tr>
<td>14</td>
<td>EAIN</td>
<td>Error Amplifier Input Negative (I Channel)</td>
</tr>
<tr>
<td>15</td>
<td>EAIP</td>
<td>Error Amplifier Input Positive (I Channel)</td>
</tr>
<tr>
<td>16</td>
<td>A2IO</td>
<td>Amplifier 2 output (I Channel)</td>
</tr>
<tr>
<td>17</td>
<td>A2IP</td>
<td>Amplifier 2 input Positive (I Channel)</td>
</tr>
<tr>
<td>18</td>
<td>A1IO</td>
<td>Amplifier 1 Output (I Channel)</td>
</tr>
<tr>
<td>19</td>
<td>A1IN</td>
<td>Amplifier 1 Input Negative (I Channel)</td>
</tr>
<tr>
<td>20</td>
<td>A1IP</td>
<td>Amplifier 1 Input Positive (I Channel)</td>
</tr>
<tr>
<td>21</td>
<td>VCCITX</td>
<td>Analogue Supply for I Channel Modulator</td>
</tr>
<tr>
<td>22</td>
<td>VCCLO1</td>
<td>Analogue Supply for LO path</td>
</tr>
<tr>
<td>23</td>
<td>VEELO1</td>
<td>Analogue Ground for LO path</td>
</tr>
<tr>
<td>24</td>
<td>LON</td>
<td>Local Oscillator Negative Input (Note: this pin requires a low impedance dc path to ground)</td>
</tr>
<tr>
<td>25</td>
<td>LOP</td>
<td>Local Oscillator Positive Input (Note: this pin requires a low impedance dc path to ground)</td>
</tr>
<tr>
<td>26</td>
<td>VEELO2</td>
<td>Analogue Ground for LO path</td>
</tr>
<tr>
<td>27</td>
<td>VCCLO2</td>
<td>Analogue Supply for LO path</td>
</tr>
<tr>
<td>28</td>
<td>VCC</td>
<td>Analogue Supply</td>
</tr>
<tr>
<td>29</td>
<td>Spare</td>
<td>(Do not connect to this pin: reserved for future use)</td>
</tr>
<tr>
<td>30</td>
<td>VREF</td>
<td>Bandgap reference decoupling</td>
</tr>
<tr>
<td>31</td>
<td>BVREF</td>
<td>Buffered Vref</td>
</tr>
<tr>
<td>32</td>
<td>VEE</td>
<td>Analogue Ground (0V)</td>
</tr>
<tr>
<td>33</td>
<td>DCMEAS</td>
<td>DC Measurement Output</td>
</tr>
<tr>
<td>34</td>
<td>VDREF</td>
<td>Reference Supply for monitor signals full scale value</td>
</tr>
<tr>
<td>35</td>
<td>VCCIRX</td>
<td>Analogue Supply I Channel Downconverter</td>
</tr>
<tr>
<td>36</td>
<td>SOI</td>
<td>Switch Output (I Channel)</td>
</tr>
<tr>
<td>37</td>
<td>SII</td>
<td>Switch Input when open loop (I Channel)</td>
</tr>
<tr>
<td>38</td>
<td>DOI</td>
<td>Demodulator Output (I Channel)</td>
</tr>
<tr>
<td>39</td>
<td>VEEIRX</td>
<td>Analogue Ground I Channel Downconverter</td>
</tr>
<tr>
<td>40</td>
<td>DIP</td>
<td>Demodulator Input Positive</td>
</tr>
<tr>
<td>41</td>
<td>DIN</td>
<td>Demodulator Input Negative</td>
</tr>
<tr>
<td>42</td>
<td>VEEERX</td>
<td>Analogue Ground Q Channel Downconverter</td>
</tr>
<tr>
<td>43</td>
<td>DOQ</td>
<td>Demodulator Output (Q Channel)</td>
</tr>
<tr>
<td>44</td>
<td>SIQ</td>
<td>Switch Input when open loop (Q Channel)</td>
</tr>
<tr>
<td>Package Q1</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>--------------------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>45</td>
<td>SOQ</td>
<td>Switch Output (Q Channel)</td>
</tr>
<tr>
<td>46</td>
<td>IASIG</td>
<td>Demodulator Output for Instability Detector</td>
</tr>
<tr>
<td>47</td>
<td>VCCQRX</td>
<td>Analogue Supply Q Channel Downconverter</td>
</tr>
<tr>
<td>48</td>
<td>IAI</td>
<td>Instability Amplifier Input</td>
</tr>
<tr>
<td>49</td>
<td>IAO</td>
<td>Instability Amplifier Output</td>
</tr>
<tr>
<td>50</td>
<td>PDI</td>
<td>Peak Detector Input</td>
</tr>
<tr>
<td>51</td>
<td>PDO</td>
<td>Peak Detector Output</td>
</tr>
<tr>
<td>52</td>
<td>VDD</td>
<td>Digital Supply</td>
</tr>
<tr>
<td>53</td>
<td>VDDIO</td>
<td>Supply voltage for digital control interface</td>
</tr>
<tr>
<td>54</td>
<td>SCK</td>
<td>C-BUS Serial Clock</td>
</tr>
<tr>
<td>55</td>
<td>SDI</td>
<td>C-BUS Command Data Input</td>
</tr>
<tr>
<td>56</td>
<td>SDO</td>
<td>C-BUS Reply Data Output</td>
</tr>
<tr>
<td>57</td>
<td>CSN</td>
<td>C-BUS Enable</td>
</tr>
<tr>
<td>58</td>
<td>RESET</td>
<td>General RESET (RESET active LOW)</td>
</tr>
<tr>
<td>59</td>
<td>VSS</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>60</td>
<td>VCCQTX</td>
<td>Analogue Supply for Q Channel Modulator</td>
</tr>
<tr>
<td>61</td>
<td>A1QP</td>
<td>Amplifier 1 Input Positive (Q Channel)</td>
</tr>
<tr>
<td>62</td>
<td>A1QN</td>
<td>Amplifier 1 Input Negative (Q Channel)</td>
</tr>
<tr>
<td>63</td>
<td>A1QO</td>
<td>Amplifier 1 Output (Q Channel)</td>
</tr>
<tr>
<td>64</td>
<td>A2QP</td>
<td>Amplifier 2 Input Positive (Q Channel)</td>
</tr>
</tbody>
</table>

Total = 64 Pins

Table 1 Pin List

3.1 Signal Definitions

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Pins</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD</td>
<td>VCC, VCCIRX, VCCQRX, VCCITX, VCCQTX, VCCLO2, VCCLO1</td>
<td>Power supply for analogue circuits</td>
</tr>
<tr>
<td>DVDD</td>
<td>VDD</td>
<td>Power supply for digital circuits</td>
</tr>
<tr>
<td>VDDIO</td>
<td>VDDIO</td>
<td>Power supply voltage for digital interface (C-BUS)</td>
</tr>
<tr>
<td>VDref</td>
<td>VDREF</td>
<td>Power Supply for scaling analogue measurement signal outputs. (RF detector, instability detector and DC offset measurement)</td>
</tr>
<tr>
<td>DVSS</td>
<td>VSS</td>
<td>Ground for digital circuits</td>
</tr>
<tr>
<td>AVSS</td>
<td>VEE, VEEIRX, VEEQRX, VEEITX, VEEQTX, VEELO2, VEELO1</td>
<td>Ground for analogue circuits</td>
</tr>
</tbody>
</table>

Table 2 Definition of Power Supply and Reference Voltages
4 External Components

4.1 Power Supply Decoupling

The CMX998 has separate supply pins for the analogue and digital circuitry: a 3.3V nominal supply is recommended for all circuits.

![Power Supply Connections and Decoupling Diagram]

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>10nF</td>
</tr>
<tr>
<td>C2</td>
<td>10nF</td>
</tr>
<tr>
<td>C3</td>
<td>10nF</td>
</tr>
<tr>
<td>C4</td>
<td>10nF</td>
</tr>
<tr>
<td>C5</td>
<td>10nF</td>
</tr>
<tr>
<td>C6</td>
<td>10nF</td>
</tr>
<tr>
<td>C7</td>
<td>10nF</td>
</tr>
<tr>
<td>C8</td>
<td>10nF</td>
</tr>
<tr>
<td>R1</td>
<td>3.3Ω</td>
</tr>
<tr>
<td>R2</td>
<td>3.3Ω</td>
</tr>
<tr>
<td>R3</td>
<td>3.3Ω</td>
</tr>
<tr>
<td>R4</td>
<td>3.3Ω</td>
</tr>
<tr>
<td>R5</td>
<td>3.3Ω</td>
</tr>
<tr>
<td>R6</td>
<td>3.3Ω</td>
</tr>
<tr>
<td>R7</td>
<td>10Ω</td>
</tr>
<tr>
<td>R8</td>
<td>10Ω</td>
</tr>
</tbody>
</table>

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated

Note:

It is expected that low frequency interference on the 3.3 Volt supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important, to ensure that there is no interference from the VDDIO (which supplies the digital I/O) or from any other circuit that may use the +3V3_DIG supply (such as a microprocessor), to sensitive analogue supplies like VCCITX or VCCIRX. It is therefore advisable to use separate power supplies for the digital and analogue circuitry.

The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well; this may be cost effectively done with the resistor and capacitor values shown. The use of resistors results in small DC voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the DC current requirements of each supply, ensures the DC voltage drop on each supply are reasonably matched. In any case the DC voltage change that results is well within the design tolerance of the device.
If higher impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when parts of the device are enabled or disabled. It is also advisable to have separate ground planes for the analogue and digital circuits.

### 4.2 Upconverter

![Modulator and Bias External Components Diagram]

**Figure 3** Modulator and Bias External Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>10nF</td>
</tr>
<tr>
<td>C2, C3</td>
<td>33nF</td>
</tr>
<tr>
<td>C4</td>
<td>1µF</td>
</tr>
<tr>
<td>T1</td>
<td>Balun 4:1 (See note 1)</td>
</tr>
<tr>
<td>R1, R2</td>
<td>100 Ω</td>
</tr>
<tr>
<td>R3, R4</td>
<td>(See note2)</td>
</tr>
</tbody>
</table>

**Note 1:** For example TC4-14 from mini circuits.

**Note 2:** The resistors R3 and R4 are optional. Fitting these with 110 Ω resistors will give a good broadband match however will reduce output level available. For many applications they will be unnecessary.

**Table 3** Up-converter Components
4.3 Down Converter

A 1:1 balun transformer should be used on the input to the down converter.

![Downconverter External Component Configuration](image)

Figure 4 – Downconverter External Component Configuration

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1nF</td>
</tr>
<tr>
<td>C2</td>
<td>1nF</td>
</tr>
<tr>
<td>C3</td>
<td>1nF</td>
</tr>
<tr>
<td>T1</td>
<td>Balun 1:1 (e.g. TC1-1-13M from Mini Circuits)</td>
</tr>
</tbody>
</table>

4.4 Local Oscillator Input

A 1:1 balun transformer should be used on the local oscillator input for optimum performance. In the local-oscillator divide by 4 mode, a single ended input may be used by decoupling the LON pin to ground.

![LO Input Configuration using a 1:1 Balun](image)

Figure 5 – LO Input Configuration using a 1:1 Balun

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1nF</td>
</tr>
<tr>
<td>T1</td>
<td>Balun 1:1 (e.g. ETC1-1T-75 from M/A-com)</td>
</tr>
</tbody>
</table>

Note: The configuration of the 1:1 Balun used at the LO input has to create a DC path to analogue GND for both LO inputs, LOP and LON as shown in Figure 5.
4.5 Instability Detector

![Diagram of Instability Detector Section Configuration]

Table 4 Instability Detector Components with Passband above 40kHz

<table>
<thead>
<tr>
<th>C11</th>
<th>1nF</th>
<th>R11</th>
<th>47kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>C12</td>
<td>220pF</td>
<td>R12</td>
<td>4.7kΩ</td>
</tr>
<tr>
<td>C13</td>
<td>470pF</td>
<td>R13</td>
<td>1.8kΩ</td>
</tr>
<tr>
<td>C14</td>
<td>47nF</td>
<td>R14</td>
<td>470kΩ</td>
</tr>
</tbody>
</table>

Table 5 Instability Detector Components with Passband above 300kHz

<table>
<thead>
<tr>
<th>C11</th>
<th>150pF</th>
<th>R11</th>
<th>56kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>C12</td>
<td>22pF</td>
<td>R12</td>
<td>4.7kΩ</td>
</tr>
<tr>
<td>C13</td>
<td>68pF</td>
<td>R13</td>
<td>1.5kΩ</td>
</tr>
<tr>
<td>C14</td>
<td>47nF</td>
<td>R14</td>
<td>470kΩ</td>
</tr>
</tbody>
</table>
4.6 Error Amplifier

A typical error amplifier configuration is shown in Figure 7.

![Figure 7 – Error Amplifier External Component Configuration](image)

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>100pF</td>
</tr>
<tr>
<td>C2</td>
<td>100pF</td>
</tr>
<tr>
<td>C3</td>
<td>33nF</td>
</tr>
<tr>
<td>R1</td>
<td>1kΩ</td>
</tr>
<tr>
<td>R2</td>
<td>1kΩ</td>
</tr>
<tr>
<td>R3</td>
<td>100kΩ</td>
</tr>
<tr>
<td>R4</td>
<td>150Ω</td>
</tr>
<tr>
<td>R5</td>
<td>15Ω</td>
</tr>
</tbody>
</table>

**Table 6 – Error Amplifier Typical Component Values**

The component values shown in Table 6 give 40dB of gain, with the 1st pole at ~16kHz, 2nd pole at ~32kHz and the zero at ~320kHz.
5 General Description

The CMX998 is a single chip transmitter IC providing all the functionality necessary to implement a Cartesian Feed-back Loop transmitter with the addition of an external power amplifier, coupler and fixed value feed-back attenuator. A block diagram of the IC is shown in section 2. The IC can support a wide range of modulation formats and standards including TDMA operation.

The following sections describe the functionality of the IC.

5.1 Input Amplifiers

Differential amplifiers are provided for conversion of differential input signals to single ended format. This is necessary when interfacing to the CMX980A or the CMX981 Advanced Digital Baseband Processor. This amplifier may also be configured to provide DC level translation, filtering and signal gain/attenuation.

Further amplifiers are provided that may be used to implement additional filtering, if required.

5.2 Forward Path

The forward path of the IC comprises two ‘error amplifiers’ followed by an I/Q vector modulator.

The ‘error amplifiers’ are differential amplifiers where the feedback signal is compared with the reference modulation input and an ‘error’ signal is produced. This ‘error’ signal is effectively a pre-distorted waveform that when applied to the remainder of the forward path will produce a ‘perfect’ signal at the output. To ensure loop stability a filter must be used. The ‘error amplifier’ may be configured as an active filter / integrator to provide this function. The bandwidth of the filter is selectable with external components as this can be used to optimise parameters in the loop. Additional filtering may be used between the ‘error amplifier’ output and the input to the I/Q modulator.

The I/Q modulator provides translation from baseband I and Q signals to a modulated RF signal. The wideband noise of this modulator is optimised to ensure a low noise floor at the output, compliant with common product standards. This stage also provides gain control to allow levels around the loop to be optimised.

5.3 Feedback Path

The feedback path of the IC comprises a variable attenuator, down-converter I/Q mixers, baseband amplifiers and switching, to enable operation in ‘open loop’ mode.

Linearity of the down-converter is critical to the overall performance of the Cartesian loop, also a low noise figure is vital to ensure that emissions limits of typical product standards are met. As a result the input attenuators and I/Q down-converter mixers offer an excellent combination of noise and linearity.

Low noise baseband amplifiers provide the correct gain to ensure signal levels around the loop are optimised for noise and linearity. The baseband chain provides various outputs to allow connection to monitoring ADC for loop calibration. To ensure the loop has good stability and can thus achieve maximum linearisation, the down-converter baseband path is broadband and achieves low time-delay.

The loop switches provide the ability to break the loop and operate in open loop mode while simultaneously reducing the gain of the error amplifiers. This mode can be useful for loop phase calibration. When the loop switches are in the normal (closed loop) position, the output of the down-converter is connected to the error amplifiers via external resistors. With the loop switches open, the error
amplifier inputs are connected to the SII and SIQ pins. These pins may be connected to the reference voltage via a resistor which may be chosen to set the error amplifier gain in the open-loop mode.

## 5.4 Local Oscillator Phase Shifting

The local oscillator signal supplied to the IC may be at twice or four times the desired operating frequency and a selectable divider is provided to select between these two options. Internal division is used to generate in phase and quadrature local oscillator signals. The feedback path LO chain has a 360 degree phase shifter included to allow loop phase to be adjusted. The forward path LO chain is optimised for low noise to achieve the best possible wideband noise floor of the transmitter.

A bit is provided in the frequency control register to tune the phase shifter for optimum phase step accuracy at low and high frequencies, the breakpoint being around 500MHz.

## 5.5 DC Nulling

An error in the DC content of the drive to the up-converter modulator will result in carrier leakage in the output signal. In the Cartesian loop, DC signals can be caused by offset errors generated in the down-converter path, or errors in the input signal. It is possible to correct the errors by pre-compensating the input signal. The IC includes circuits to allow easy measurement of the error between the reference and the modulation signal from the error amplifier, as shown in Figure 8.

![Figure 8 Configuration of DCMEAS output switching](image-url)
The levels have been optimised to allow direct interface to an ADC. If the CMX980A or CMX981 is used to generate the I / Q input signals the auxiliary ADC in the same device can be used for measuring the DC offset levels. The x4 scaling of the error allows easy digital arithmetic to find the DC offset correction values which can then be loaded into the CMX980A or CMX981 Transmit I Channel Offset Register and the Transmit Q Channel Offset Register.

The DC Bias Measurement Output (DCMEAS) is a measure of the difference between the mixer reference voltage and the I or Q channel input to the mixer (normally driven from the error amplifier). The measurement is taken from the input to the mixers to allow any losses / gains due to external circuits after the error amplifier to be included in the measurement. The DCMEAS output is centred around a nominal voltage of VDref/2 (see Figure 8). In a typical application the VDref input should be the full scale voltage of the ADC used to sample DCMEAS output. Any error in the reference bias point (VDref /2) may be removed from the measurement by connecting both the differential inputs to the mixer bias, as can be see in Figure 8. If DCMEAS is sampled in this mode, then measured with the mixer input signal connected to one of the differential inputs, the difference between the two results is a measure of the DC offset, excluding the effect of VDref /2.

The reference voltage (VDref) may have any value from 2.1 volts up to the same voltage as AVDD. VDref may not be greater than AVDD + 0.3V. The VDref supply is shared with the instability detector and the RF detector circuits. The DC bias measurement output pin ‘DCMEAS’ is shared with the RF detector circuit. The decoder circuit for enabling the two functions, DCMEAS or RF detector, results in these functions being mutually exclusive.

To aid the measurement and correction of DC levels, the error amplifiers have an internal feedback resistor which may be connected between the output pin and the negative input of each amplifier. A typical configuration is shown in Figure 9. In the normal closed loop operation the error amplifier will typically have a high gain, e.g. 40dB as shown in the figure. In this case the internal switch should be open. During measurement of DC parameters it may be beneficial to reduce the error amp-gain, in which case the internal switch may be closed using the general control register. This method of error amplifier gain reduction is in addition to that provided by the loop switches (see section 5.3).

**Figure 9  Configuration of Error amplifier gain switching.**

Note: Only the I channel is shown but same arrangement is provided on the Q channel.
5.6 Instability Detector

The function of this section is to detect the increasing presence of out-of-band energy that occurs if the Cartesian Loop approaches a region of instability due to incorrect phase correction. To achieve this the Instability Detector is connected so as to look at the “Q” signal provided by the buffered output IASIG.

The Instability Detector comprises a high pass filter, to remove the lower frequencies, (i.e. modulation, present during stable operation), and a detector (peak-hold) stage to provide the analogue level of the out-of-band signal. The circuitry is designed to allow the simple construction of a 3rd order Sallen-Key filter. Figure 6 show how typical filters may be configured.

There is a gain control stage and level shifter included as part of the detector circuit. This allows the user to select one of four gain settings prior to the detection (see Auxiliary Control Register); it also shifts the region of operation so that the detector output is a nominal $V_{D_{ref}}/2$ for no signal and has a maximum limited value of $V_{D_{ref}}$. $V_{D_{ref}}$ is a supply that allows the output of the detector to be conveniently connected to the input of an A-D converter operating from a supply that may be different from that of this device. An example would be connection of this circuit to an auxiliary A-D input on the CMX981, which operates from 2.5V; by supplying the 2.5V as the supply $V_{D_{ref}}$, this would allow the A-D converter to operate so that 1.25V would represent zero signal and give a reasonable dynamic range of operation with a maximum output of close to 2.5V. $V_{D_{ref}}$ must be in the range $2.1V$ to $AV_{DD}+0.3V$ (but not greater than 3.6V).

The examples in Figure 6 have a peak hold capacitor of 47nF and a discharge resistor of 470k. These values may be changed to suit the requirements. A larger capacitor will hold longer at the expense of having a slower attack time; a larger resistor will also give a longer hold time (without affecting attack time). The above example gives attack times (to 90% of final value) in about 100μs and decay to 10% in about 7ms.

5.7 Reference Voltages

The IC includes on-chip reference voltage generation. A pin is provided to allow decoupling of noise. A buffered version of the reference is also provided on a pin. After filtering to remove noise, this may be used to provide DC reference for modulator mixer inputs.

5.8 RF Power Detector

An RF envelope detector is provided in the down converter. The input to the detector is taken between the attenuator block and the down-converter mixers.

Note: The input signal to the detector will vary as the gain control in the feedback path is split between baseband and RF as shown in Figure 10. This results in the detector output increasing as the attenuation increases in 1dB steps (and therefore as the output power from the PA increases), but then returning to its first value on every 5th step increase.
Figure 10  Downconverter Attenuation Configuration and RF Detector

Note: The detector responds to peak envelope rather than average level and has a detection bandwidth greater than 100kHz (response to amplitude modulation). This may be restricted by external capacitance after the DCMEAS output.
6 C-BUS Interface and Register Description

This block provides for the transfer of data and control or status information between the CMX998 internal registers and the µC over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC which may be followed by one or more data bytes sent from the µC to be written into one of the CMX998’s registers, as illustrated in Figure 11.

Data sent from the µC on the Command Data line is clocked into the CMX998 on the rising edge of the Serial Clock input. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Figure 11 gives detailed C-BUS timing requirements.

The following C-BUS addresses and registers are:

<table>
<thead>
<tr>
<th>Register Description</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Reset Register (Address only, no data)</td>
<td>$01</td>
</tr>
<tr>
<td>General Command, 8-bit write only</td>
<td>$02</td>
</tr>
<tr>
<td>Phase Control Register, 8-bit write only</td>
<td>$03</td>
</tr>
<tr>
<td>Gain Control, 16-bit write only</td>
<td>$04</td>
</tr>
<tr>
<td>Forward Path Gain Control, 8-bit write only</td>
<td>$05</td>
</tr>
<tr>
<td>Feedback Path Gain Control, 8-bit write only</td>
<td>$06</td>
</tr>
<tr>
<td>Aux Control, 8-bit write only</td>
<td>$07</td>
</tr>
<tr>
<td>Frequency Control Register, 8-bit write only</td>
<td>$08</td>
</tr>
<tr>
<td>General Command, 8-bit read only</td>
<td>$F2</td>
</tr>
<tr>
<td>Phase Control Register, 8-bit read only</td>
<td>$F3</td>
</tr>
<tr>
<td>Gain Control, 16-bit read only</td>
<td>$F4</td>
</tr>
<tr>
<td>Forward Path Gain Control, 8-bit read only</td>
<td>$F5</td>
</tr>
<tr>
<td>Feedback Path Gain Control, 8-bit read only</td>
<td>$F6</td>
</tr>
<tr>
<td>Aux Control, 8-bit read only</td>
<td>$F7</td>
</tr>
<tr>
<td>Frequency Control Register 8-bit read only</td>
<td>$F8</td>
</tr>
</tbody>
</table>

Notes:

- All registers will retain data if DVDD and VDIO are held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices DVDD and VDIO must be maintained in their normal operating ranges otherwise ESD protection diodes may cause a problem with loading signals connected to SCK, SDO and SDI pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the IC may be powered down without causing this problem.
Figure 11  C-BUS Transactions
6.1 General Reset Command

6.1.1 General Reset Command  C-BUS address $01  
(no data)

This command resets the device and clears all bits of all registers. The General Reset command places the device into Power save mode.

Whenever power is applied to the DVDD pin, a built in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. The RESET pin on the device will also reset the device to the same state.

6.2 General Control Register

6.2.1 General Control Register:  C-BUS address $02  
8-bit write-only

This register controls general features such as Powersave. All bits of this register are cleared to 0 by a General Reset command.

<table>
<thead>
<tr>
<th>Bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Fwd Pwr</td>
<td>FB Pwr</td>
<td>Vbias</td>
<td>Filt Pwr</td>
<td>InputAmp Pwr</td>
<td>Error Amp Pwr</td>
<td>Open loop</td>
<td>Error Amp Gain Red.</td>
</tr>
</tbody>
</table>

General Control Register b7-b2: Select high input gain

These bits control power up/power down of the various blocks of the IC. In all cases ‘1’ = power up, ‘0’ = power down.

| b7 | Enable forward path and common local oscillator sections |
| b6 | Enable feed-back path, phase shifter and common local oscillator sections |
| b5 | Enable bias circuits |
| b4 | Enable filter amplifiers |
| b3 | Enable input amplifier |
| b2 | Enable error amplifiers |

Note: Local oscillator blocks which are common between forward and feed-back paths are enabled by either b7 or b6 being set to ‘1’.

General Control Register b1: Open loop mode

| b1 = 1 | Open loop mode enabled |
| b1 = 0 | Loop closed (Normal Operation) |

General Control Register b0: Error Amplifier Gain Reduction

| b0 = 1 | Error amplifier gain reduction by adding 1kΩ between output and negative input. |
| b0 = 0 | Normal Operation |
6.2.2  General Control Register  C-BUS address $F2
8-bit read-only

This register allows the current settings of register $02 to be read, see section 6.2.1 for details of bit functions.

6.3  Phase Control Register

6.3.1  Phase Control Register:  C-BUS address $03
8-bit write-only

This register controls the loop phase shifters.
All bits of this register are cleared to 0 by a General Reset command.

<table>
<thead>
<tr>
<th>Bit:</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase 1</td>
<td>Phase 2</td>
<td>Phase 3</td>
<td>Phase 4</td>
<td>Phase 5</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

Phase Control Register b7-3: Phase Shift Setting

<table>
<thead>
<tr>
<th>b7 b6 b5 b4 b3</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1 1 1 1</td>
<td>348.75 degrees</td>
</tr>
<tr>
<td>1 1 1 1 0</td>
<td>337.5 degrees</td>
</tr>
<tr>
<td>1 1 1 0 1</td>
<td>Other states follow binary count with steps of 11.25 degrees.</td>
</tr>
<tr>
<td>0 0 0 1 1</td>
<td>22.5 degrees</td>
</tr>
<tr>
<td>0 0 0 0 1</td>
<td>11.25 degrees</td>
</tr>
<tr>
<td>0 0 0 0 0</td>
<td>0 degrees</td>
</tr>
</tbody>
</table>

Phase Control Register b2-0: Reserved for future use, set to '0'.

6.3.2  Phase Control Register:  C-BUS address $F3
8-bit read-only

This register allows the current settings of register $03 to be read, see section 6.3.1 for details of bit functions.
6.4 Gain Control Register

6.4.1 Gain Control Register: C-BUS address $04
16-bit write-only

This register controls forward and feedback path gain. All bits of this register are cleared to 0 by a General Reset.

Gain Control Register b10-7: Reserved for future use, set to '0'.
Gain Control Register b15-11: Forward Path Attenuation

<table>
<thead>
<tr>
<th>b14</th>
<th>b13</th>
<th>b12</th>
<th>b11</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Gain Control Register b15: Reserved for Forward Path Attenuation, set to '0'.
Gain Control Register b5-b1: Feedback Path Attenuation

<table>
<thead>
<tr>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Other states follow binary count with steps of 1dB

0 1 0 1 1
0 1 0 1 0 19dB Attenuation
0 1 0 0 0 1 20dB Attenuation
0 1 0 0 0 0 21dB Attenuation
0 0 1 1 1 1 22dB Attenuation
0 0 1 1 0 1 23dB Attenuation
0 0 1 0 1 1 24dB Attenuation
0 0 1 0 0 1 25dB Attenuation
0 0 0 1 1 1 26dB Attenuation
0 0 0 1 0 1 27dB Attenuation
0 0 0 0 1 1 28dB Attenuation
0 0 0 0 0 1 29dB Attenuation
Gain Control Register b6 and b0: Reserved for Feedback Path Attenuation, set to '0'.

6.4.2 Gain Control Register: C-BUS address $F4
16-bit read-only
This register allows the current settings of register $04 to be read, see section 6.4.1 for details of bit functions.

6.5 Forward Path Gain Control Register

6.5.1 Forward Path Gain Control Register: C-BUS address $05
8-bit write-only
This register controls forward path gain. The same functions can be accessed from register $04.

<table>
<thead>
<tr>
<th>Bit:</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>F5</td>
<td>F4</td>
<td>F3</td>
<td>F2</td>
<td>F1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

For functionality see section 6.4.1. Addressing this register is identical to addressing the most significant 8 bits of register $04. It is the same physical register.

Forward Path Gain Control Register b2-0: Reserved for future use, set to '0'.

6.5.2 Forward Path Gain Control Register: C-BUS address $F5
8-bit read-only
This register allows the current settings of register $05 to be read, see sections 6.4.1 and 6.5.1 for details of bit functions.

6.6 Feedback Path Gain Control Register

6.6.1 Feedback Path Gain Control Register: C-BUS address $06
8-bit write-only
This register controls feedback path gain. The same functions can be accessed from register $04.

<table>
<thead>
<tr>
<th>Bit:</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R7</td>
<td>R6</td>
<td>R5</td>
<td>R4</td>
<td>R3</td>
<td>R2</td>
<td>R1</td>
<td></td>
</tr>
</tbody>
</table>

For functionality see section 6.4.1. Addressing this register is identical to addressing the least significant 8 bits of register $04. It is the same physical register.

Feedback Path Gain Control Register b7: Reserved for future use, set to '0'.

6.6.2 Feedback Path Gain Control Register: C-BUS address $F6
8-bit read-only
This register allows the current settings of register $06 to be read, see sections 6.4.1 and 6.6.1 for details of bit functions.
6.7 **Aux Control Register**

6.7.1 **Aux Control Register: C-BUS address $07**

8-bit write-only

<table>
<thead>
<tr>
<th>Bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC On</td>
<td>Instab Det Enable</td>
<td>RFDet On</td>
<td>DCMEAS</td>
<td>IS1</td>
<td>IS2</td>
<td>DC1</td>
<td>DC0</td>
<td></td>
</tr>
</tbody>
</table>

**Aux Control Register b7: DC On**

Writing ‘b7’ = 1 will power up DC offset measuring circuits, writing ‘b7’ = 0 will place these circuits in zero power mode.

**Aux Control Register b6: Instability Detector Enable**

Writing ‘b6’ = 1 will power up instability detector circuits, writing ‘b6’ = 0 will place these circuits in zero power mode.

**Aux Control Register b5: RF Det On**

Writing ‘b5’ = 1 will power up RF Detector circuits, writing ‘b5’ = 0 will place these circuits in zero-power mode.

**Aux Control Register b4: DCMEAS**

Writing ‘b4’ = 1 will connect the DCMEAS pin to the output of the RF Detector circuits, writing ‘b4’ = 0 will connect the DCMEAS pin to the DC offset measuring circuits.

**Aux Control Register b3-b2**

Controls the gain of the instability detector.

<table>
<thead>
<tr>
<th>Bit</th>
<th>3</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>6dB</td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>12dB</td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>18dB</td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>24dB</td>
<td></td>
</tr>
</tbody>
</table>

**Aux Control Register b1-b0**

<table>
<thead>
<tr>
<th>Bit</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODQN and MODQN</td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODIN and MODIN</td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODIP and MODIN</td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>DCMEAS connected to differential amplifier (gain x4) with inputs connected to MODQP and MODQN</td>
<td></td>
</tr>
</tbody>
</table>

6.7.2 **Aux Control Register: C-BUS address $F7**

8-bit read-only

This register allows the current settings of register $07 to be read, see section 6.7.1 for details of bit functions.
6.8 Frequency Control Registers

6.8.1 Frequency Control Register: C-BUS address $08
8-bit write-only

<table>
<thead>
<tr>
<th>Bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>DIV</td>
<td>0</td>
<td>0</td>
<td>F2</td>
<td>F1</td>
</tr>
</tbody>
</table>

Frequency Control Register b7-5 and b3-2: Reserved for future use, set to '0'.

Frequency Control Register b4: Local Oscillator Divider Control

Writing ‘b4’ = 1 will enable divide the local oscillator by 4 mode, writing ‘b4’ = 0 will enable divide local oscillator by 2 mode.

Frequency Control Register b1-b0

Controls the operating frequency band of the feedback loop.

<table>
<thead>
<tr>
<th>Bit</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Operation below 500MHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Operation above 500MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Note: Frequencies are the operating frequency of the loop, not the local oscillator input frequency.

6.8.2 Frequency Control Register: C-BUS address $F8
8-bit read-only

This register allows the current settings of register $08 to be read, see section 6.8.1 for details of bit functions.
# 7 Performance Specification

## 7.1 Electrical Performance

For definition of voltage and reference signal see Table 2.

### 7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

<table>
<thead>
<tr>
<th></th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (AV\textsubscript{DD} - AV\textsubscript{SS}) or (DV\textsubscript{DD} - DV\textsubscript{SS})</td>
<td>-0.3</td>
<td>+4.0</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on any pin to AV\textsubscript{SS} or DV\textsubscript{SS}</td>
<td>-0.3</td>
<td>V\textsubscript{DD} + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Voltage between AV\textsubscript{SS} and DV\textsubscript{SS}</td>
<td>-50</td>
<td>+50</td>
<td>mV</td>
</tr>
<tr>
<td>Voltage between AV\textsubscript{DD} and DV\textsubscript{DD}</td>
<td>-0.3</td>
<td>+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Current into or out of AV\textsubscript{SS}, DV\textsubscript{SS}, AV\textsubscript{DD} or DV\textsubscript{DD} pins</td>
<td>-50</td>
<td>+50</td>
<td>mA</td>
</tr>
<tr>
<td>Current into or out of any other pin</td>
<td>-20</td>
<td>+20</td>
<td>mA</td>
</tr>
</tbody>
</table>

### Q1 Package

<table>
<thead>
<tr>
<th></th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Allowable Power Dissipation at Tamb = 25°C</td>
<td>-</td>
<td>1000</td>
<td>mW</td>
</tr>
<tr>
<td>... Derating</td>
<td></td>
<td>13</td>
<td>mW/°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-55</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Temperature (see Note below)</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: The Operating Temperature is defined as the temperature measured on the mounting surface of the device whilst the device is operating (i.e. the Case temperature, not the Ambient temperature).

### 7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

<table>
<thead>
<tr>
<th></th>
<th>Notes</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (AV\textsubscript{DD} – AV\textsubscript{SS}) and (DV\textsubscript{DD} – DV\textsubscript{SS})</td>
<td>3.0</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IO Supply (VD\textsubscript{IO} – DV\textsubscript{SS})</td>
<td>1.6</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Reference Supply (VD\textsubscript{ref})</td>
<td>§</td>
<td>2.1</td>
<td>AV\textsubscript{DD} + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature (see Note above)</td>
<td></td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

§ Note: Also the Output Reference (VD\textsubscript{ref}) voltage must not exceed 3.6V.
7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V\text{DD} = AV\text{DD} = DV\text{DD} = 3.0V to 3.6V; VD\text{ref} = 2.1V to V\text{DD}; VD\text{IO} = 1.6V to V\text{DD}; V\text{SS} = AV\text{SS} = DV\text{SS}.

RF performance is only guaranteed at normal operating temperatures (ie T\text{case} = +15 to +55°C). Outside this range but within the maximum limit (section 7.1.2) functionality is guaranteed but performance may be degraded.

<table>
<thead>
<tr>
<th>DC Parameters</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Current Consumption</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power save mode</td>
<td>1, 54</td>
<td>-</td>
<td>10</td>
<td>70</td>
<td>µA</td>
</tr>
<tr>
<td>(Band gap Vref only)</td>
<td></td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td>(Operating)</td>
<td></td>
<td>-</td>
<td>135</td>
<td>160</td>
<td>mA</td>
</tr>
<tr>
<td>Current from VD\text{IO}</td>
<td>2a</td>
<td>-</td>
<td>-</td>
<td>600</td>
<td>µA</td>
</tr>
<tr>
<td>Current from VD\text{ref}</td>
<td>2b</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>mA</td>
</tr>
<tr>
<td>Logic “1” Input Level</td>
<td>70%</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>VD\text{IO}</td>
</tr>
<tr>
<td>Logic ‘0’ Input Level</td>
<td></td>
<td>-</td>
<td>30%</td>
<td>VD\text{IO}</td>
<td></td>
</tr>
<tr>
<td>Logic Input Leakage Current (Vin = 0 to DV\text{DD})</td>
<td>-1.0</td>
<td>-</td>
<td>+1.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Output Logic ‘1’ Level (I\text{OH} = 0.6 mA)</td>
<td>80%</td>
<td>-</td>
<td>-</td>
<td>VD\text{IO}</td>
<td></td>
</tr>
<tr>
<td>Output Logic ‘0’ Level (I\text{OL} = -1.0 mA)</td>
<td>-</td>
<td>-</td>
<td>+0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Power up time</td>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Reference Voltage</td>
<td></td>
<td>-</td>
<td>0.5</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>All blocks except Voltage Reference</td>
<td></td>
<td>-</td>
<td>10</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

Reference Voltage (V\text{ref}, BV\text{ref})

|       | 1.45 | 1.6  | 1.75 | V    |

Notes:
1. Power save mode includes after general reset with all analogue and digital supplies applied and also in the case with V\text{DD} applied but with all analogue supplies disconnected (i.e. in this later scenario power from V\text{DD} will not exceed the specified value whatever the state of the registers).
2a. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5MHz.
2b. Current drawn from VD\text{ref} when either the DC Bias Measurement or the RF Detector circuit are enabled.
## AC Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency Range</td>
<td></td>
<td>100</td>
<td>-</td>
<td>1000</td>
<td>MHz</td>
</tr>
<tr>
<td>Local Oscillator Frequency Range</td>
<td>6</td>
<td>200</td>
<td>2000</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Local Oscillator Input Impedance (Differential)</td>
<td></td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td>Local Oscillator Input Level</td>
<td></td>
<td>-15</td>
<td>-</td>
<td>-10</td>
<td>dBm</td>
</tr>
<tr>
<td>I/Q Input Level</td>
<td></td>
<td>-</td>
<td>-</td>
<td>2.2</td>
<td>V p-p</td>
</tr>
<tr>
<td>I/Q Input Common Mode Voltage</td>
<td></td>
<td>1.2</td>
<td>1.55</td>
<td>1.7</td>
<td>V</td>
</tr>
</tbody>
</table>

### Forward Path

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Path Output Power (PEP)</td>
<td>7, 8, 55</td>
<td>-</td>
<td>+3</td>
<td>+6</td>
<td>dBm</td>
</tr>
<tr>
<td>Forward Path Wideband Noise</td>
<td>9, 10, 55</td>
<td>-148</td>
<td>-145</td>
<td></td>
<td>dBc/Hz</td>
</tr>
</tbody>
</table>

**Forward Path Noise Floor**

- Forward Path Attenuation = 5dB: -153 dBm/Hz
- Forward Path Attenuation = 10dB: -155 dBm/Hz
- Forward Path Attenuation = 15dB: -156 dBm/Hz
- Forward Path Attenuation = 20dB: -158 dBm/Hz
- Forward Path Attenuation = 25dB: -159 dBm/Hz

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Path Image Suppression</td>
<td>55</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Forward Path Intermodulation</td>
<td>14, 55</td>
<td>35</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Forward Path Output Load Impedance (Differential)</td>
<td>56</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>Ω</td>
</tr>
</tbody>
</table>

**Discrete unwanted emissions (other than harmonics of the output) in the frequency range 9kHz - 12.75 GHz.**

### Feedback Path

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback Path Max Input Power (PEP)</td>
<td>8, 15</td>
<td>-22</td>
<td>-</td>
<td>+7</td>
<td>dBm</td>
</tr>
<tr>
<td>Feedback Path Input Impedance</td>
<td>4</td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td>Feedback Path Image Suppression</td>
<td>11, 55</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Feedback Path Gain</td>
<td>18</td>
<td>-</td>
<td>24</td>
<td>-</td>
<td>dBV/V</td>
</tr>
<tr>
<td>Feedback Path Gain Absolute Error From Nominal Gain Setting</td>
<td>55</td>
<td>-</td>
<td>-</td>
<td>±2</td>
<td>dB</td>
</tr>
</tbody>
</table>

**Feedback Path Noise Figure**

- Feedback Path Noise Figure: 21 dB

**Feedback Path Gain Control Range**

- Feedback Path Gain Control Range: 29 dB

**Feedback Path Gain Control Step Size**

- Feedback Path Gain Control Step Size: 1 dB

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain switching time</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>μs</td>
</tr>
<tr>
<td>Feedback Path Bandwidth</td>
<td>12</td>
<td>10</td>
<td>50</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Feedback Path Output Load</td>
<td>17</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>kΩ</td>
</tr>
<tr>
<td>Feedback Path Second Order Intermodulation</td>
<td>13, 55</td>
<td>65</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Feedback Path Third Order Intermodulation</td>
<td>13, 55</td>
<td>65</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Feedback Path Fifth Order Intermodulation</td>
<td>13, 55</td>
<td>75</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
</tbody>
</table>

**Feedback Path Phase Shift at 10MHz with 1 kΩ output load**

- Feedback Path Phase Shift at 10MHz: 50 deg

**Feedback Path Open Loop Isolation**

- Feedback Path Open Loop Isolation: 50 dB

**Feedback Path DC Output (nominal)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback Path DC Output (nominal)</td>
<td>Vref</td>
<td>0.15</td>
<td>Vref</td>
<td>0.15</td>
<td>V</td>
</tr>
<tr>
<td>AC Parameters</td>
<td>Notes</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
<td>Units</td>
</tr>
<tr>
<td>-----------------------------------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>Phase Shift</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Shift Range</td>
<td>-</td>
<td>348.75</td>
<td>-</td>
<td>-</td>
<td>deg</td>
</tr>
<tr>
<td>Phase Shift Step Size</td>
<td>-</td>
<td>11.25</td>
<td>-</td>
<td>-</td>
<td>deg</td>
</tr>
<tr>
<td>Phase Shift Absolute Error</td>
<td>55</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>deg</td>
</tr>
<tr>
<td>Switching time</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>µs</td>
</tr>
</tbody>
</table>

**Notes:**

3. Time from rising edge of the last (8\textsuperscript{th} or 16\textsuperscript{th} depending on whether 8 or 16 bit registers are used) serial clock input following CSN being asserted for write to appropriate control register.

4. The input to the chip is differential. Specified input impedance is measured using a 1:1 balun transformer.

5. Measured at 100kHz with minimum feedback path attenuation, Noise figure as measured in I or Q path.

6. Local oscillator input frequency twice or four times the required operating frequency, selectable with DIV bit (see section 6.8.1).

7. Output power reduced dB for dB with forward path attenuation.


9. Measured between noise floor and mean power in TETRA π/4-DQPSK modulated wanted signal.

10. Measured at 400MHz, 5MHz offset over specified Forward Path Output Power range and with forward path attenuation between 0dB and –5dB, NB: typical noise performance achieved at typical output power and above.

10a. Measured at 400MHz, 5MHz offset with specified Forward Path Output Power for relevant attenuation level.

11. Combination of amplitude and phase balance of I/Q paths.

12. With specified typical output load impedance.

13. Two-tone test, intermodulation product level measured relative to one of the wanted tones, specification met for following conditions:
   - minimum feedback path attenuation and minimum input signal level
   - maximum feedback path attenuation and maximum input signal level
   - All combinations of attenuation and signal level that achieve the same signal level at the output of the feedback path as in the above conditions

14. Specification met for specified maximum output power, two tone test and maintained at all gain steps.

15. Specification for ‘min.’ valid at minimum attenuation and ‘max.’ at maximum attenuation.

16. Measured with modulated output signal at relevant output power for forward path attenuations as specified.

17. Operating into a virtual earth (not ground).

18. Measured as peak-to-peak voltage from c.w. 50 ohm source at input to down converter path, single ended, before balun to peak-to-peak voltage at the output of I or Q paths.

19. Equivalent to 13.89ns delay.
### DC Calibration

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential gain to DCMEAS pin</td>
<td>20</td>
<td>-</td>
<td>4</td>
<td>-</td>
<td>V/V</td>
</tr>
<tr>
<td>Vdco</td>
<td>22</td>
<td>-</td>
<td>VDref/2</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output switching time</td>
<td>21</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>µs</td>
</tr>
</tbody>
</table>

**Notes:**
- An application note on DC Calibration of the CMX998 is available at www.cmlmicro.com.
- 20. Gain of the differential amplifier described in section 5.5 and Figure 8. For detail of circuit control see section 6.7.1.
- 21. Time for output to change between measurement modes, measured from rising edge of CSN.
- 22. Not used.

### I/Q Modulator

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Input Bandwidth</td>
<td></td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Input Signal</td>
<td>0.25</td>
<td>0.35</td>
<td>0.5</td>
<td></td>
<td>Vp-p</td>
</tr>
<tr>
<td>DC Bias Input</td>
<td>23</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Forward Path Gain Control Range</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Forward Path Gain Control Step Size</td>
<td>-</td>
<td>2.5</td>
<td>-</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain switching time</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>Other Parameters see ‘AC Parameters’ table</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
- 23. Normally connected to BVREF pin via RC filter, the tolerance of BVREF is specified in DC Parameter table and these same tolerance limits apply here.

### Error Amplifier

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current (Enabled)</td>
<td></td>
<td>2.3</td>
<td>3.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Supply Current (Standby)</td>
<td>54</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>Gain Bandwidth product</td>
<td>25</td>
<td>-</td>
<td>65</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Input Common Mode Range</td>
<td>26</td>
<td>1.1</td>
<td>1.6</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>Input bias Current</td>
<td>-</td>
<td>1.6</td>
<td>4.5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>-</td>
<td>38</td>
<td>-</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>25</td>
<td>-</td>
<td>32</td>
<td>-</td>
<td>V/µs</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>27</td>
<td>-</td>
<td>-</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>Input Referred Noise Voltage</td>
<td>28</td>
<td>-</td>
<td>5</td>
<td>10</td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>Intermodulation products</td>
<td>24, 29a</td>
<td>-</td>
<td>-90</td>
<td>-</td>
<td>dBC</td>
</tr>
<tr>
<td>Intermodulation products</td>
<td>24, 29b</td>
<td>-</td>
<td>-90</td>
<td>-</td>
<td>dBC</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>24</td>
<td>AVss + 0.2</td>
<td>-</td>
<td>AVdd – 0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

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Notes:  
24. Typical loads are 150 ohms and 33nF in series or 150 ohms and 100nF in series.  
25. With a load of 150 Ohms in series with 100 nF. (Note 17 also applies).  
26. For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the reference voltage setting.  
27. The inputs are protected with diodes. These diodes prevent the inadvertent appliance of voltages that may cause damage to the input transistors.  
28. Measured at 10kHz.  
29a. Measured with respect to an output signal level of 0.4V pk-pk for each tone of a two-tone signal with 7kHz and 9kHz tones and with a load of 150 Ohms in series with 33nF. Amplifier configured as a voltage follower. (Note 17 also applies).  
29b. Also measured with same conditions but with 70kHz and 90kHz tones with a load of 100 Ohms in series with 10nF. (Note 17 also applies).  

<table>
<thead>
<tr>
<th>Input Amplifiers and Filter Amplifiers</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current (Enabled) per amplifier</td>
<td>-</td>
<td>0.7</td>
<td>0.9</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply Current (Standby) per amplifier</td>
<td>54</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>30</td>
<td>-</td>
<td>10</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Input Common Mode Range</td>
<td>32</td>
<td>1.0</td>
<td>1.6</td>
<td>2.5</td>
<td>V p-p</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>-</td>
<td>0.4</td>
<td>-</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>-</td>
<td>160</td>
<td>-</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>30</td>
<td>-</td>
<td>6</td>
<td>-</td>
<td>V/µs</td>
</tr>
<tr>
<td>IMD</td>
<td>30, 31, 34</td>
<td>-</td>
<td>-85</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>33</td>
<td>-</td>
<td>-</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>Input Referred Noise at 1kHz,</td>
<td>-</td>
<td>15</td>
<td>-</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>Output Load</td>
<td>17</td>
<td>1kΩ</td>
<td></td>
<td>100pF</td>
<td>-</td>
</tr>
<tr>
<td>DC Output Range</td>
<td>AV_{ss}+0.1</td>
<td>-</td>
<td>AV_{dd}-0.1</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Notes:  
30. With a load of 1kΩ in parallel with 100pF. (Note 17 also applies).  
31. Includes all IMD products up to and including the 7th order products e.g. 2nd, 3rd, 5th etc. Specification limit applies to each IMD product, not composite power of all products.  
32. For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the setting of the reference voltage.  
33. The inputs are protected with diodes. These diodes prevent the inadvertent appliance of voltages that may cause damage to the input transistors.  
34. Two-tone test with value measured relative to power in either tone, unity gain, 0.8V p-p signal with two tones at 70kHz and 90kHz (400mV p-p each tone).
<table>
<thead>
<tr>
<th>Instability Detector</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current from Vcc (Enabled)</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply current from VDREF (Enabled)</td>
<td>-</td>
<td>120</td>
<td>-</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Supply current from BVREF (Enabled)</td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Supply Current (from all sources) (Standby)</td>
<td>54</td>
<td>-</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

**1st stage (Filter amplifier)**

- Gain (internally configured as voltage follower): - 0 - dB
- All other characteristics (see section "Input Amplifiers and Filter Amplifiers")

**2nd Stage (Detector)**

- Attack Time to 90%: 44 | -100 | - | µs |
- Input Offset Voltage: -20 | - | +20 | mV |
- Input Common Mode Range: 41 | 1.1 | 1.6 | 2.1 | V |
- Input Bias Current: - | 10 | - | nA |
- Input Resistance: - | 100 | - | MΩ |
- AC Gain: 42, 44 | 6, 12, 18, 24 | - | dB |
- Voltage out when no signal present: - | VDref/2 | - | V |
- Maximum voltage out: - | VDref | - | V |
- Output Load: 43 | 470kΩ //47nF | - |

Notes:

40. The function of the detector is to follow the maximum peaks of the input voltage waveform. The ability to this is frequency dependent, which in turn, is dependent on the choice of external capacitor.

41. For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the setting of the reference voltage.

42. Amplifier gain configurable in 4 nominal steps.

43. The time constant of the peak detector can be controlled by a parallel resistor and capacitor on the output (Pin PDO). If a purely resistive load is used, the minimum resistor value is 10kΩ.

44. Measured at 1MHz. The attack time is dependant on external component values. This specified time is based on the use of typical configurations, shown in section 4.5.

<table>
<thead>
<tr>
<th>RF Detector</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power Range</td>
<td>58</td>
<td>-</td>
<td>+10, -6</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Nominal Input Power (PEP)</td>
<td>51</td>
<td>-</td>
<td>-22</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Scale</td>
<td>50</td>
<td>-</td>
<td>10</td>
<td>-</td>
<td>V/V p-p</td>
</tr>
<tr>
<td>Vdco</td>
<td>59</td>
<td>-</td>
<td>VDref/2</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>52</td>
<td>100</td>
<td>-</td>
<td>1000</td>
<td>MHz</td>
</tr>
<tr>
<td>Output SINAD</td>
<td>53</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Output bandwidth (3dB)</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Output load</td>
<td>-</td>
<td>100</td>
<td>-</td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>
50. With feedback path attenuator set to 0dB.
51. PEP Input level assuming TETRA \(\pi/4\)-DQPSK modulation or 2-tone signal.
52. Operation to 100MHz but RF Detector performance parameters are not guaranteed between 100MHz and 300MHz.
53. Measured with 400MHz signal having 1kHz, 30% AM modulation at –15dBm input to the down-converter, 0dB feedback path attenuation, 300Hz to 3.4kHz measurement bandwidth.
54. At Tcase = 25ºC, not including any current drawn from the CMX998 pins by external circuitry.
55. For Tcase = +15 to +55ºC. (This represents nominal equipment operating conditions of +15 to +35ºC ambient with 20ºC added to the higher temperature to allow for Tcase rise over the equipment ambient.)
56. This is the impedance that should be presented to the output of the CMX998 up-converter, e.g. using a balun as shown in Figure 3. The precise load impedance may be optimised for a given operating frequency, or band of frequencies, to achieve improved output level and signal-to-noise.
57. With a spurious-free LO input and specified output level.
58. The typical input power range is –12dBm PEP (i.e. –22dBm + 10dB) to –28dBm PEP (i.e. –22dBm – 6dB).
59. Vdco is the nominal voltage that would be measured at the detector output with no RF input applied.

<table>
<thead>
<tr>
<th>C-BUS Timings (See Figure 12)</th>
<th>Notes</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{CSE})</td>
<td>CSN-Enable to Clock-High time</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CSH})</td>
<td>Last Clock-High to CSN-High time</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LOZ})</td>
<td>Clock-Low to Reply Output enable time</td>
<td>0.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{HIZ})</td>
<td>CSN-High to Reply Output 3-state time</td>
<td>-</td>
<td>-</td>
<td>1.0</td>
<td>µs</td>
</tr>
<tr>
<td>(t_{COFF})</td>
<td>CSN-High Time between transactions</td>
<td>1.0</td>
<td>-</td>
<td>-</td>
<td>µs</td>
</tr>
<tr>
<td>(t_{NXT})</td>
<td>Inter-Byte Time</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CK})</td>
<td>Clock-Cycle time</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CH})</td>
<td>Serial Clock (SCK) - High time</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CL})</td>
<td>Serial Clock (SCK) - Low time</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CDS})</td>
<td>Command Data (SDI) - Set-Up time</td>
<td>75.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CDH})</td>
<td>Command Data (SDI) - Hold time</td>
<td>25.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{RDS})</td>
<td>Reply Data (SDO) - Set-Up time</td>
<td>50.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{RDH})</td>
<td>Reply Data (SDO) - Hold time</td>
<td>0.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

Maximum 30pF load on each C-BUS interface line.
Figure 12 C-BUS Timing
7.2 Packaging

The underside of the package has an exposed metal pad which can be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required.

Note:
In this device, the underside of the Q1 package should be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.

Figure 13 Q1 Mechanical Outline: Order as part no. CMX998Q1

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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For detailed application notes: www.cmlmicro.com/products/applications/