MP39

FEATURES

- HIGH INTERNAL DISSIPATION — 125 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 100V, 10A
- HIGH SLEW RATE — 10V/µS
- 4 WIRE CURRENT LIMIT SENSING
- OPTIONAL BOOST VOLTAGE INPUTS

APPLICATIONS

- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±45V
- INDUSTRIAL AUDIO
- PACKAGE OPTION - DIP10 - DUAL-IN-LINE

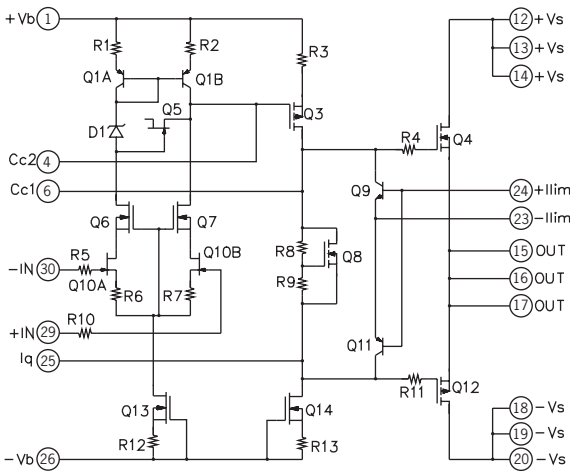
DESCRIPTION

The MP39 is a cost-effective high voltage MOSFET power operational amplifier constructed with surface mount components on a thermally conductive but electrically isolated substrate.

While the cost is low the MP39 offers many of the same features and performance specifications found in much more expensive hybrid power amplifiers.

The metal substrate allows the MP39 to dissipate power up to 125 watts and its power supply voltages can range up to +/- 50 Volts (100V total). Optional boost voltage inputs allow the small signal portion of the amplifier to operate at higher supply voltages than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high current for extra efficient operation. External compensation tailors performance to the user needs. A four-wire sense technique allows current limiting without the need to consider internal or external mili-ohm parasitic resistance in the output line. An Iq pin is available which can be used to shut off the quiescent current in the output stage. The output stage then operates class C and lowers quiescent power dissipation. This is useful in applications where output crossover distortion is not important.

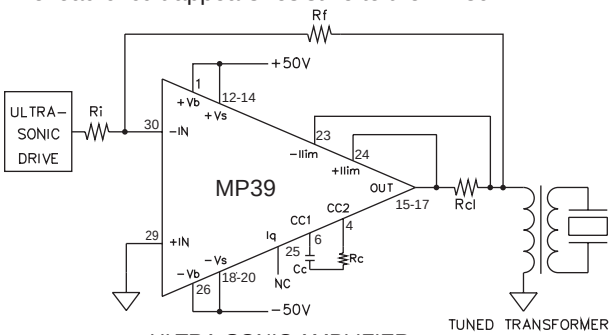
EQUIVALENT SCHEMATIC



OPEN FRAME PACKAGE (MP39CL)

TYPICAL APPLICATION Ref: Application Note 25

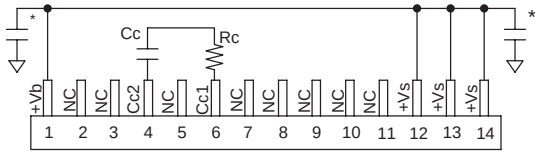
The high power bandwidth and high voltage output of the MP39 allows driving ultra-sonic transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the MP39.



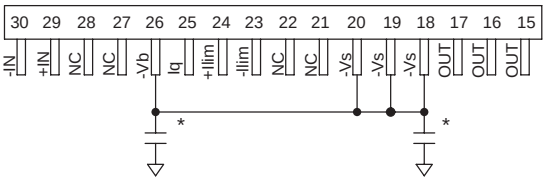
ULTRA-SONIC AMPLIFIER

EXTERNAL CONNECTIONS - MP39CL

PACKAGE: DIP10



COMPONENT SIDE VIEW



* SEE "BYPASSING" PARAGRAPH

Phase Compensation

Gain	Cc	Rc
1	470pF	100Ω
≥ 3	220pF	Short
≥ 10	100pF	Short

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
BOOST VOLTAGE	$\pm V_S$ ±20V
OUTPUT CURRENT, within SOA	25A
POWER DISSIPATION, internal	125W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_B$
TEMPERATURE, pin solder - 10s	200°C
TEMPERATURE, junction[2]	175°C
TEMPERATURE, storage	–40 to +105°C
OPERATING TEMPERATURE RANGE, case	–40 to +85°C

SPECIFICATIONS

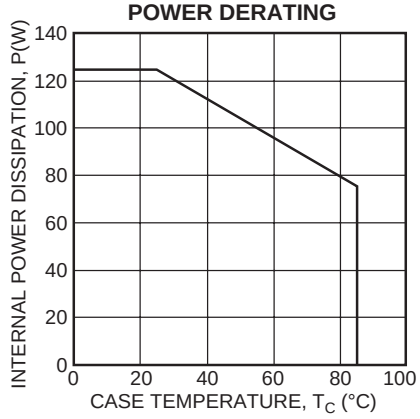
PARAMETER	TEST CONDITIONS[1]	MP39 MIN	MP39 TYP	MP39 MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			5	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50	µV/°C
OFFSET VOLTAGE, vs. supply			15		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30		µV/W
BIAS CURRENT, initial			10	200	pA
BIAS CURRENT, vs. supply			.01		pA/V
OFFSET CURRENT, initial			10	50	pA
INPUT IMPEDANCE, DC			10^{10}		Ω
INPUT CAPACITANCE			20		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B$ ∓15	$\pm V_B$ ∓12		V
COMMON MODE REJECTION, DC	Full temp, range, V_{CM}= ±20V	86	98		dB
INPUT NOISE	100kHz BW, R_S = 1KΩ		10		µVrms
GAIN					
OPEN LOOP, @15Hz	Full temperature range, C_C = 100pF	94	102		db
GAIN BANDWIDTH PRODUCT	I_O=10A		2		MHz
POWER BANDWIDTH	R_L=10Ω, V_O = 90V p-p C_C = 100pF		40		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING	I_O=10A	$\pm V_S$ ∓ 8.8	$\pm V_S$ ∓7.5		V
VOLTAGE SWING	$\pm V_B$ = $\pm V_S$ ±10V, I_O=10A	$\pm V_S$ ∓ 6.8	$\pm V_S$ ∓5.5		V
SETTLING TIME to .1%	A_V=+1,10V step, R_L =4Ω		2.5		µs
SLEW RATE	A_V= –10, C_C= 100pF	10			V/µs
CAPACITIVE LOAD	Full temperature range, A_V=+1	10			nF
RESISTANCE			4		Ω
CURRENT, CONTINUOUS				10	A
POWER SUPPLY					
VOLTAGE	Full temperature range	±15	±40	±50	V
CURRENT, quiescent, boost supply				22	mA
CURRENT, quiescent, total				26	mA
THERMAL					
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz			.9	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz			1.2	°C/W
RESISTANCE[4], junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-40		85	°C

NOTES:

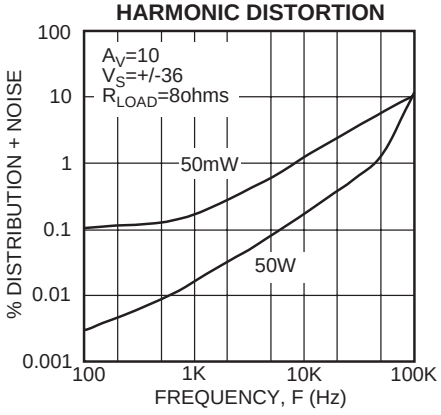
1. Unless otherwise noted: T_C = 25°C, C_C = 100Ω, R_C = 470pF. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_B$ = $\pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The MP39 must be used with a heat sink or the quiescent power may drive the unit to junction temperatures higher than 175°C.

CAUTION The MP39 is constructed from MOSFET transistors. ESD handling procedures must be observed.

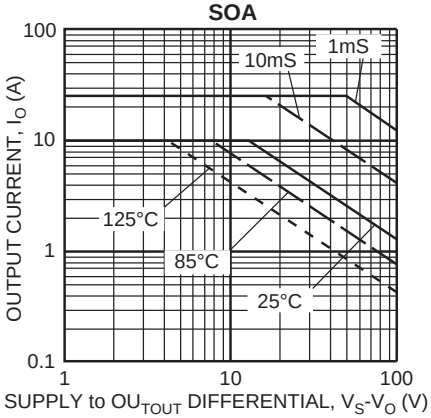
POWER DERATING



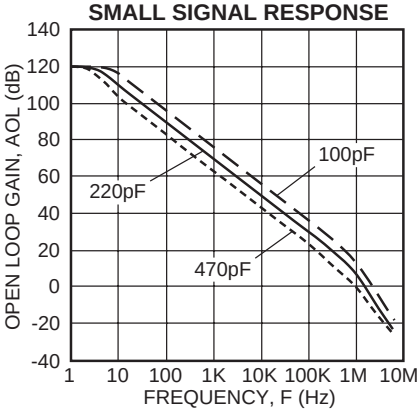
HARMONIC DISTORTION



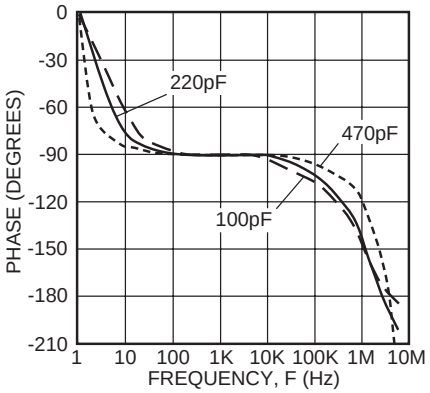
SOA



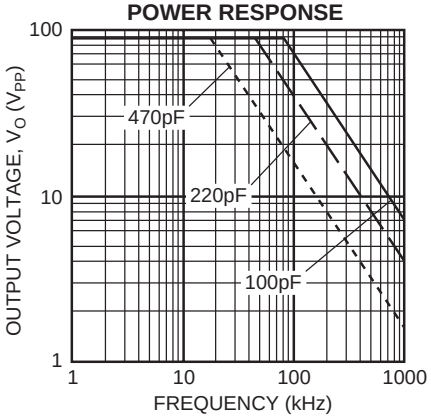
SMALL SIGNAL RESPONSE



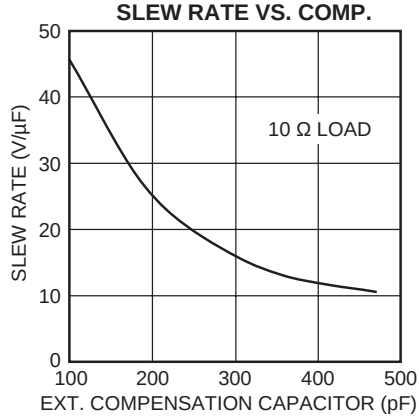
PHASE RESPONSE



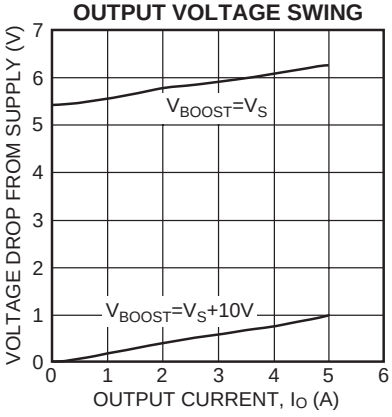
POWER RESPONSE



SLEW RATE VS. COMP.



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. **For the current limit to work correctly pin 24 must be connected to the amplifier output side and pin 23 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.** This connection will bypass any parasitic resistances, Rp, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.7}{I_{LIMIT}}$$

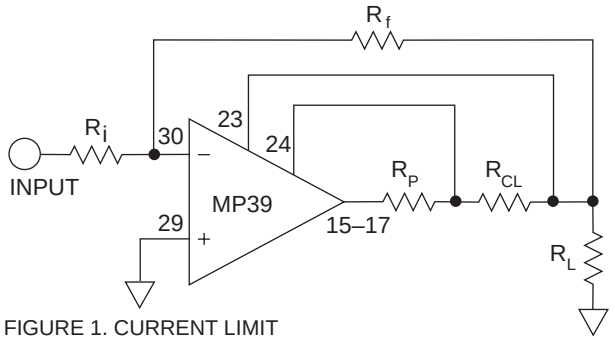


FIGURE 1. CURRENT LIMIT

BOOST OPERATION

With the V_B feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_S$ (pins 12-14) and $-V_S$ (pins 18-20) are connected to the high current output stage. An additional 10V on the V_B pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swing to the supply rails is not required the $+V_B$ and $+V_S$ pins must be strapped together as well as the $-V_B$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

BYPASSING

Proper bypassing of the power supply pins is crucial for proper operation. Bypass the ±Vs pins with a aluminum electrolytic capacitor with a value of at least 10µF per amp of expected output current. In addition a .47µF to 1µF ceramic capacitor should be placed in parallel with each aluminum electrolytic capacitor. Both of these capacitors have to be placed as close to the power supply pins as physically possible. If not connected to the Vs pins (See BOOST OPERATION) the V_B pins should also be bypassed with a .47µF to 1µF ceramic capacitor.

USING THE Iq PIN FUNCTION

Pin 25 (Iq) can be tied to pin 6 (Cc1) to eliminate the class AB biasing current from the output stage. Typically this would remove 1-4 mA of quiescent current. The resulting decrease in quiescent power dissipation may be important in some applications. Note that implementing this option will raise the output impedance of the amplifier and increase crossover distortion as well.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 4 and 6. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate.

APPLICATION REFERENCES

For additional technical information please refer to the following application notes.

AN 1 General Operating Considerations
AN 11 Thermal Techniques
AN 38 Loop Stability with Reactive Loads

