

# Linear IC converter

CMOS

## D/A Converter for Digital Tuning (8-channel, 8-bit, on-chip OP amp, low-voltage)

### MB88347L

#### ■ DESCRIPTION

The MB88347L incorporates eight 8-bit D/A converter modules. This device operates at low supply voltage in the performance guarantee range from 2.7 to 3.6 V. It also contains an output amplifier, allowing driving at large current.

Since the MB88347L inputs data in serial mode, it requires only three control lines for data input and two or more MB88347L units can be cascaded.

The MB88347L is function and pin compatible with the MB88347 (5-volt supply voltage model). The MB88347L can therefore easily replace the MB88347 in a system, thereby reducing the system's voltage requirement.

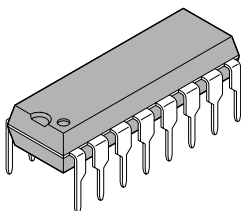
The MB88347L is the best replacement for electronic variable resistors or screwdriver control resistors.

#### ■ FEATURES

- Ultra-low power consumption (0.5 mW/ch: typical)
- Low voltage operation ( $V_{CC} = 2.7$  to  $3.6$  V)
- Ultra-compact space-saving package (SSOP-16)
- Contains 8-channel R-2R type 8-bit D/A converter
- On-chip analog output amps (sink current max. 1.0 mA, source current max. 1.0 mA)
- Analog output range from 0 V to  $V_{CC}$
- Two separate power supply/ground lines for MCU interface block/operational amplifier output buffer block and D/A converter block
- Serial data input, maximum operating speed 2.5 MHz
- CMOS process
- Package lineup includes DIP 16-pin, SOP 16-pin, SSOP 16-pin

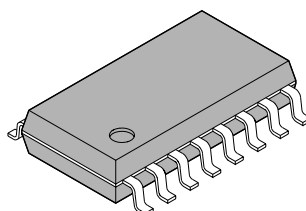
#### ■ PACKAGES

16 pin, Plastic DIP



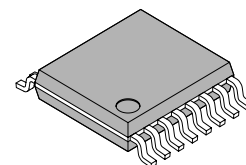
(DIP-16P-M04)

16 pin, Plastic SOP



(FPT-16P-M06)

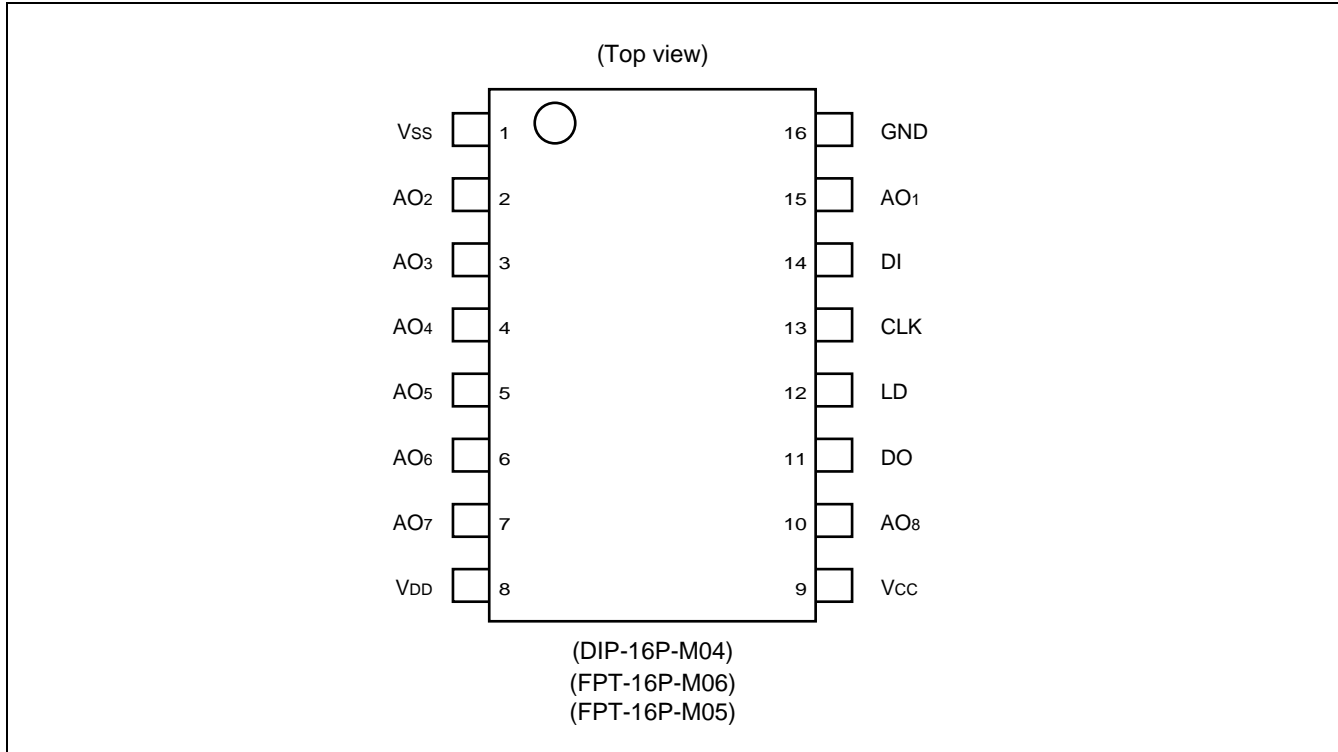
16 pin, Plastic SSOP



(FPT-16P-M05)

# MB88347L

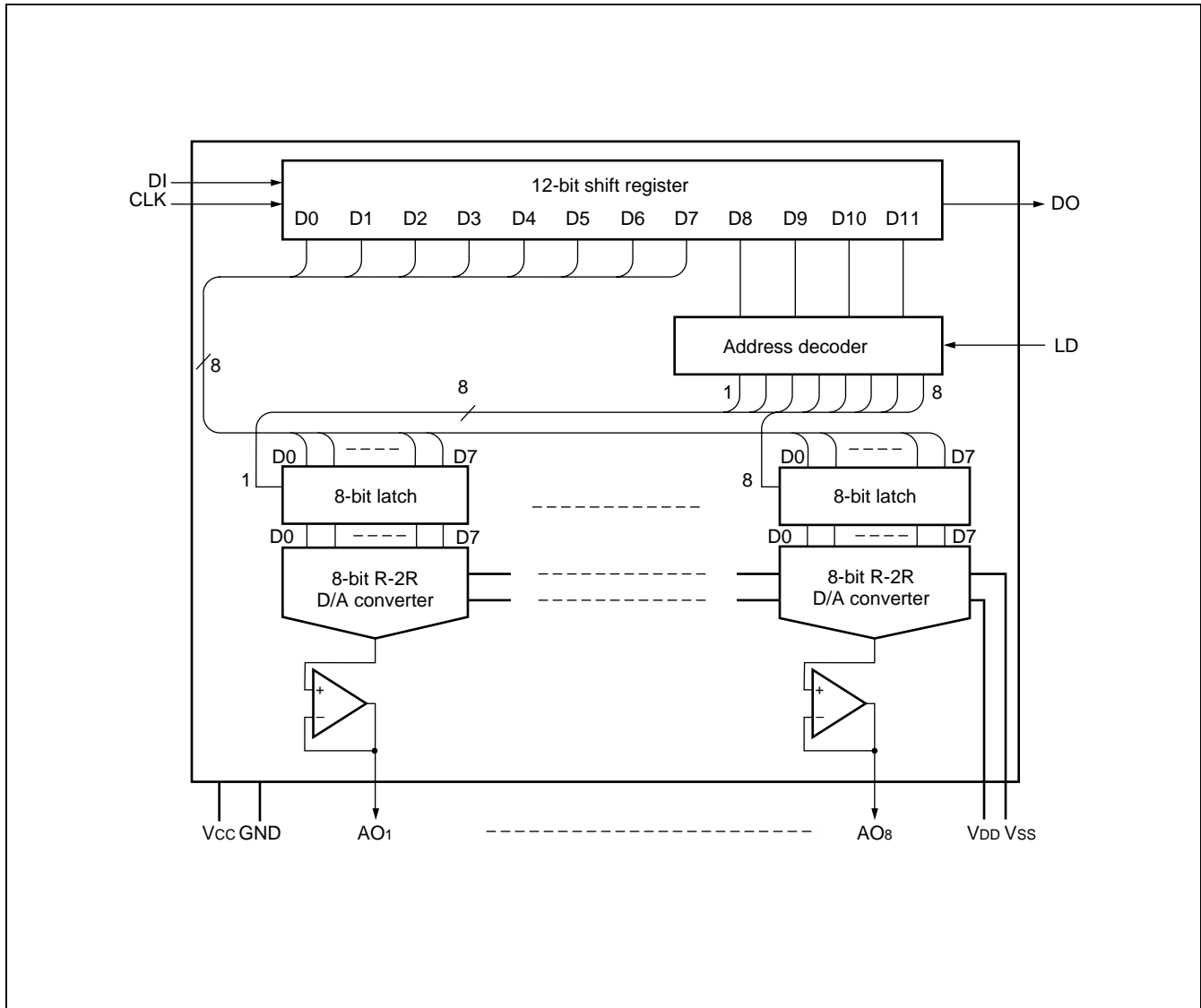
## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Functions
14	DI	I	Serial data input pin. This pin inputs serial data with a data length of 12 bits. (Do not leave the pin floating.)
11	DO	O	This pin outputs the MSB data in the 12-bit shift register at the CLK falling edge.
13	CLK	I	Shift clock input pin. The input signal from the DI pin enters the 12-bit shift register at the rising edge of the shift clock pulse. (Do not leave this pin floating.)
12	LD	I	When the LD pin inputs the High-level signal, shift register value is loaded to the decoder and the D/A output register. (Do not leave this pin floating. When data is not transferred, fix the pin to the "Low" level.)
15 2 3 4 5 6 7 10	AO <sub>1</sub> AO <sub>2</sub> AO <sub>3</sub> AO <sub>4</sub> AO <sub>5</sub> AO <sub>6</sub> AO <sub>7</sub> AO <sub>8</sub>	O	8-bit D/A output with op amp.
9	V <sub>CC</sub>	—	MCU interface and OP amp power-supply pin.
16	GND	—	MCU interface and OP amp GND pin.
8	V <sub>DD</sub>	—	D/A converter reference power (High) input pin.
1	V <sub>SS</sub>	—	D/A converter reference power (Low) input pin.

## ■ BLOCK DIAGRAM



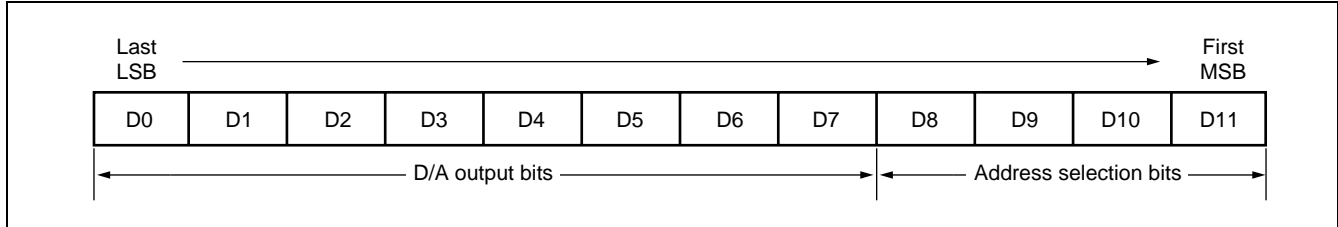
# MB88347L

## ■ DATA CONFIGURATION

The MB88347L has a 12-bit shift register for chip control.

The 12-bit shift register must be used to set up data in the configuration shown below.

The data configuration has a total of 12 bits, for address selection and eight for D/A data output.



### • D/A converter control signals

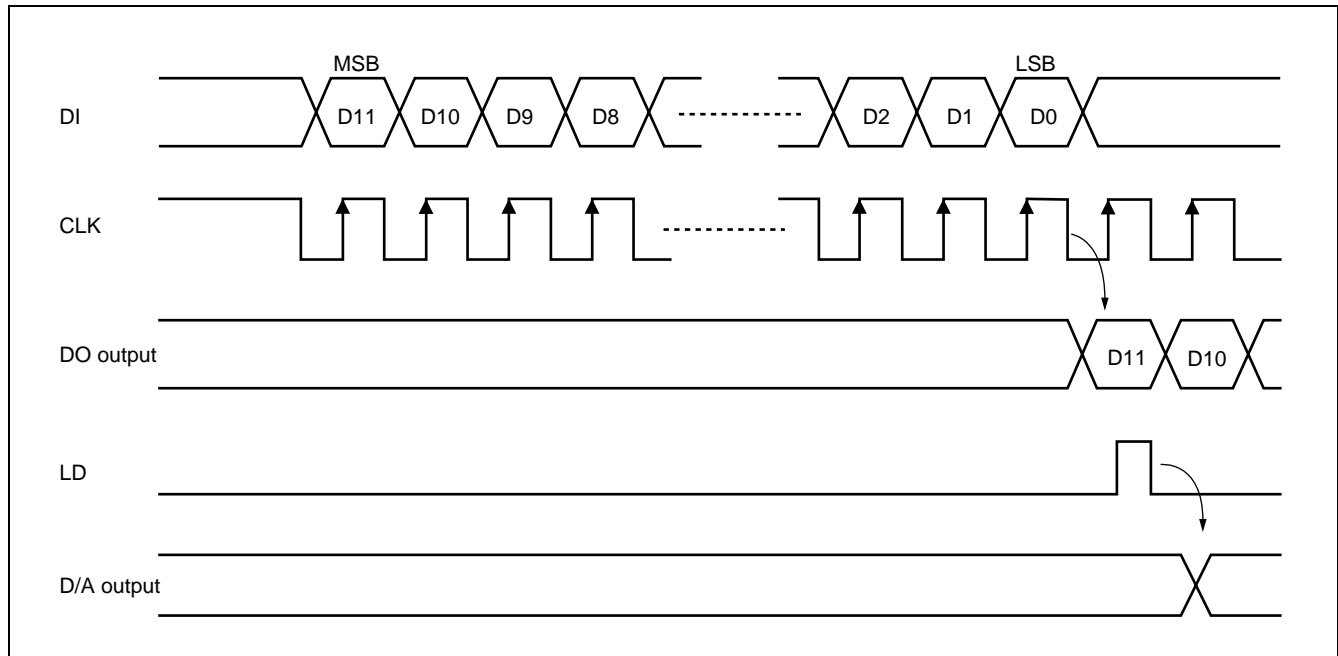
D0	D1	D2	D3	D4	D5	D6	D7	D/A data output
0	0	0	0	0	0	0	0	$\equiv V_{SS}$
1	0	0	0	0	0	0	0	$\equiv V_{LB} \times 1 + V_{SS}$
0	1	0	0	0	0	0	0	$\equiv V_{LB} \times 2 + V_{SS}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$\equiv V_{LB} \times 254 + V_{SS}$
1	1	1	1	1	1	1	1	$\equiv V_{LB} \times 255 + V_{SS}$

Note:  $V_{LB} = (V_{DD} - V_{SS})/256$

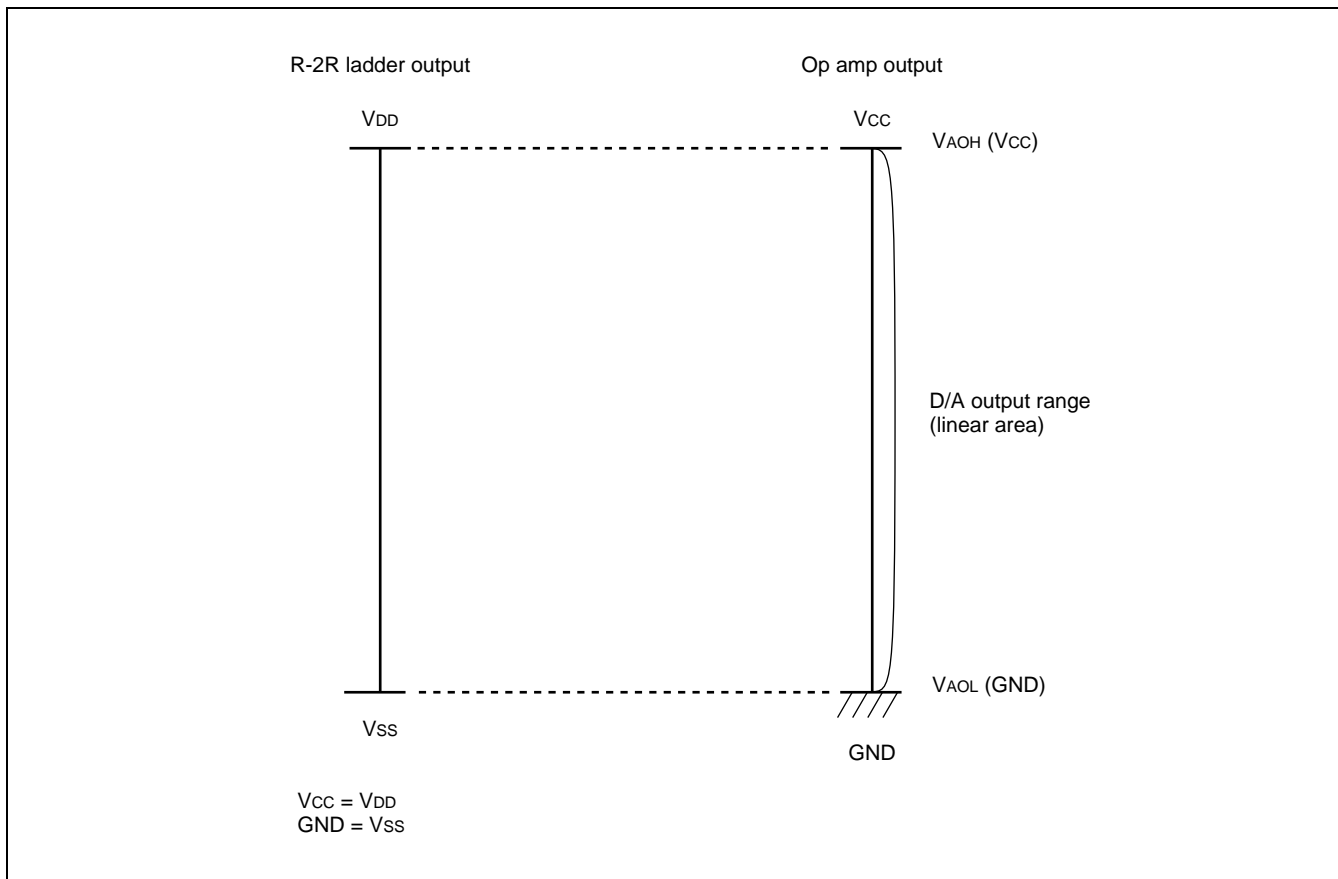
### • Address selection signals

D8	D9	D10	D11	Address selection
0	0	0	0	Don't Care
0	0	0	1	AO <sub>1</sub> Selection
0	0	1	0	AO <sub>2</sub> Selection
0	0	1	1	AO <sub>3</sub> Selection
0	1	0	0	AO <sub>4</sub> Selection
0	1	0	1	AO <sub>5</sub> Selection
0	1	1	0	AO <sub>6</sub> Selection
0	1	1	1	AO <sub>7</sub> Selection
1	0	0	0	AO <sub>8</sub> Selection
1	0	0	1	Don't Care
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

## DATA SETTING TIMING CHART



## ANALOG OUTPUT VOLTAGE RANGE



# MB88347L

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Supply voltage	V <sub>CC</sub>	Based on GND Ta = +25°C	-0.3	5.0	V
	V <sub>DD</sub>		-0.3*	5.0*	V
Input voltage	V <sub>IN</sub>		-0.3	V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>		-0.3	V <sub>CC</sub> + 0.3	V
Power consumption	P <sub>D</sub>	—	—	250	mW
Operating temperature	Ta	—	-20	+85	°C
Storage temperature	T <sub>stg</sub>	—	-55	+150	°C

\* : V<sub>CC</sub> ≥ V<sub>DD</sub>

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage 1	V <sub>CC</sub>	—	2.7	3.6	V
	GND	—	Typical: 0		V
Power supply voltage 2	V <sub>DD</sub>	V <sub>DD</sub> - V <sub>SS</sub> ≥ 2.0 V	2.0	V <sub>CC</sub>	V
	V <sub>SS</sub>		GND	V <sub>CC</sub> - 2.0	V
Analog output source current	I <sub>AL</sub>	V <sub>CC</sub> = 3.0 V	—	1.0	mA
Analog output sink current	I <sub>AH</sub>	V <sub>CC</sub> = 3.0 V	—	1.0	mA
Oscillation limit output capacity	C <sub>OL</sub>	—	—	1.0	μF
Digital data value range	—	—	#00	#FF	—
Operating temperature	Ta	—	-20	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

#### (1) Digital block

( $V_{DD}, V_{CC} = 2.7\text{ V to }3.6\text{ V}$  ( $V_{CC} \geq V_{DD}$ ), GND,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	$V_{CC}$	$V_{CC}$	—	2.7	3.0	3.6	V
Power supply current 1	$I_{CC}$		Operation at CLK = 1 MHz (with no load)	—	0.8	2.0	mA
Input leak current	$I_{ILK}$	CLK DI LD	$V_{IN} = 0\text{ V to }V_{CC}$	-10	—	10	$\mu\text{A}$
L level input voltage	$V_{IL}$		—	—	—	$0.2 V_{CC}$	V
H level input voltage	$V_{IH}$		—	$0.8 V_{CC}$	—	—	V
L level output voltage	$V_{OL}$	DO	$I_{OL} = 2.5\text{ mA}$	—	—	0.4	V
H level output voltage	$V_{OH}$		$I_{OH} = -400\ \mu\text{A}$	$V_{CC} - 0.4$	—	—	V

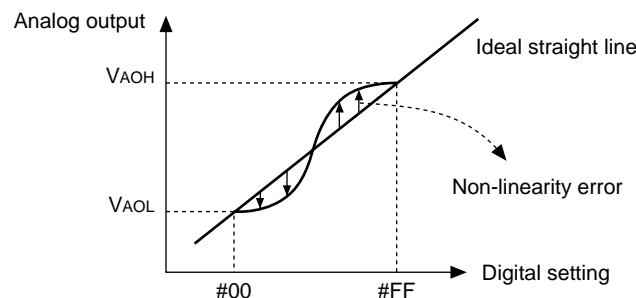
#### (2) Analog block (1)

( $V_{DD}, V_{CC} = 2.7\text{ V to }3.6\text{ V}$  ( $V_{CC} \geq V_{DD}$ ), GND,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power consumption	$I_{DD}$	$V_{DD}$	No load	—	0.6	1.0	mA
Analog voltage	$V_{DD}$	$V_{DD}$	$V_{DD} - V_{SS} \geq 2.0\text{ V}$	2.0	—	$V_{CC}$	V
	$V_{SS}$	$V_{SS}$		GND	—	$V_{CC} - 2.0$	V
Resolution	Res	AO <sub>1</sub> to AO <sub>8</sub>	—	—	8	—	bits
Monotonic increase	Rem		—	—	8	—	bits
Non-linearity error*1	LE		No load $V_{DD} \leq V_{CC} - 0.1\text{ V}$ $V_{SS} \geq 0.1\text{ V}$	-1.5	—	1.5	LSB
Differential linearity error*2	DLE		-1.0	—	1.0	LSB	

\*1: Deviation (error) in input/output curves with respect to an ideal straight line connecting output voltage at "00" and output voltage at "FF."

\*2: Deviation (error) in amplification with respect to theoretical increase in amplification per 1-bit increase in digital value.



Note: The value of  $V_{AOH}$  and  $V_{DD}$ , and the value of  $V_{AOL}$  and  $V_{SS}$  are not necessarily equivalent.

# MB88347L

## (3) Analog section (2)

(Ta = -20°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Values			Unit
				Min.	Typ.	Max.	
Output minimum voltage 1	VAOL1	AO <sub>1</sub> to AO <sub>8</sub>	V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AL</sub> = 0 μA Digital data = #00	V <sub>SS</sub>	—	V <sub>SS</sub> + 0.1	V
Output minimum voltage 2	VAOL2		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AL</sub> = 500 μA Digital data = #00	V <sub>SS</sub> - 0.2	V <sub>SS</sub>	V <sub>SS</sub> + 0.2	V
Output minimum voltage 3	VAOL3		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AH</sub> = 500 μA Digital data = #00	V <sub>SS</sub>	—	V <sub>SS</sub> + 0.2	V
Output minimum voltage 4	VAOL4		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AL</sub> = 1.0 mA Digital data = #00	V <sub>SS</sub> - 0.3	V <sub>SS</sub>	V <sub>SS</sub> + 0.3	V
Output minimum voltage 5	VAOL5		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AH</sub> = 1.0 mA Digital data = #00	V <sub>SS</sub>	—	V <sub>SS</sub> + 0.3	V
Output maximum voltage 1	VAOH1		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AL</sub> = 0 μA Digital data = #FF	V <sub>DD</sub> - 0.1	—	V <sub>DD</sub>	V
Output maximum voltage 2	VAOH2		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AL</sub> = 500 μA Digital data = #FF	V <sub>DD</sub> - 0.2	—	V <sub>DD</sub>	V
Output maximum voltage 3	VAOH3		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AH</sub> = 500 μA Digital data = #FF	V <sub>DD</sub> - 0.2	V <sub>DD</sub>	V <sub>DD</sub> + 0.2	V
Output maximum voltage 4	VAOH4		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AL</sub> = 1.0 mA Digital data = #FF	V <sub>DD</sub> - 0.3	—	V <sub>DD</sub>	V
Output maximum voltage 5	VAOH5		V <sub>DD</sub> = V <sub>CC</sub> = 3.0 V V <sub>SS</sub> = GND = 0.0 V I <sub>AH</sub> = 1.0 mA Digital data = #FF	V <sub>DD</sub> - 0.3	V <sub>DD</sub>	V <sub>DD</sub> + 0.3	V



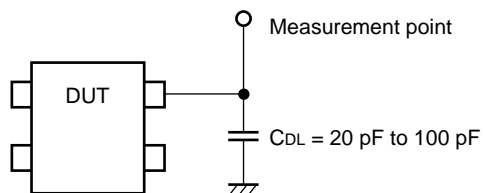
## 2. AC Characteristics

( $V_{DD}$ ,  $V_{CC} = 2.7\text{ V to }3.6\text{ V}$  ( $V_{CC} \geq V_{DD}$ ),  $GND$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20^\circ\text{C to }+85^\circ\text{C}$ )

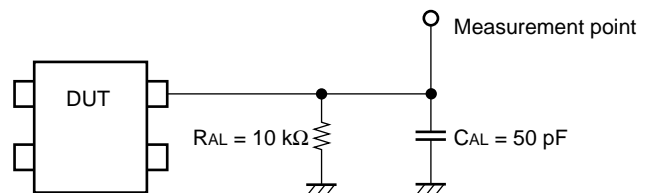
Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Clock L level pulse width	t <sub>CKL</sub>	—	200	—	ns
Clock H level pulse width	t <sub>CKH</sub>	—	200	—	ns
Clock rise time Clock fall time	t <sub>Cr</sub> t <sub>Cf</sub>	—	—	200	ns
Data setup time	t <sub>DCH</sub>	—	30	—	ns
Data hold time	t <sub>CHD</sub>	—	60	—	ns
Load setup time	t <sub>CHL</sub>	—	200	—	ns
Load hold time	t <sub>LDC</sub>	—	100	—	ns
Load H level pulse width	t <sub>LDH</sub>	—	100	—	ns
Data output delay time	t <sub>DO</sub>	See "Load conditions (1)."	—	170	ns
D/A output settling time	t <sub>LDD</sub>	See "Load conditions (2)."	—	200	μs

### Load conditions

- Load conditions (1)

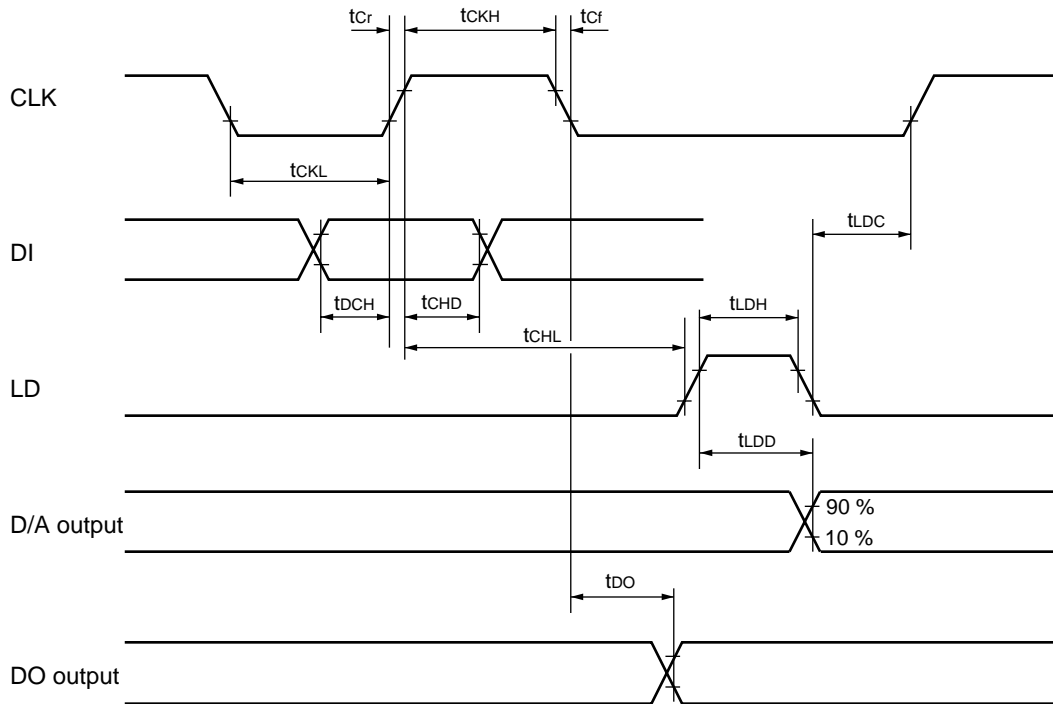


- Load conditions (2)



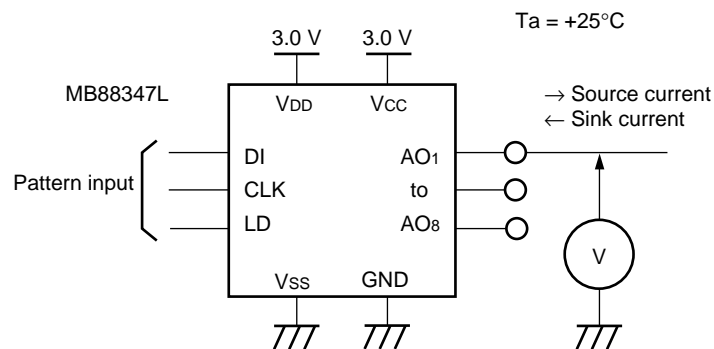
# MB88347L

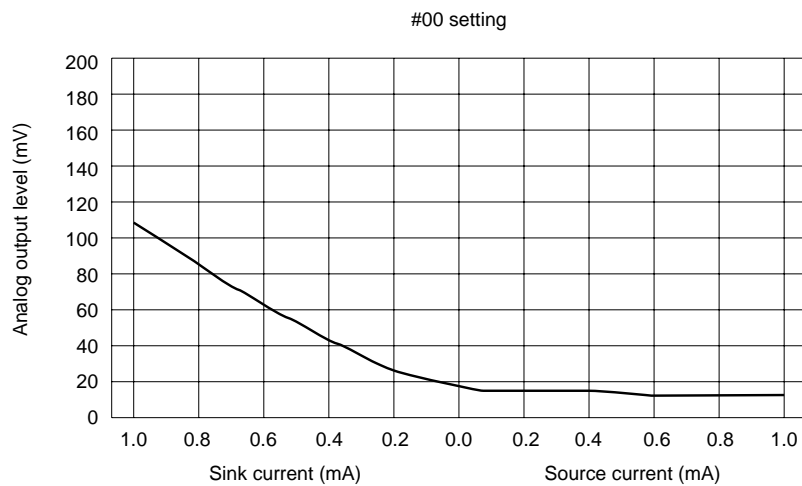
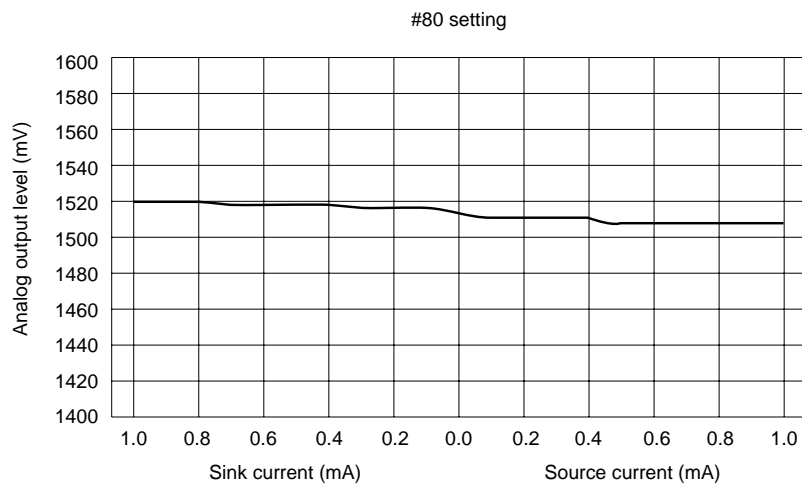
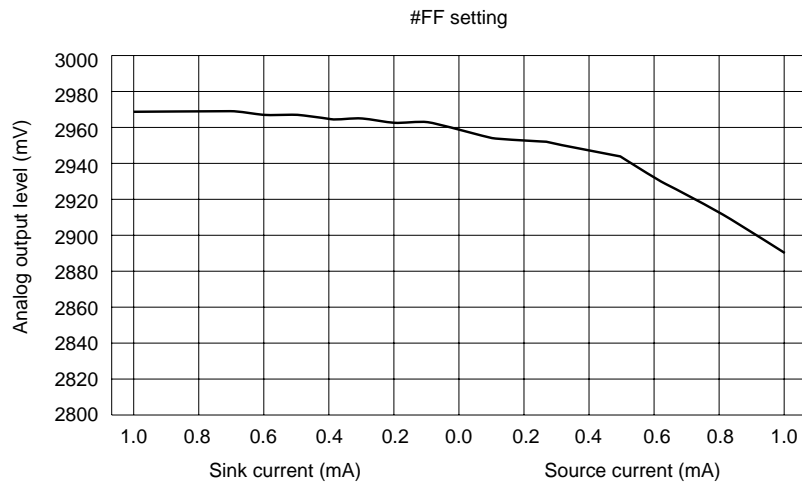
## Input/output timing



Note: Evaluation levels are 80% and 20% of  $V_{CC}$ .

## ■ $V_{AO}$ vs. $I_{AO}$ CHARACTERISTICS: EXAMPLE





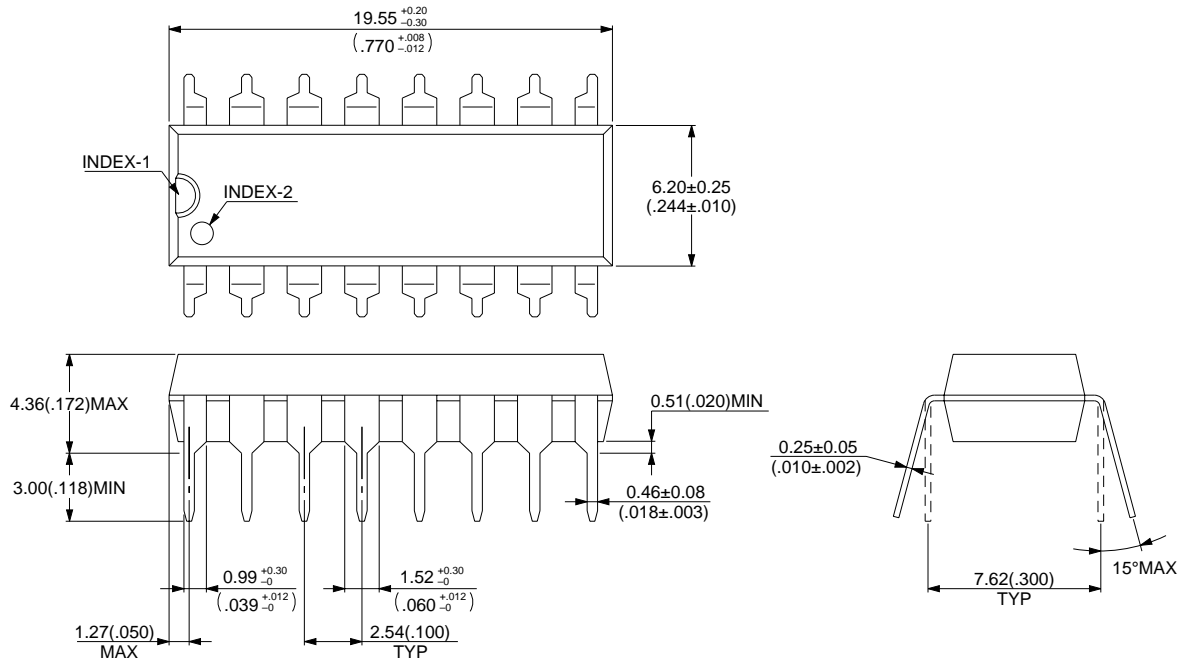
# MB88347L

## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB88347LP	16 pin, Plastic DIP (DIP-16P-M04)	
MB88347LPF	16 pin, Plastic SOP (FPT-16P-M06)	
MB88347LPFV	16 pin, Plastic SSOP (FPT-16P-M05)	

## ■ PACKAGE DIMENSIONS

16 pin, Plastic DIP  
(DIP-16P-M04)



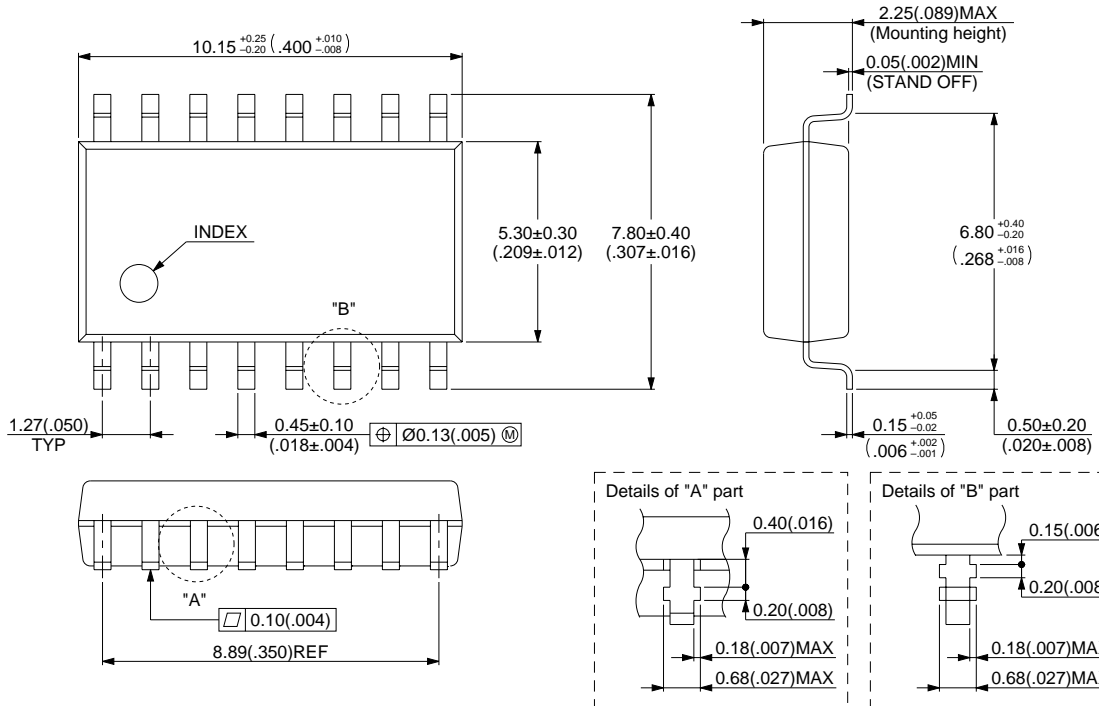
Dimensions in mm (inches).

© 1994 FUJITSU LIMITED D16033S-2C-3

(Continued)

# MB88347L

16 pin, Plastic SOP  
(FPT-16P-M06)



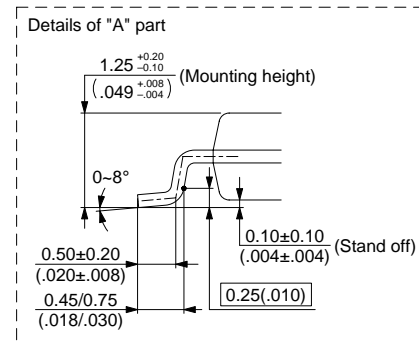
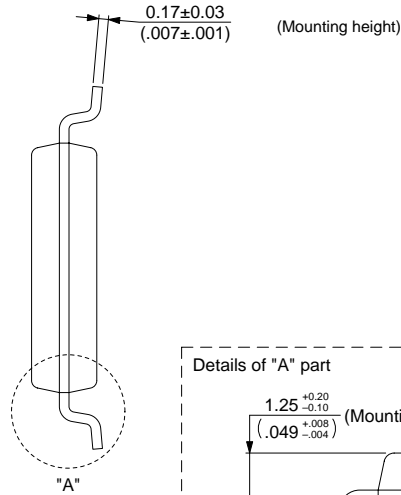
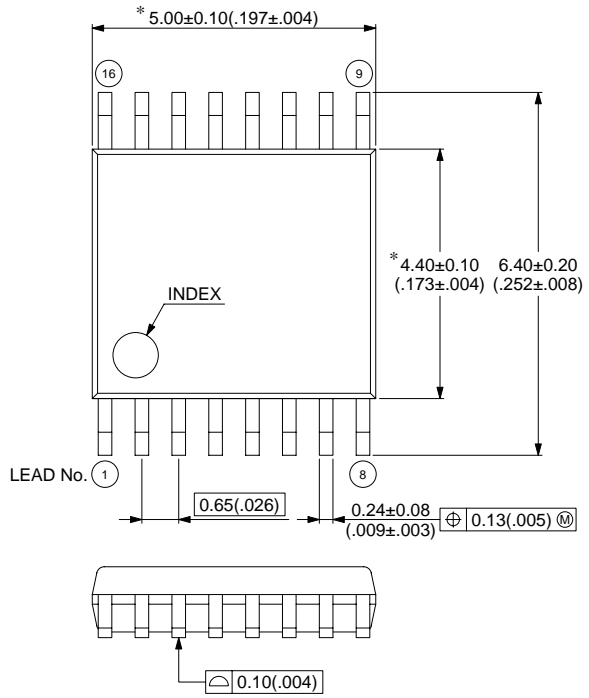
Dimensions in mm (inches).

© 1994 FUJITSU LIMITED F16015S-2C-4

(Continued)

16 pin, Plastic SSOP  
(FPT-16P-M05)

Note 1) \*: These dimensions do not include resin protrusion.  
Note 2) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).

## FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0001

© FUJITSU LIMITED Printed in Japan