

MB1508

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER ON CHIP 2.5 GHz PRESCALER

DESCRIPTION

The Fujitsu MB1508 with an on chip 2.5 GHz dual modulus prescaler is a serial input PLL (Phase Locked Loop) frequency synthesizer with pulse swallow function. It is well suited for BS tuner, CATV system, and TV tuner applications.

It operates with a supply voltage of 5.0V typ. and dissipates 16mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

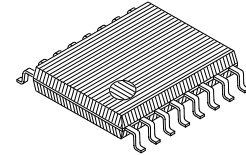
FEATURES

- Power supply voltage: $V_{CC} = 4.5$ to $5.5V$
- High operating frequency: $f_{IN} = 2.5$ GHz ($P_{IN} = -4dBm$)
- 2.5 GHz dual modulus prescaler: $P = 256/272, 512/528$
- Low supply current: $I_{CC} = 16mA$ typ.
- Programmable reference divider consisting of:
Binary 2-bit programmable reference counter ($R = 256, 512, 1024, 2048$)
- Programmable divider consisting of:
Binary 5-bit swallow counter ($A = 0$ to 31)
Binary 12-bit programmable counter ($N = 32$ to 4095)
- Wide operating temperature: $-40^{\circ}C$ to $+85^{\circ}C$
- Plastic 20-pin Flat Package (Suffix: —PF)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

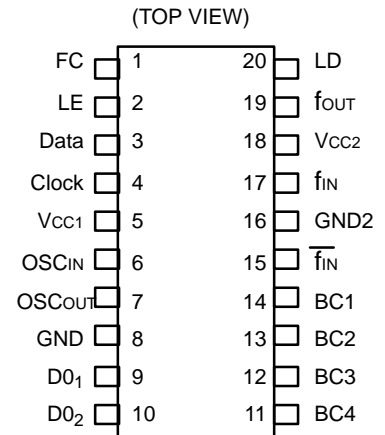
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to $+7.0$	V
Output Voltage	V_O	-0.5 to $V_{CC} + 0.5$	V
Output Current	I_O	± 10	mA
Storage Temperature	T_{STG}	-55 to $+125$	$^{\circ}C$

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

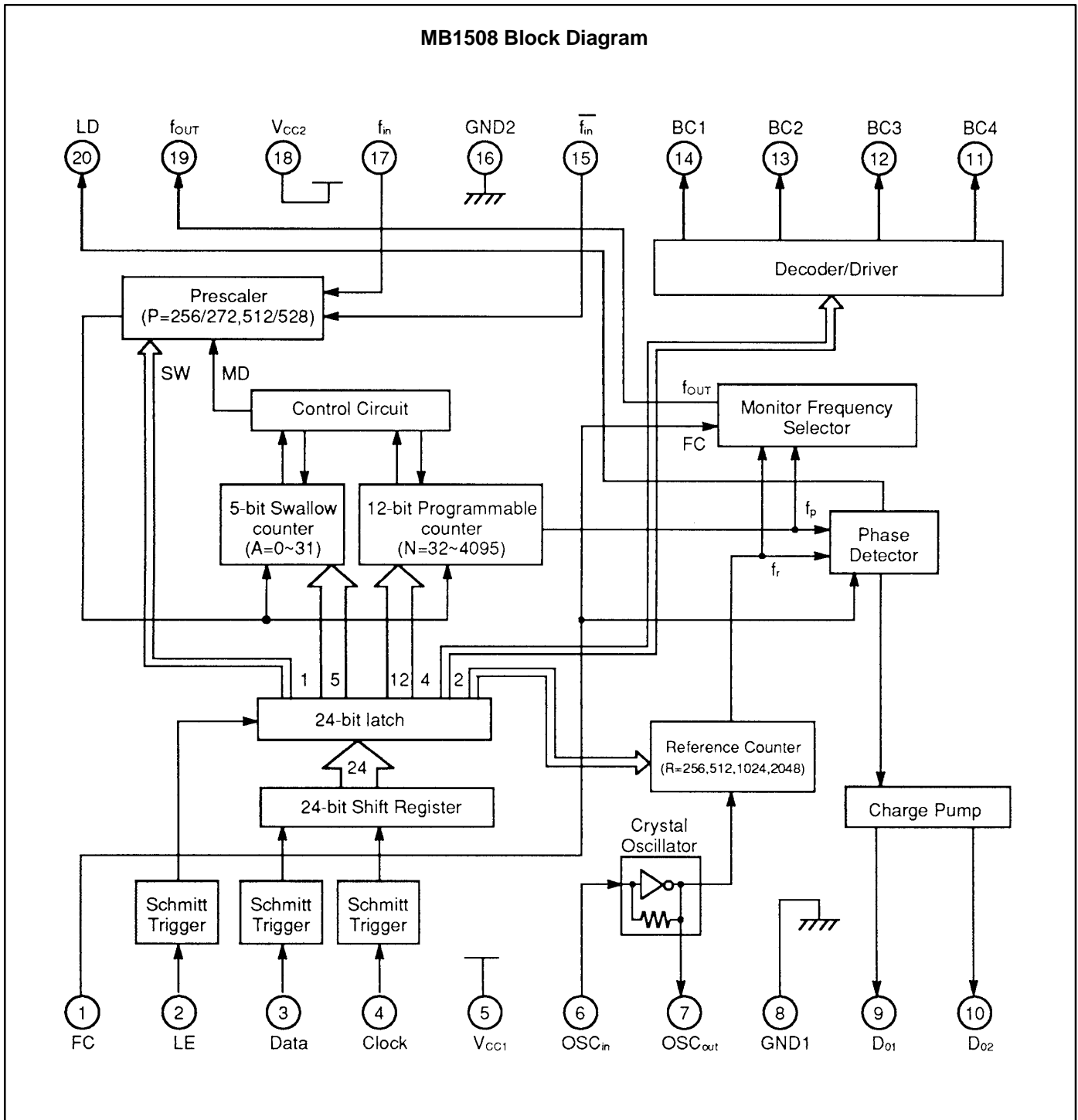


Plastic Package
FPT-20P-M01

Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description						
1	FC	I	Phase select input pin of the phase detector. This pin involves an internal pull up resistor. When this pin is low, characteristics of the charge pump and phase detector can be reversed. This input also selects f_{OUT} pin output level, either f_r or f_p . Please see page 6.						
2	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch.						
3	Data	I	Serial data of binary code input pin. This pin involves a schmitt trigger circuit.						
4	Clock	I	Clock input for 24-bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of data into the shift registers.						
5	V _{CC1}	—	PLL power supply voltage input pin.						
6 7	OSC _{IN} OSC _{OUT}	I O	Oscillator input pin. Oscillator output pin. A crystal is connected between OSC _{IN} pin and OSC _{OUT} pin.						
8	GND1	—	PLL ground pin.						
9 10	DO ₁ DO ₂	O O	Charge pump output pins. Phase characteristics can be reversed depending upon FC pin input level.						
11 12 13 14	BC4 BC3 BC2 BC1	O O O O	Band switching output pins. (Open-collector output) Output is controlled by a band bit data, individually. BCX—bit = H : BCX output transistor is ON. BCX—bit = L : BCX output transistor is OFF. (X = 1 to 4)						
15	fin	I	Complementary input pin of f_{in} . Please connect to GND through a capacitor.						
16	GND2	—	Prescaler ground pin.						
17	f_{in}	I	Prescaler input pin. This signal is AC coupled.						
18	V _{CC2}	—	Prescaler power supply voltage input pin.						
19	f_{OUT}	O	Monitor pin of the phase detector input. f_{OUT} pin outputs either of the programmable reference divider output frequency f_r or programmable divider output frequency f_p depending upon the FC pin input level. <table border="1" data-bbox="618 1402 1008 1545"> <thead> <tr> <th>FC Pin</th> <th>f_{out} output signal</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>f_r</td> </tr> <tr> <td>L</td> <td>f_p</td> </tr> </tbody> </table>	FC Pin	f_{out} output signal	H	f_r	L	f_p
FC Pin	f_{out} output signal								
H	f_r								
L	f_p								
20	LD	O	Phase detector output pin. Normally this pin outputs high. While the phase difference between f_r and f_p exists, this pin outputs low.						

FUNCTIONAL DESCRIPTIONS

DIVIDE RATIO SETTING

Divide ratio can be set using the following equation:

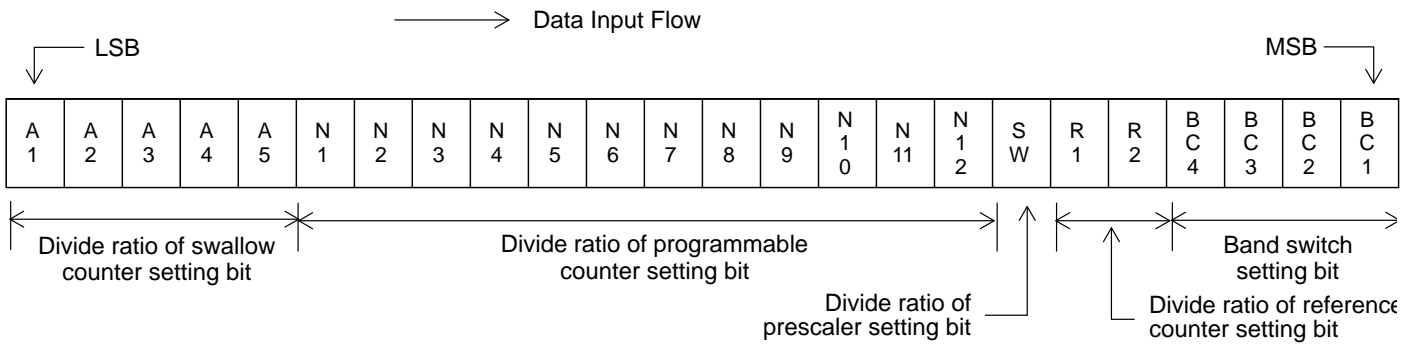
$$f_{VCO} = [(P \times N) + (16 \times A)] \times f_{osc} \div R$$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- P: Preset divide ratio of an internal dual modulus prescaler (256 or 512)
- N: Preset divide ratio of binary 12-bit programmable counter (32 to 4095)
- A: Preset divide ratio of binary 5-bit swallow counter (0 to 31)
- f_{osc} : Reference oscillator frequency
- R: Preset divide ratio of reference counter (256, 512, 1024, 2048)

SERIAL DATA INPUT

On rising edge of clock shifts one bit of the data into the shift register.
When the load enable is high, the data stored in the shift register is transferred to the latch.

24 bit of serial data format is shown below.



5-BIT SWALLOW COUNTER DIVIDE RATIO (A1 to A5)

Divide Ratio A	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
Σ	Σ	Σ	Σ	Σ	Σ
31	1	1	1	1	1

12-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (N1 to N12)

Divide Ratio	N 12	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
32	0	0	0	0	0	0	1	0	0	0	0	0
33	0	0	0	0	0	0	1	0	0	0	0	1
34	0	0	0	0	0	0	1	0	0	0	1	0
Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ
4095	1	1	1	1	1	1	1	1	1	1	1	1

FUNCTIONAL DESCRIPTIONS

REFERENCE COUNTER DIVIDE RATIO (R1 to R2)

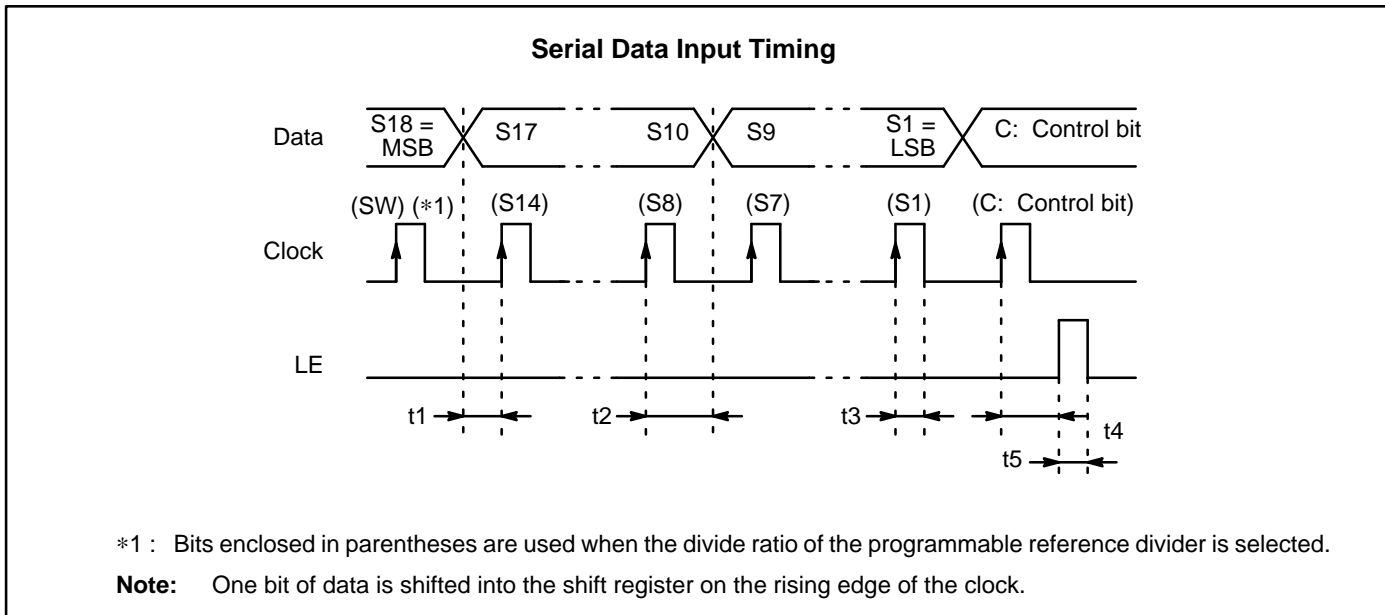
Divide Ratio R	R 2	R 1
256	0	0
512	0	1
1024	1	0
2048	1	1

Prescaler divide ratio (SW)

When divide ratio of prescaler setting bit is high, divide ratio of 256/272 is selected.
When divide ratio of prescaler setting bit is low, divide ratio of 512/528 is selected.

Band Switch Setting (BC1 to BC4)

When band switch setting bit is high, output is ON.
When band switch setting bit is low, output is OFF.



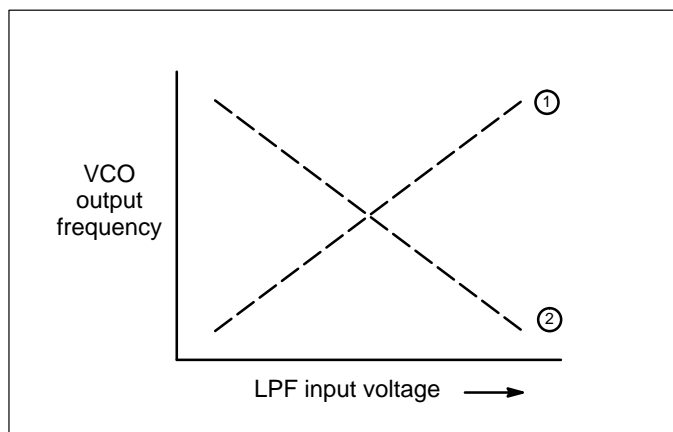
NOTES: On rising edge of the clock shifts one bit of data into the shift register.
When LE is high, the data stored in the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

FC pin selects the phase of the phase detector. Phase characteristics (charge pump output) can be reversed depending upon the FC pin input level. Monitor pin (f_{OUT}) output level is selected by FC pin input level as well

	FC=H or open		FC=L	
	D_{01}, D_{02}	f_{OUT}	D_0, D_{02}	f_{OUT}
$f_r > f_p$	H	Outputs programmable reference divider output frequency f_r .	L	Outputs programmable divider output frequency f_p .
$f_r = f_p$	L		Z	
$f_r < f_p$	Z		H	

Note: Z = (High impedance)

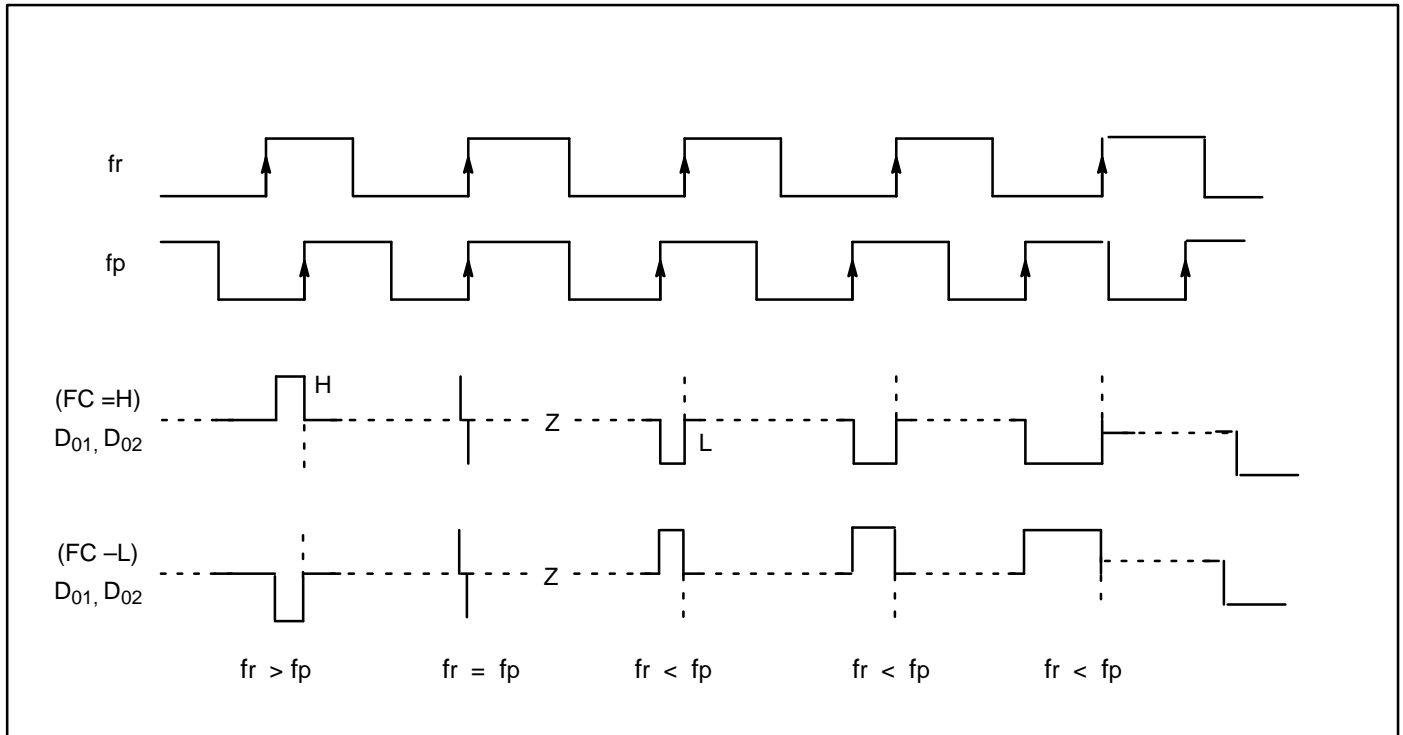


VCO CHARACTERISTICS

Depending upon VCO polarity, FC pin should be set accordingly:

- When VCO polarity are like ① FC should be set High or open.
- When VCO polarity are like ② FC should be set Low.

PHASE DETECTOR WAVEFORM



NOTES: Phase difference detection range: -2π to $+2\pi$
 Spike shape depends on charge pump characteristics.
 The spike is output to diminish dead band.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_I	GND	—	V_{CC}	V
Operating Temperature	T_A	-40	—	+85	°C

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

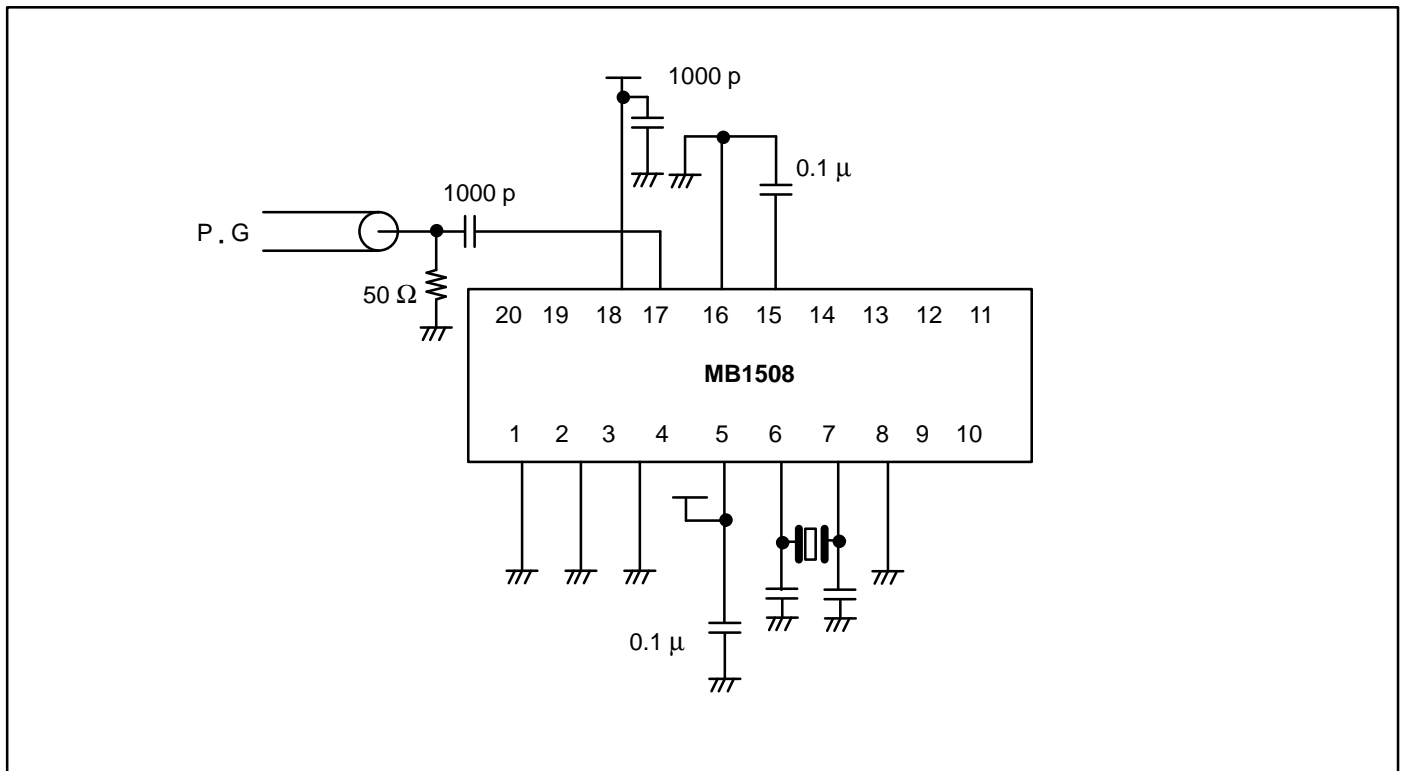
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	
Power Supply Current	I_{CC}	Note 1	—	16.0	—	mA	
Operating Frequency	f_{in}	Note2	10	—	2500	MHz	
	OSC_{IN}	—	—	4	10		
Input Sensitivity	f_{in}	P_{fin}	2300 to 2500MHz	-4	—	6	dBm
			1900 to 2300MHz	-7	—	6	
			10 to 1900MHz	-10	—	6	
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V _{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	—	$V_{CC} \times 0.7 + 0.4$	—	V	
Low-level Input Voltage		V_{IL}	—	—	$V_{CC} \times 0.3 - 0.4$		
High-level Input Current	Data Clock LE	I_{IH}	—	—	1.0	μA	
Low-level Input Current		I_{IL}	—	—	-1.0		—
		FC	I_{ILFC}	—	—		-60
Input Current	OSC_{IN}	I_{OSC}	—	—	+50	—	
High-level Output Voltage	Except D _O and BC1 to BC4	V_{OH}	$V_{CC} = 5.0 V$	4.4	—	—	V
Low-level Output Voltage		V_{OL}		—	—	0.4	
High Impedance Cutoff Current	D _{O1} , D _{O2} BC1 to BC4	I_{OFF}	—	—	—	1.1	μA
High-level Output Current	Except D _O and BC1 to BC4	I_{OH}	—	-1.0	—	—	mA
Low-level Output Current		I_{OL}	—	1.0	—	—	
Withstand Output Voltage	BC1 to BC4	V_B	—	—	—	12	V

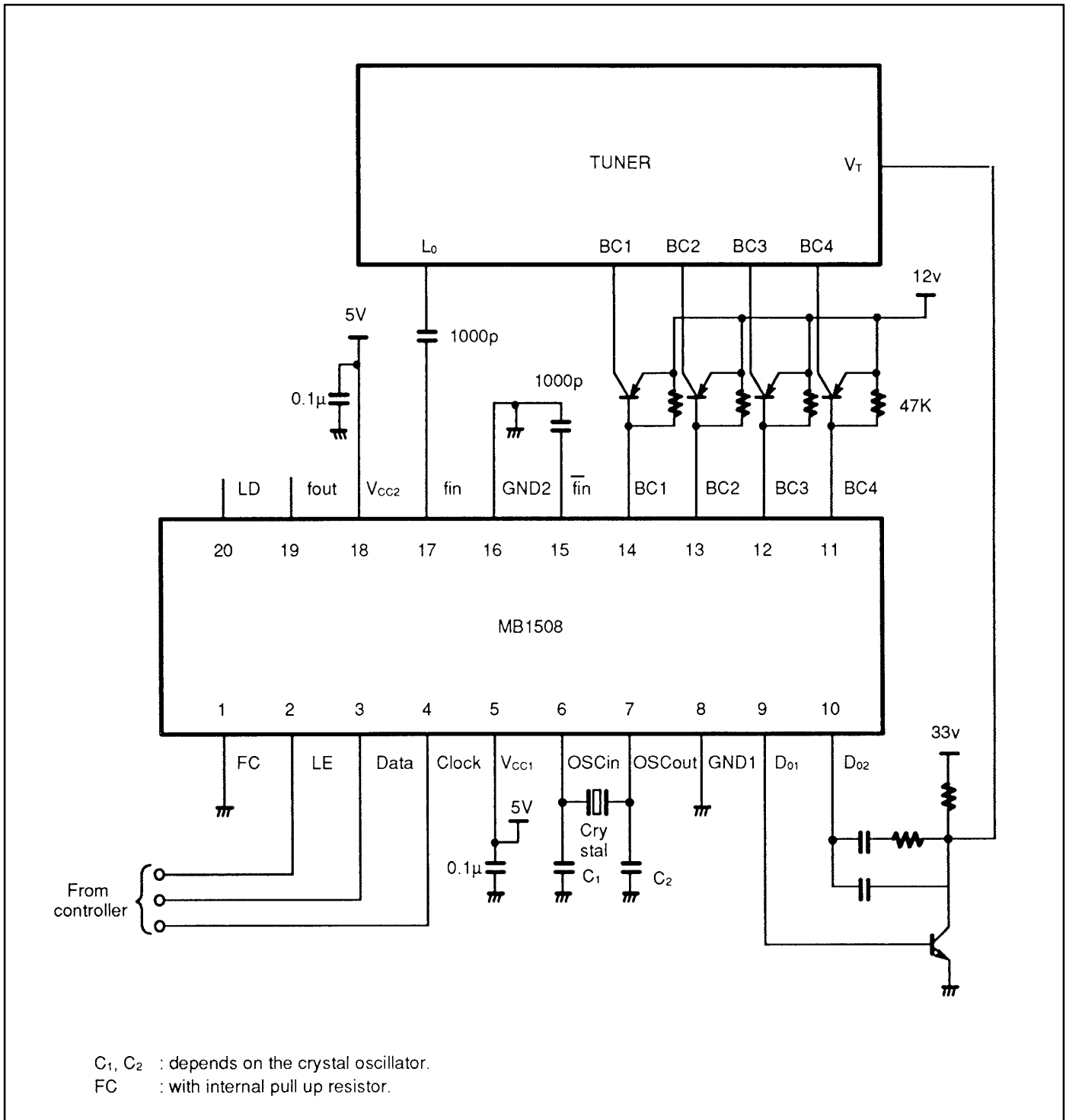
NOTE: 1: $f_{in} = 2.5\text{GHz}$, $OSC_{IN} = 4.0\text{MHz}$, $V_{CC} = 5.0\text{V}$. Inputs are grounded and outputs are open.
2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

TEST CIRCUIT

Prescaler Input Sensitivity

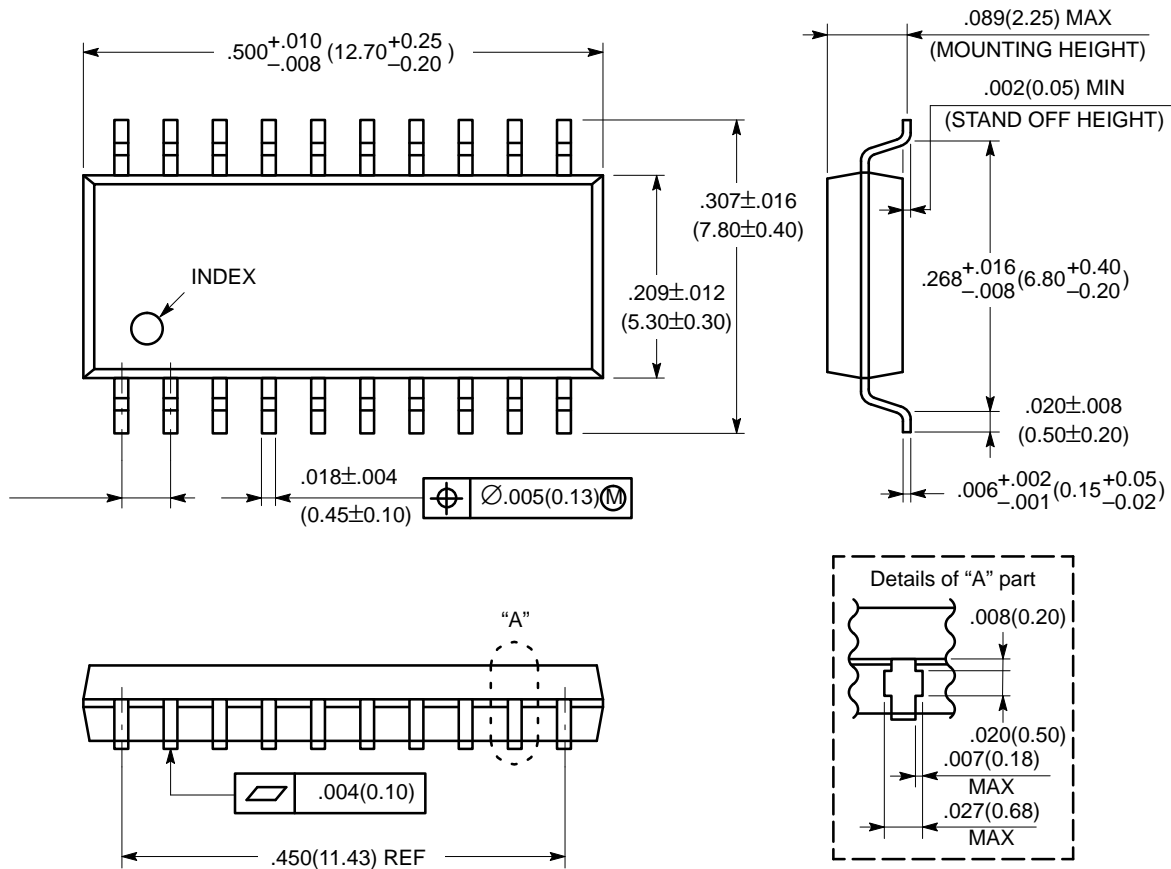


MB1508 MB1508 APPLICATION CIRCUIT



PACKAGE DIMENSIONS

**20-Lead Plastic Flat Package
(Case No.: FPT-20P-M01)**



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Dimensions in inches (millimeters)

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