FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27218-4E

ASSP For Power Supply Applications

Pentium® II DC/DC Converter IC

MB3870

■ DESCRIPTION

The FUJITSU MB3870 is a pulse width modulation (PWM) DC/DC converter IC chip that provides a selection of 1.3 V to 3.5 V output voltages for Pentium®* CPU's, using a 5-bit input signal information.

The MB3870 utilizes synchronous rectification for high efficiency and features a soft-start/discharge control function for ease in designing power supplies in multi-supply systems, making it ideal for Pentium® II power supply systems.

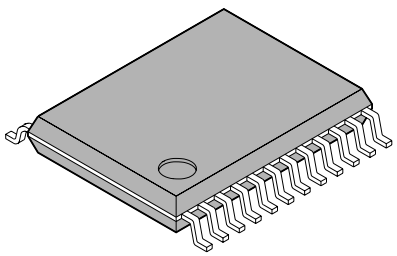
* : Pentium is the registered trademark of Intel Corporation.

■ FEATURES

- Highly efficient for using synchronous rectification scheme
- On-chip soft-start/discharge control circuit
- High precision output voltage: ±1.2%
- 5-bit, 32-step DAC: 3.5 V to 2.1 V in 100 mV steps
  2.05 V to 1.3 V in 50 mV steps
- Frequency range: 100 kHz to 500 kHz using variable resistance (on-chip frequency setting capacitance)
- Standby current: 0 µA TYP
- On-chip PWRGOOD circuit for output voltage state detection
- Timer-latch short-circuit protection circuit, and overvoltage protection circuit for output protection

■ PACKAGE

24-pin Plastic SSOP



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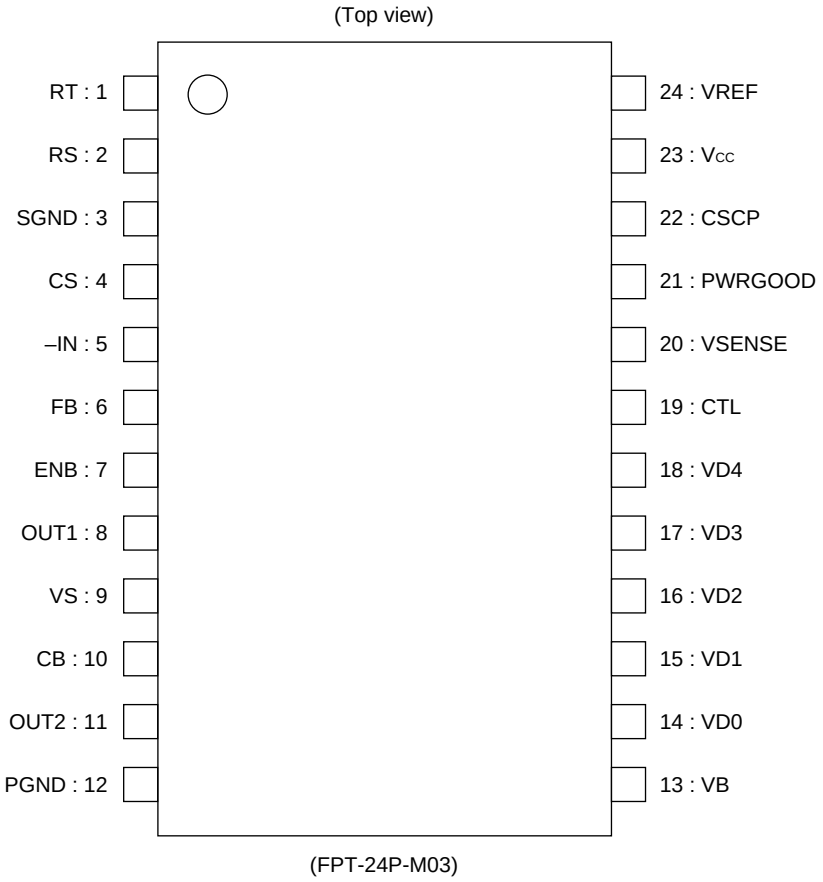
■ PIN ASSIGNMENT



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■ PIN DESCRIPTION

Pin no.	Symbol	I/O	Descriptions
1	RT	—	Triangular wave frequency setting resistor connection pin
2	RS	—	Discharging resistor connection pin for soft start capacitor
3	SGND	—	Ground pin
4	CS	—	Soft start capacitor connection pin (Also used for discharge control)
5	–IN	I	Error amplifier inverted input pin
6	FB	O	Error amplifier output pin
7	ENB	I	Discharge control function enable/disable switch control pin
8	OUT1	O	Totem-pole output pin (External main-side FET gate drive)
9	VS	—	External main-side FET source-side connection
10	CB	—	Output bootstrap pin Insert a capacitor between the CB and VS pins, to bootstrap the IC internal output transistor.
11	OUT2	O	Totem-pole output pin (External synchronous rectifier-side FET gate drive)
12	PGND	—	Ground pin
13	VB	—	Output circuit power supply pin
14	VD0	I	5-bit digital input pin used to set DC/DC converter output voltage
15	VD1	I	5-bit digital input pin used to set DC/DC converter output voltage
16	VD2	I	5-bit digital input pin used to set DC/DC converter output voltage
17	VD3	I	5-bit digital input pin used to set DC/DC converter output voltage
18	VD4	I	5-bit digital input pin used to set DC/DC converter output voltage
19	CTL	I	Power supply control pin The CTL pin is set to “L” level to place the IC in standby mode.
20	VSENSE	I	PWRGOOD circuit input pin
21	PWRGOOD	O	PWRGOOD output pin (open-drain output) Outputs a “H” level signal when the output voltage is within the range from VTLOW to VTHIGH.
22	CSCP	—	Timer-latch short-circuit protection capacitor connection pin
23	V_{CC}	—	Power supply pin for reference power and control circuit
24	VREF	O	Reference voltage output pin

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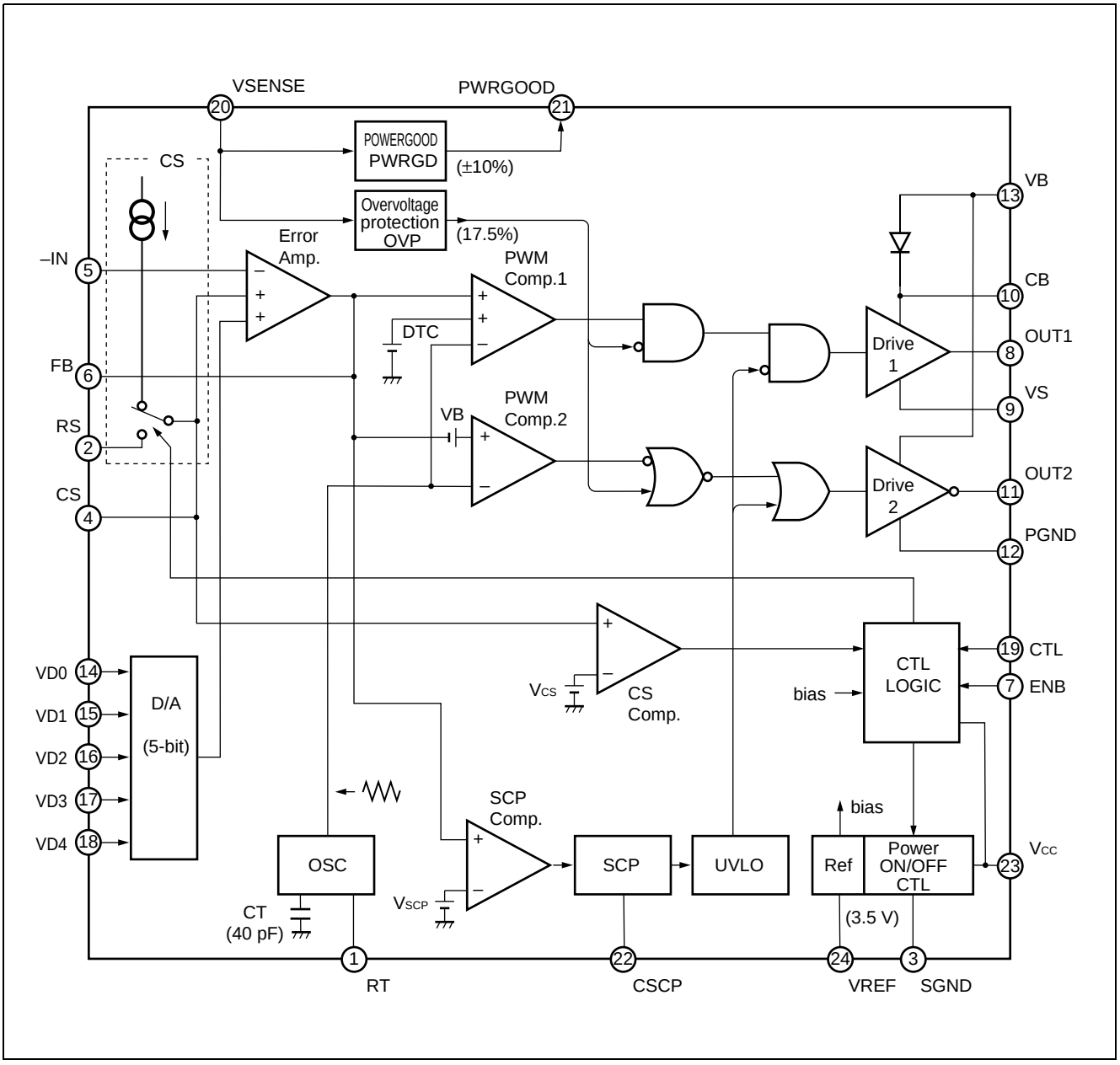
■ BLOCK DIAGRAM



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■ OUTPUT VOLTAGE SETTING CODE

VD4	VD3	VD2	VD1	VD0	VD (DC/DC converter output voltage) (V)
1	0	0	0	0	3.500
1	0	0	0	1	3.400
1	0	0	1	0	3.300
1	0	0	1	1	3.200
1	0	1	0	0	3.100
1	0	1	0	1	3.000
1	0	1	1	0	2.900
1	0	1	1	1	2.800
1	1	0	0	0	2.700
1	1	0	0	1	2.600
1	1	0	1	0	2.500
1	1	0	1	1	2.400
1	1	1	0	0	2.300
1	1	1	0	1	2.200
1	1	1	1	0	2.100
1	1	1	1	1	0 (output OFF)
0	0	0	0	0	2.050
0	0	0	0	1	2.000
0	0	0	1	0	1.950
0	0	0	1	1	1.900
0	0	1	0	0	1.850
0	0	1	0	1	1.800
0	0	1	1	0	1.750
0	0	1	1	1	1.700
0	1	0	0	0	1.650
0	1	0	0	1	1.600
0	1	0	1	0	1.550
0	1	0	1	1	1.500
0	1	1	0	0	1.450
0	1	1	0	1	1.400
0	1	1	1	0	1.350
0	1	1	1	1	1.300

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■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Power supply voltage	V_{CC}	—	20	V
Bias voltage	V_B	—	20	V
Boot voltage	V_{CB}	—	32	V
Control input voltage	V_{CTL}	—	20	V
PWRGOOD output voltage	V_{PWRGD}	—	17	V
Output current	I_O	—	120	mA
Peak output current	I_O	Duty ≤ 5% (t = 1/f_{OSC} × Duty)	800	mA
Allowable dissipation	P_D	Ta ≤ +25°C	740*	mW
Storage temperature	Tstg	—	–55 to +125	°C

* : When mounted on a 10 cm-square dual-sided epoxy base board

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{CC}	—	4.6	5	18	V
Bias voltage	V_B	—	—	5	18	V
Boot voltage	V_{CB}	—	—	—	30	V
Reference voltage output current	I_{OR}	—	–1	—	0	mA
Input voltage	V_{IN}	–IN pin	0	—	V_{CC} – 0.9	V
	V_{IN}	CTL, ENB, VD4 to VD0 pins	0	—	18	V
	V_{IN}	VSENSE	0	—	V_{CC}	V
Output current	I_O	OUT pin	–100	—	100	mA
	I_{PG}	PWRGOOD pin	—	—	1	mA
Peak output current	I_O	Duty ≤ 5% ($t = 1/f_{OSC} \times$ Duty)	–700	—	700	mA
Oscillator frequency	f_{OSC}	—	100	200	500	kHz
Timing resistance	R_T	—	51	130	270	kΩ
Boot capacitance	C_B	—	—	0.1	1.0	µF
Reference voltage output capacitance	C_{REF}	—	—	0.1	1.0	µF
Soft start capacitance	C_S	—	—	4700	10000	pF
Discharge control resistance	R_S	—	—	100	470	kΩ
Short detection capacitance	C_{SCP}	—	—	2200	10000	pF
Operating temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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■ ELECTRICAL CHARACTERISTICS

(Ta = +25°C, V_{CC} = 5 V)

Parameter		Symbol	Pin no.	Condition	Value			Unit
					Min.	Typ.	Max.	
Reference voltage block (Ref)	Output voltage	V_{REF}	24	V_{REF} = 0 mA	3.465	3.500	3.535	V
	Output voltage temperature regulation	ΔV_{REF} /V_{REF}	24	Ta = –30°C to +85°C*	—	0.5	—	%
	Input stability	Line	24	V_{CC} = 4.6 V to 18 V	—	1	10	mV
	Load stability	Load	24	I_O = 0 mA to –1 mA	—	3	10	mV
	Short circuit output current	I_{OS}	24	VREF = 1 V	–20	–10	–3	mA
Under voltage lockout circuit block (UVLO)	Threshold voltage	V_{TH}	4	V_{CC} = ↑	3.4	3.7	4.0	V
	Hysteresis voltage	V_H	4	—	—	0.18	0.21	V
	Reset voltage	V_{RST}	4	—	1.7	2.1	—	V
Soft start block (CS)	Charge current	I_{CS}	4	—	–2.8	–2.0	–1.2	µA
Short circuit protection comparator block (SCP)	Threshold voltage	V_{TH}	4	—	0.63	0.68	0.73	V
	Input source current	I_{CSCP}	22	—	–2.8	–2.0	–1.2	µA
	Short detection interval	t_{SCP}	22	CSCP = 2200 pF	0.50	0.75	1.34	ms
Triangular wave oscillator block (OSC)	Oscillator frequency	f_{OSC}	8, 11	R_T = 130 kΩ	180	200	220	kHz
	Frequency temperature regulation	Δf/fdt	8, 11	Ta = –30°C to +85°C*	—	1	—	%
Error amplifier block (Error Amp.)	Threshold voltage	V_{TH1}	6	FB = 1.6 V, VD4 to VD0 = 00101	1.7784	1.8000	1.8216	V
		V_{TH2}	6	FB = 1.6 V, VD4 to VD0 = 11010	2.4700	2.5000	2.5300	V
	VTH temperature regulation	$\Delta V_T/V_T$	6	Ta = –30°C to +85°C*	—	0.5	—	%
	Input bias current	I_B	5	–IN = 0 V	–200	–50	—	nA
	Voltage gain	A_V	6	DC	60	100	—	dB
	Frequency bandwidth	BW	6	A_V = 0 dB*	—	800	—	kHz
	Output voltage	V_{OH}	6	—	2.18	3.5	—	V
		V_{OL}	6	—	—	0.8	1.0	V
	Output source current	I_{SOURCE}	6	FB = 1.6 V	—	–90	–45	µA
	Output sink current	I_{SINK}	6	FB = 1.6 V	3.0	12.0	—	mA

* : Standard design value

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(Ta = +25°C, V_{CC} = 5 V)

Parameter		Symbol	Pin no.	Condition	Value			Unit
					Min.	Typ.	Max.	
PWM comparator blocks (PWM Comp.1, 2)	Threshold voltage	V_{TL}	8, 11	Duty cycle = 0%	1.2	1.3	—	V
		V_{TH}	8, 11	Duty cycle = Dtr	—	1.86	2.0	V
Dead time control block (DTC)	Maximum duty cycle	Dtr	8	R_T = 130 kΩ	85	90	95	%
Output blocks (Drive1, 2)	Output voltage (main side)	V_{OH}	8	OUT1 = –100 mA, VB = 5 V, CB = 10 V, VS = 5 V	CB – 2.5	CB – 1.5	—	V
		V_{OL}	8	OUT1 = 100 mA, VB = 5 V, CB = 10 V, VS = 5 V	—	VS + 1.1	VS + 1.4	V
	Output voltage (synchronized rectifier side)	V_{OH}	11	OUT2 = –100 mA, VB = 5 V	VB – 2.5	VB – 1.5	—	V
		V_{OL}	11	OUT2 = 100 mA, VB = 5 V	—	1.1	1.4	V
	Diode voltage	V_{DIODE}	13	I_{DIODE} = 10 mA	—	1.0	1.1	V
Control block (CTL)	CTL input voltage	V_{IH}	24	IC operating mode	2.0	—	18	V
		V_{IL}	24	IC standby mode	0	—	1.0	V
	Input current	I_{CTL}	19	CTL = 5 V	—	100	160	µA
PWRGOOD comparator protection block (PWRGD)	Threshold voltage	V_{TLOW}	21	VD4 to VD0 setting, VSENSE = ↑	0.88 × VD	0.90 × VD	0.92 × VD	V
		V_{THIGH}	21	VD4 to VD0 setting, VSENSE = ↑	1.08 × VD	1.10 × VD	1.12 × VD	V
	Hysteresis voltage	V_H	21	—	3	30	50	mV
	Output leak current	I_{LEAK}	21	PWRGOOD = 5 V	—	—	40	µA
	Output voltage	V_{OL}	21	PWRGOOD = 1 mA	—	0.06	0.4	V
Discharge control comparator (CS Comp.)	Threshold voltage	V_{TH}	24	CS = ↓	—	0.05	0.07	V
Discharge control ON/OFF block (CTL LOGIC)	ENB input voltage	V_{IH}	24	Discharge control ON	2.0	—	18	V
		V_{IL}	24	Discharge control OFF	0	—	1.0	V
	Input current	I_{ENB}	7	ENB = 0 V	–1.0	–0.05	—	µA

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(Continued) (Ta = +25°C, V_{CC} = 5 V)

Parameter		Symbol	Pin no.	Condition	Value			Unit
					Min.	Typ.	Max.	
Over voltage protection comparator block (OVP)	Threshold voltage	V_{TH}	8, 11	VSENSE = ↑, VD = 1.3 V	1.15 × VD	1.175 × VD	1.20 × VD	V
	Hysteresis voltage	V_H	8, 11	—	3	30	50	mV
	VSENSE pin input current	I_{SENSE}	20	VSENSE = 0 V	–10	–0.1	—	µA
D/A (VD4 to VD0 pin) (D/A)	D/A input voltage	V_{IH}	14 to 18	—	2.0	—	18	V
	D/A input voltage	V_{IL}	14 to 18	—	0	—	1.0	V
	Input current	I_D	14 to 18	VD4 to VD0 = 5 V	—	0.05	1.0	µA
General	Standby current	I_{CCS}	23	CTL = 0 V	—	0	10	µA
	Power supply current	I_{CC}	23	—	—	4.0	6.0	mA

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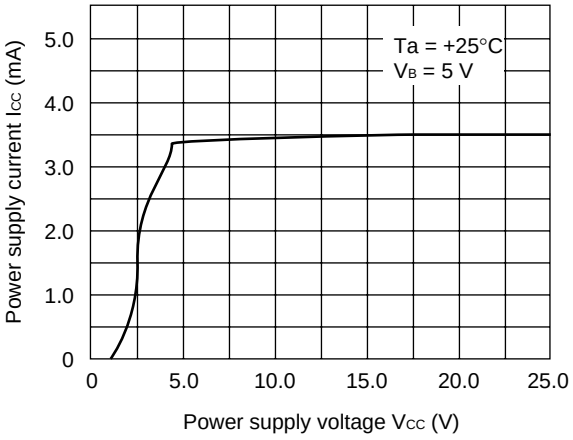
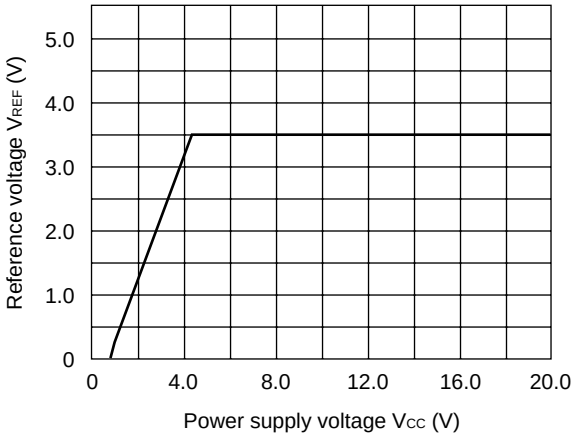
■ TYPICAL CHARACTERISTICS

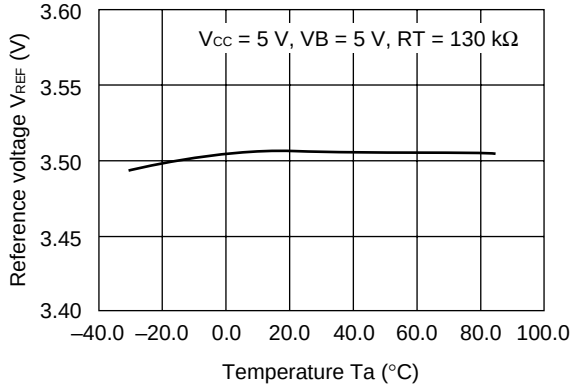
Power supply current vs. Power supply voltage characteristics



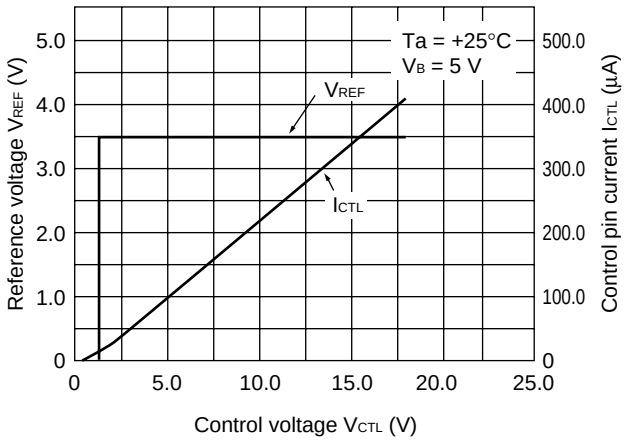
Reference voltage vs. Power supply voltage characteristics



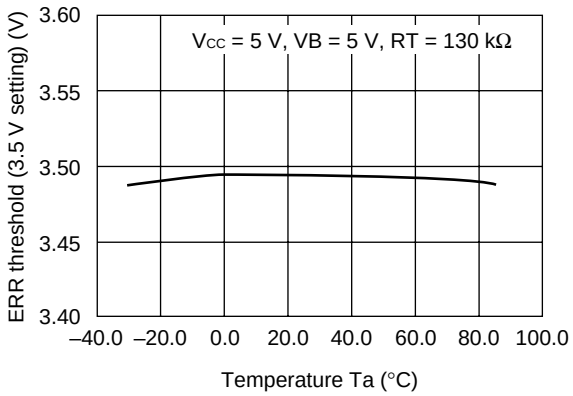
VREF vs. Temperature characteristics



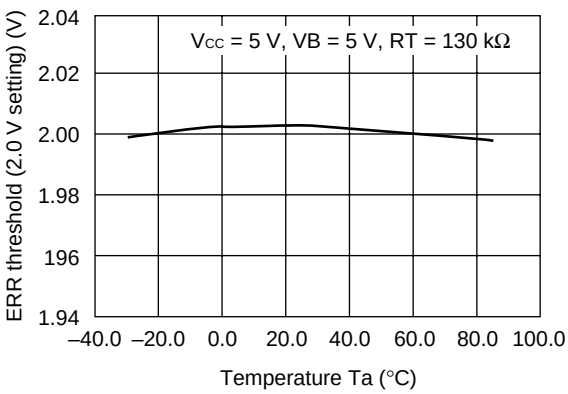
Reference voltage, CTL pin current vs. Control voltage



ERR threshold (3.5 V setting) vs. Temperature characteristics



ERR threshold (2.0 V setting) vs. Temperature characteristics



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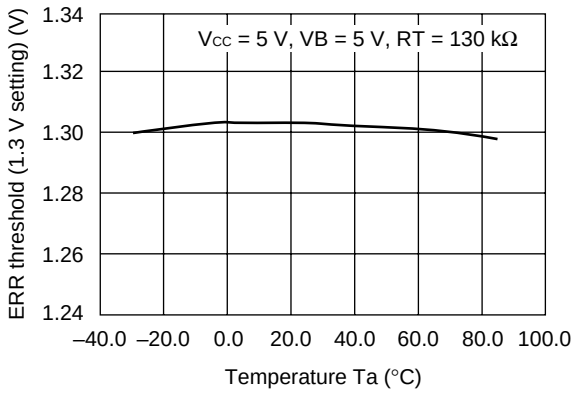
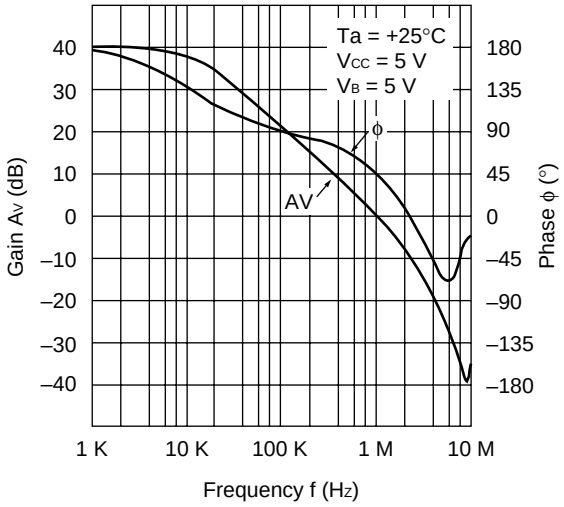
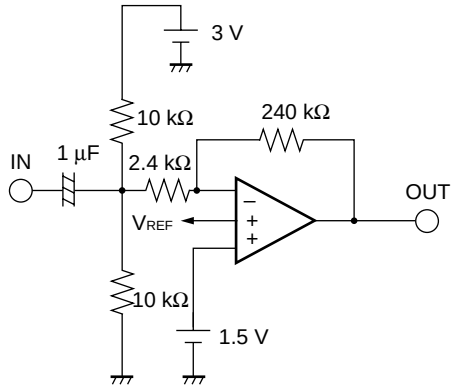
ERR threshold (1.3 V setting) vs. Temperature characteristics



Error Amp. gain, Phase vs. Frequency characteristics



Error Amp.



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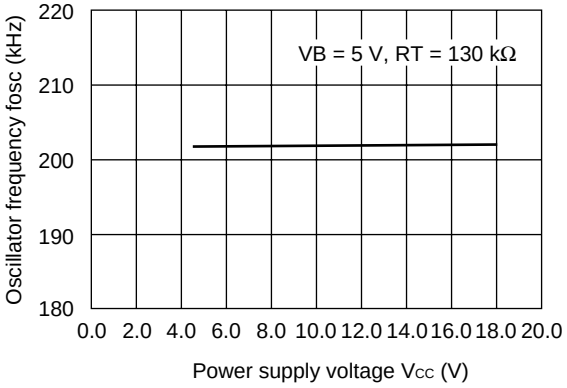
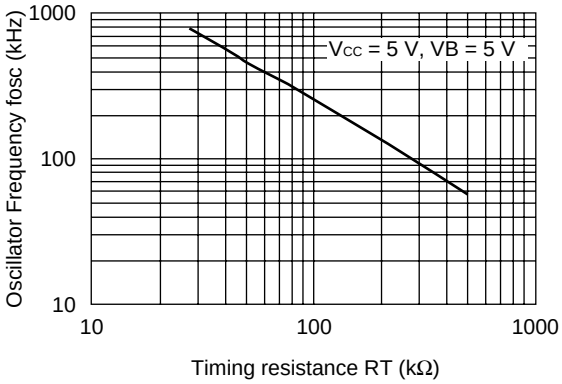
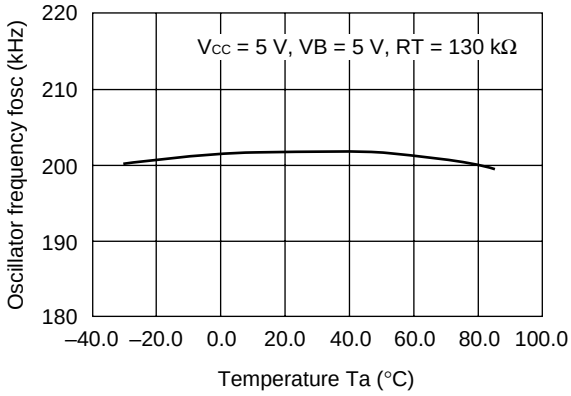
Triangular wave oscillator frequency vs.
Power supply voltage characteristics



Triangular wave oscillator frequency vs.
Timing resistance characteristics



Triangular wave oscillator frequency vs. Temperature characteristics



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■ FUNCTION DESCRIPTION

1. Switching Regulator Function

(1) Reference voltage circuit (Ref)

The reference voltage circuit uses the voltage supply from the V_{CC} pin (pin 23) to generate a temperature compensated reference voltage (≅ 3.5 V) for use as the reference voltage for the internal circuits of the IC chip.

It is also possible to supply a reference voltage output of up to 1 mA to external circuits through the VREF pin (pin 24).

(2) Triangular wave oscillator (OSC)

The triangular wave form is generated using an on-chip frequency selection capacitor, plus the frequency selection resistance connected to the RT pin (pin 1).

The triangular wave is input to the PWM comparator circuits on the IC.

(3) Error amplifier (Error Amp.)

The error amplifier circuit is used to detect the output voltage from the DC/DC converter for output as the PWM control signal. The in-phase input range covers the full range from 0 V to V_{CC} – 0.9 V. By connecting a feedback resistance and capacitor between the FB pin (pin 6) and –IN pin (pin 5), it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent current spikes at power supply start-up by connecting a soft start capacitor to the CS pin (pin 4), the non-inverting input pin for Error Amp. The use of Error Amp. for soft start detection makes it possible for a system to operate on a fixed soft start time that is independent of the output load on the DC/DC converter.

(4) PWM comparators (PWM Comp.1, PWM Comp.2)

PWM Comp.1 and PWM Comp.2 are voltage-pulse width converters that control output voltage according to input voltage.

PWM Comp.1 controls the pulse width on the main-side output circuit, and PWM Comp.2 controls the pulse width on the synchronous rectifier side output circuit.

The triangular wave generated by the triangular wave oscillator is compared with the output voltage from Error Amp., and during intervals when Error Amp. output is higher than the triangular wave, the main-side output transistor is switched on and the synchronous rectifier side output transistor is turned off.

PWM Comp.1 is set to a maximum duty cycle of approximately 90%.

(5) Output circuits (Drive1, Drive2)

The output circuits on both the main-side and synchronous rectifier-side have a totem-pole configuration, and are capable of driving an external N-ch. MOS FET.

(6) Power supply control circuit (CTL)

This circuit is able to control power supply ON/OFF switching from the CTL pin (pin 19). (During standby mode, supply current is 0 μA TYP.)

(7) DAC circuit (D/A)

This circuit controls the output voltage to the CPU between 1.3 V and 3.5 V, as selected by the 5-bit (32-step) input signal information.

The output voltage can be set in 100 mV steps between 3.5 V and 2.1 V, and in 50 mV steps between 2.05 V and 1.3 V.

When all D/A input pins VD4 through VD0 (pin 18 through pin 14) are set to “H” level, the DC/DC converter output voltage is 0 V.

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2. Protection Functions

(1) V_{CC} under voltage lockout circuit (UVLO)

Power surges at power-on, or momentary under-voltage situations can cause abnormal operation in the MB3870, which may lead to damage or deterioration in systems. This circuit prevents abnormal operation during times of low voltage by using the supply voltage to detect the level of the internal reference voltage, and fixes output pins OUT1 (pin 8) and OUT2 (pin 11) to “L” level. Once the supply voltage recovers to a level above the threshold voltage of the under voltage lockout circuit, operation is restored.

(2) Timer-latch short-circuit protection circuit (SCP)

This circuit detects the output voltage level from Error Amp. and activates the timer circuit, charging the external capacitor from the CSCP pin (pin 22) when Error Amp. output voltage level reaches or exceeds about 2.1 V. If Error Amp. output does not return to the normal voltage range before the capacitor voltage reaches about 0.68 V, the latch circuit is activated and the output pins (OUT1, OUT2) are held at “L” level. Once the protector circuit is activated, it can be reset by switching the power supply off and on again.

(3) Overvoltage protection circuit (OVP)

When the DC/DC converter output voltage (V_O) exceeds the output voltage set by the VD4 to VD0 pins by more than +17.5%, the overvoltage protection circuit output signal goes to “H” level causing one output pin (OUT1) to be held at “L” level and the other output pin (OUT2) to be held at “H” level.

(4) PWRGOOD comparator detection circuit (PWRGD)

The PWRGOOD pin (pin 21) outputs an “H” level signal as long as the VSENSE pin (pin 20) is receiving the DC/DC converter output voltage (V_O) within the range of 0.9 to 1.1 times the output voltage set by the VD4 to VD0 pins.

3. Soft Start/Discharge Control

(1) Soft start circuit (CS)

Connecting a capacitor to the CS pin (pin 4) prevents the inrush current at power turnon. Using an Error Amp. for detecting the soft error allows the soft start time to be initiated independent of output load from the DC/DC converter.

(2) Discharge control ON/OFF circuit (CTL LOGIC)

Entering an “L” level signal at the CTL pin while an “H” level signal is input at the ENB pin causes the discharge control ON/OFF circuit (CTL LOGIC) to switch the soft start circuit (CS) from charging to discharging.

The resistance (R_S) connected to the RS pin (pin 2) charges the soft start capacitor (C_S), so that Error Amp. provides control over the DC/DC converter output voltage in the same way as during a soft start. This makes it possible to control voltage drop independently of output load.

When the CS pin voltage reaches the discharge control comparator circuit (CS Comp.) threshold voltage ($\cong$ 50 mV), the discharge control is canceled.

When an “L” level signal is input at the ENB pin (pin 7), the DC/DC converter output voltage discharge time control is switched OFF.

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■ METHOD OF SETTING THE SOFT START TIME

At startup of the MB3870, the capacitor (C_S) connected to the CS pin begins charging. This produces a soft start, by providing output voltage from Error Amp. that is proportional to the CS pin voltage regardless of the DC/DC converter load current.

Soft start time (time to output setting voltage VD)

$$t_S \text{ (sec)} \simeq \frac{VD}{2\ (\mu A)} \times C_S\ (\mu F)$$

■ TIME SETTING BY SHORT DETECTION

When load conditions change rapidly with the reduced output voltage, as when a load fault occurs, the Capacitor Cscp connected to the CSCP pin (pin 22) is charged to threshold voltage (V_{TH}:=0.68V) and sets a latch, the external FET is turned off (inactive interval 100%).

Short detection time

t_{PE} (sec) ≃ 0.68 × C_{SCP} (μF) / 2 (μA)

■ OSCILLATOR FREQUENCY SETTING

The oscillator frequency can be set by connecting resistance to the RT pin (pin 1).

Oscillator frequency

f_{OSC} (kHz) ≃ 26250 / RT (kΩ)

■ METHOD OF SETTING THE DISCHARGE TIME

- An “L” level CTL signal while the ENB pin is set to “H” level causes the resistance (R_S) connected to the RS pin to discharge electrical charge the capacitor (C_S) connected to the CS pin, causing the output voltage to fall gradually regardless of the DC/DC converter load current.

  Discharge time (time to 0.05 V output voltage)

  $$\text{toff (msec)} \simeq R_S\ (k\Omega) \times C_S\ (\mu F) \times \ln\left(\frac{VD}{V_{TH\ (CS\ COMP)}}\right)$$

- As long as the ENB pin is set to “L” level, the discharge control function is switched OFF.

■ D/A BLOCK VD4 to VD0 SWITCHING

- Switching of the VD4 to VD0 pin signal during the MB3870 operation may cause transient fluctuation in output voltage from the DC/DC converter. The resulting voltage instability may cause an “L” level from the PWRGOOD block, activating the OVP protection and shutting off the output from the DC/DC converter.
  To switch VD4 to VD0 pin settings, first input an “L” level control signal to the CTL pin to place the MB3870 in standby status.
- When all VD4 to VD0 pin signals are set to “H” level, the DC/DC converter output is switched OFF.

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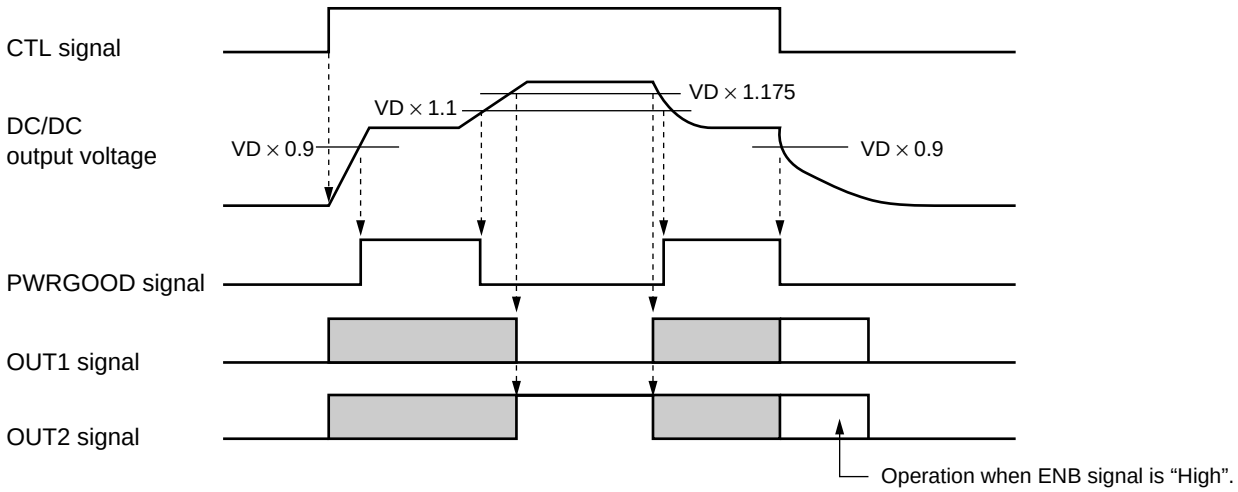
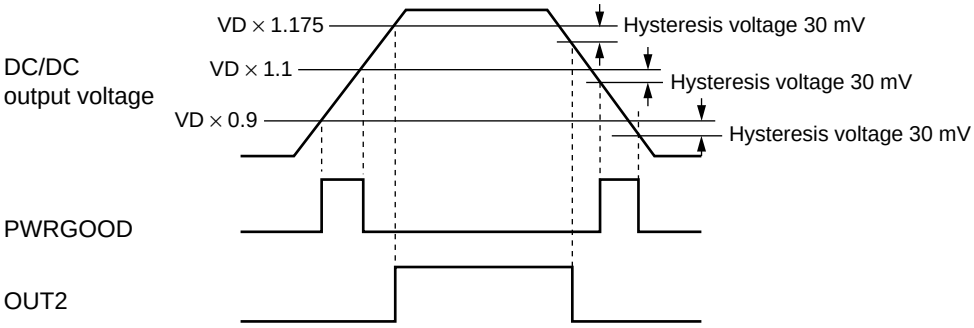
■ PWRGOOD COMPARATOR CIRCUIT, OVP CIRCUIT OPERATION TIMING CHART





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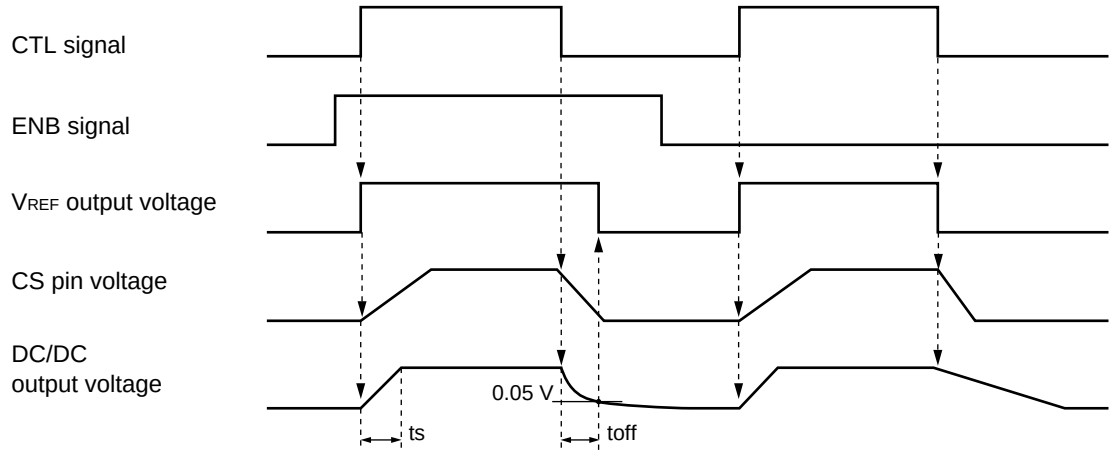
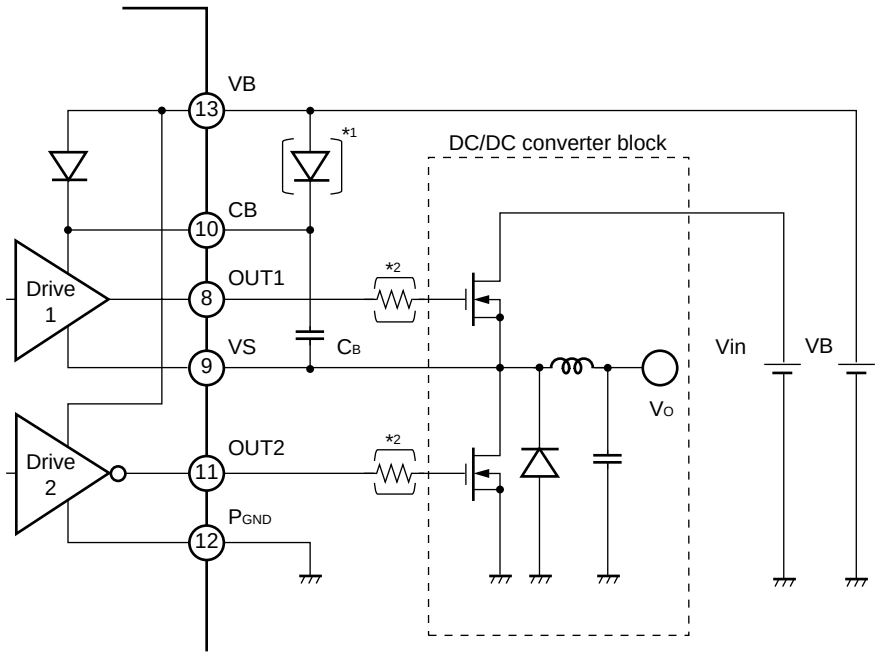
■ CTL LOGIC CIRCUIT OPERATION TIMING CHART



■ DC/DC CONVERTER INPUT VOLTAGE (Vin) AND VB VOLTAGE SETTING

The voltage at the CB pin is bootstrapped from the VS pin voltage by an amount equivalent to the VB pin voltage, as a result of the bootstrap capacitance (C_B) between the CB pin and VS pin. Therefore, either the Vin voltage or VB pin voltage should be adjusted so that the sum of the DC/DC converter block input voltage Vin plus the VB pin voltage does not exceed the recommended operating conditions for the CB pin boot voltage (V_{CB}).



*1: To connect the external low VF diode (Schottky barrier diode) makes VB pin voltage drop reduced and then can perform the higher efficiency.

*2: The switching noise can be reduced (0Ω to 5Ω) by connecting the resistance when the external MOSFET gate input capacitance (Ciss) is large, caused by the external MOSFET gate drive current limiting resistance.

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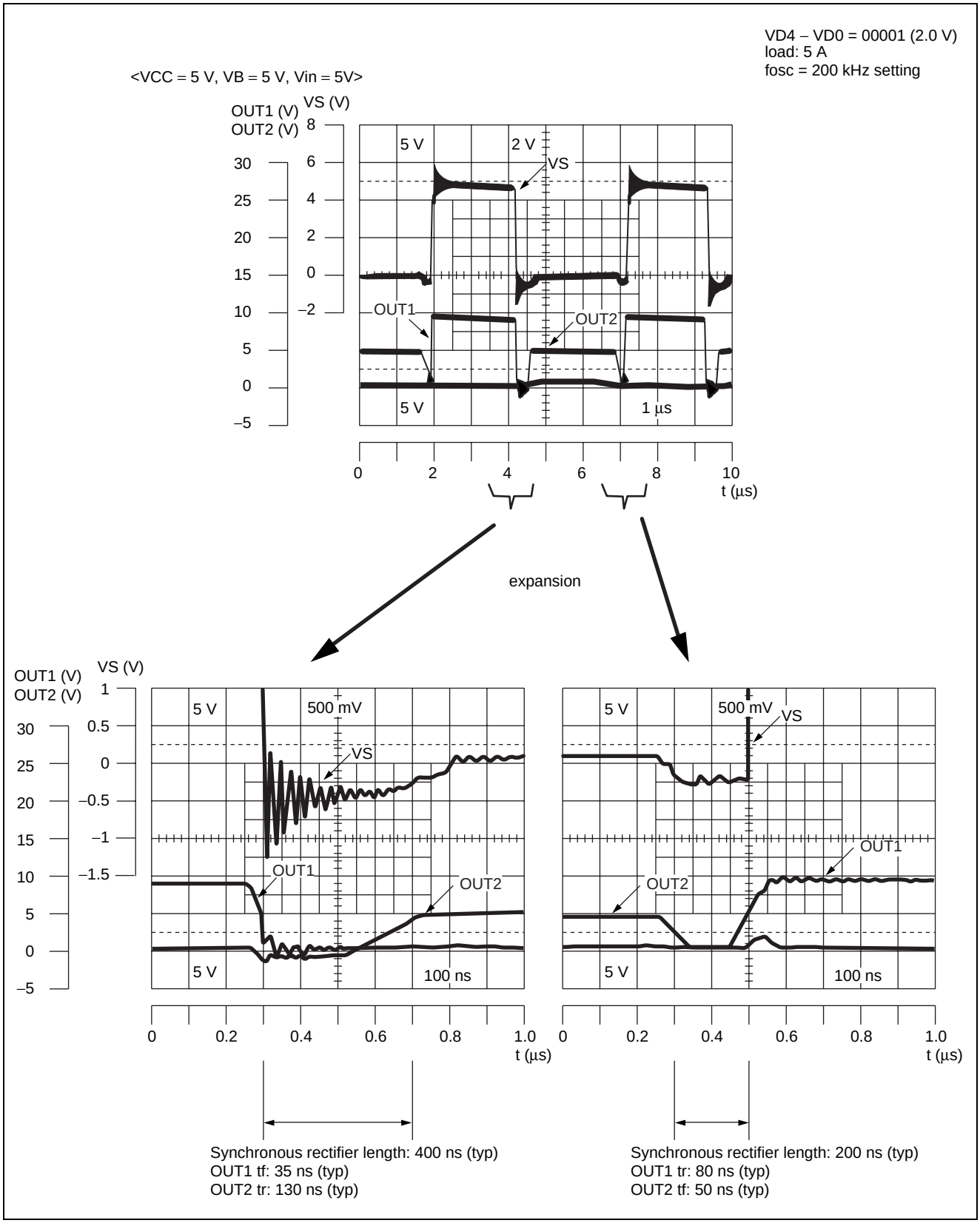
■ DC/DC CONVERTER SWITCHING OPERATION WAVEFORMS



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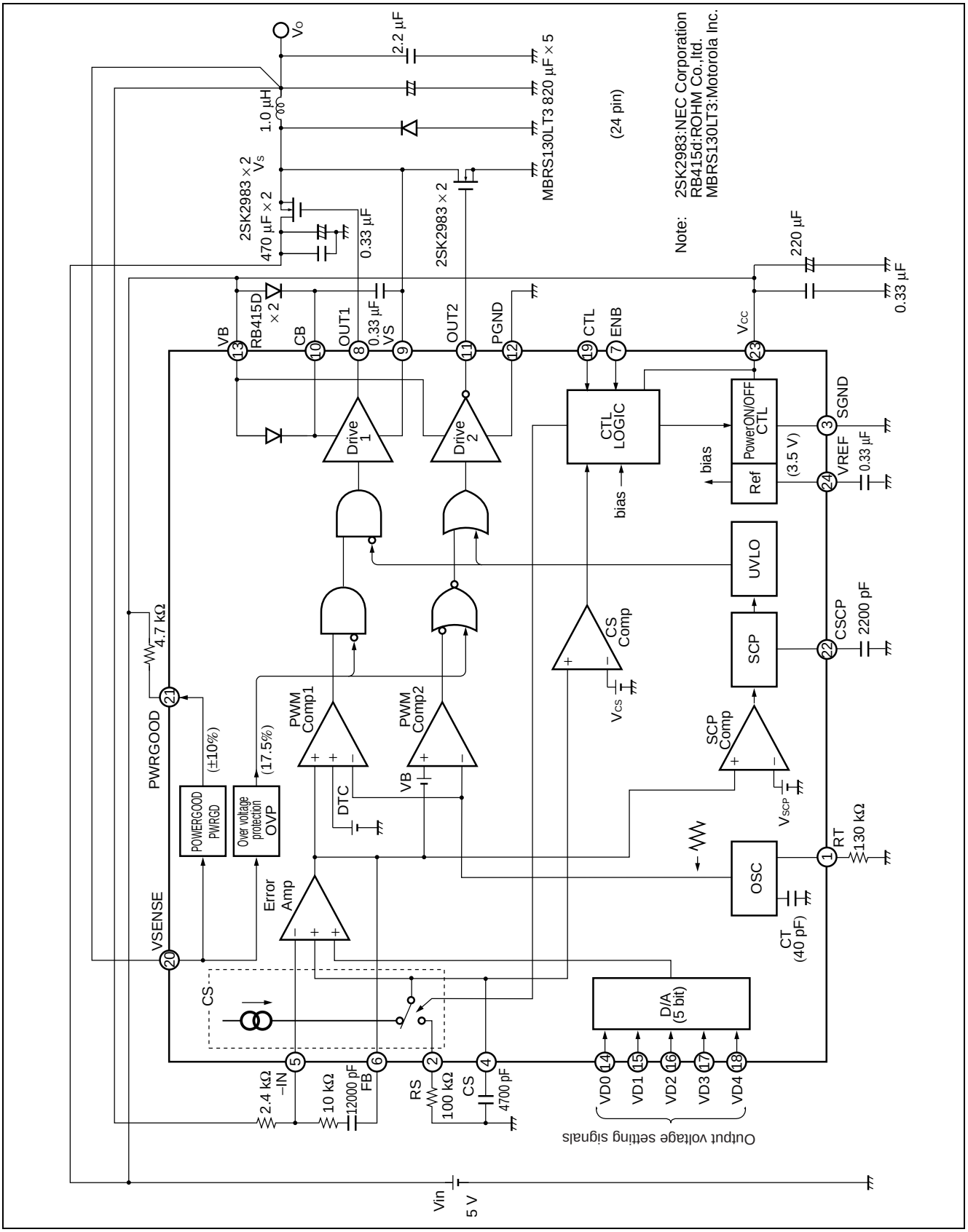
■ APPLICATION EXAMPLE



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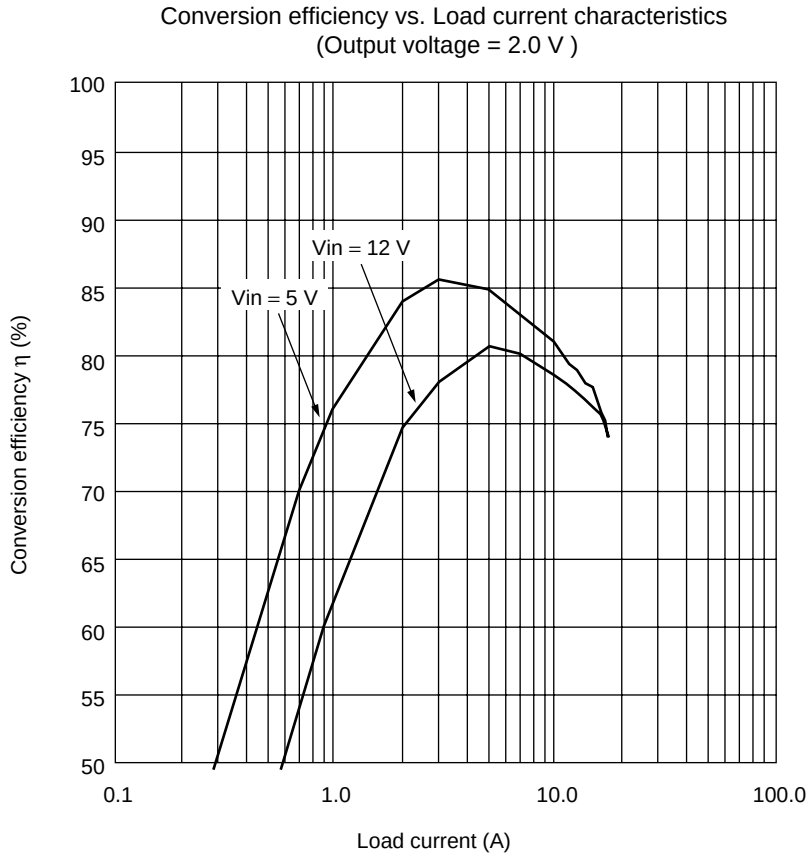
■ REFERENCE DATA



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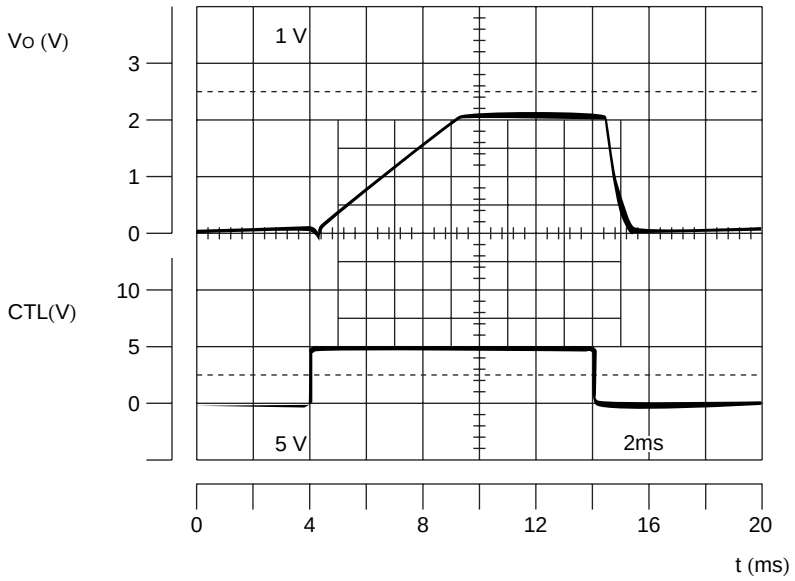
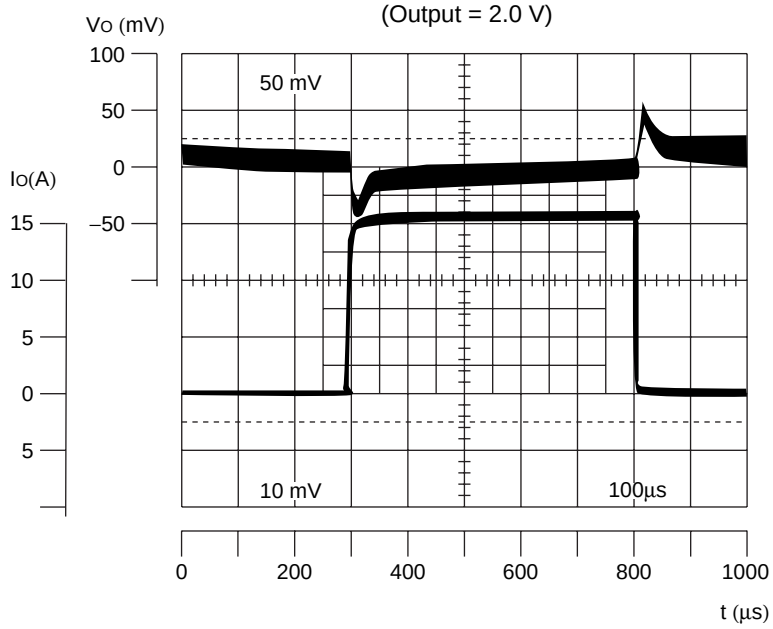
Transient response for CTL ON/OFF
(Output = 2.0 V, nonload)



Transient response for load abrupt change
(Output = 2.0 V)



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■ USAGE PRECAUTIONS

1. Device settings must not exceed absolute maximum ratings.

Usage under conditions exceeding absolute maximum ratings may permanently damage LSI devices.

Note also that in normal operation usage within recommended operating conditions is preferred, and that the reliability of LSI devices may be adversely affected when used outside these conditions.

2. Devices should be used within recommended operating conditions.

Recommended operating conditions are recommended values within which the LSI device is warranted to operate normally.

Rated values of electrical characteristics are warranted within the range of recommended operating conditions and within the conditions listed in the condition column for each parameter.

3. Printed circuit board ground lines should be designed in consideration of common impedance values.

4. Observe precautions against static electricity.

- Containers in which semiconductors are placed should either be protected against static electricity, or be of conductive material.
- After mounting of devices, use conductive bags or conductive containers when storing or transporting printed circuit boards.
- Working surfaces, tools and instruments should be properly grounded.
- Workers should be grounded by a ground line with 250 kΩ to 1 MΩ resistance in series between the worker and ground.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3870 PFV-G-BND	24-pin Plastic SSOP (FPT-24P-M03)	

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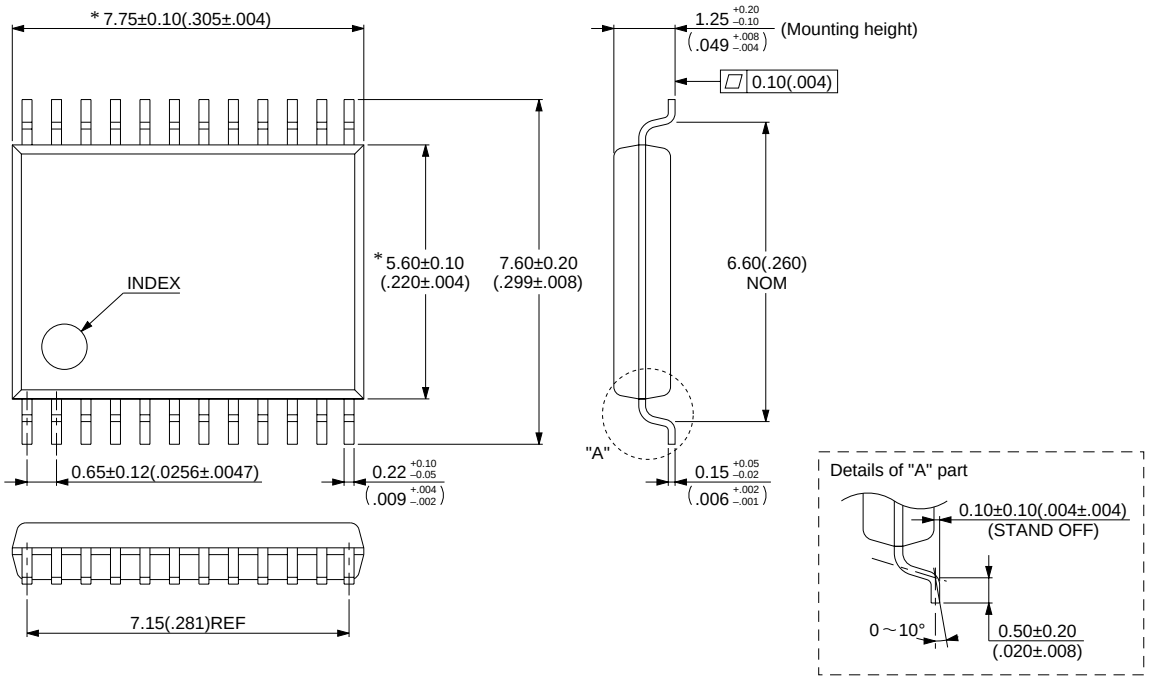
■ PACKAGE DIMENSION

24-pin Plastic SSOP
(FPT-24P-M03)

*: These dimensions do not include resin protrusion.



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Dimensions in mm (inches)

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