FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27405-1E

ASSP For Power Supply Applications

BIPOLAR

Power Voltage Monitoring IC
with Watchdog Timer

MB3793-45

■ DESCRIPTION

The MB3793 is an integrated circuit to monitor power voltage; it incorporates a watchdog timer.

A reset signal is output when the power is cut or falls abruptly. When the power recovers normally after resetting, a power-on reset signal is output to microprocessor units (MPUs). An internal watchdog timer with two inputs for system operation diagnosis can provide a fall-safe function for various application systems.

There is also a mask option that can detect voltages of 4.9 to 2.4 V in 0.1-V steps.

The model number is MB3793-45 corresponding to the detected voltage. The model number and package code are as shown below.

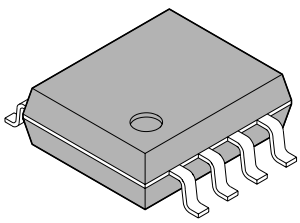
Model No.	Package code	Detection voltage
MB3793-45	3793-7	4.5 V

■ FEATURES

- Precise detection of power voltage fall: ±2.5%
- Detection voltage with hysteresis
- Low power dispersion: I_{CC} = 31 µA (reference)
- Internal dual-input watchdog timer
- Watchdog-timer halt function (by inhibition pin)
- Independently-set wacthdog and reset times

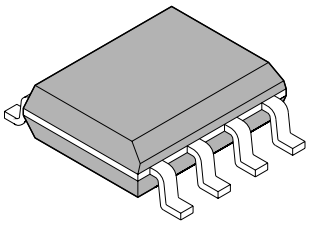
■ PACKAGE

8-pin plastic SOP



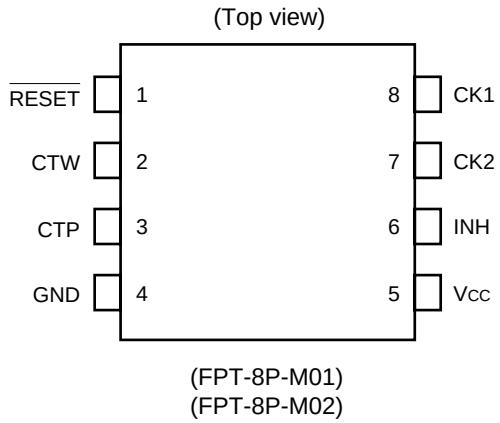
(FPT-8P-M01)

8-pin plastic SOL



(FPT-8P-M02)

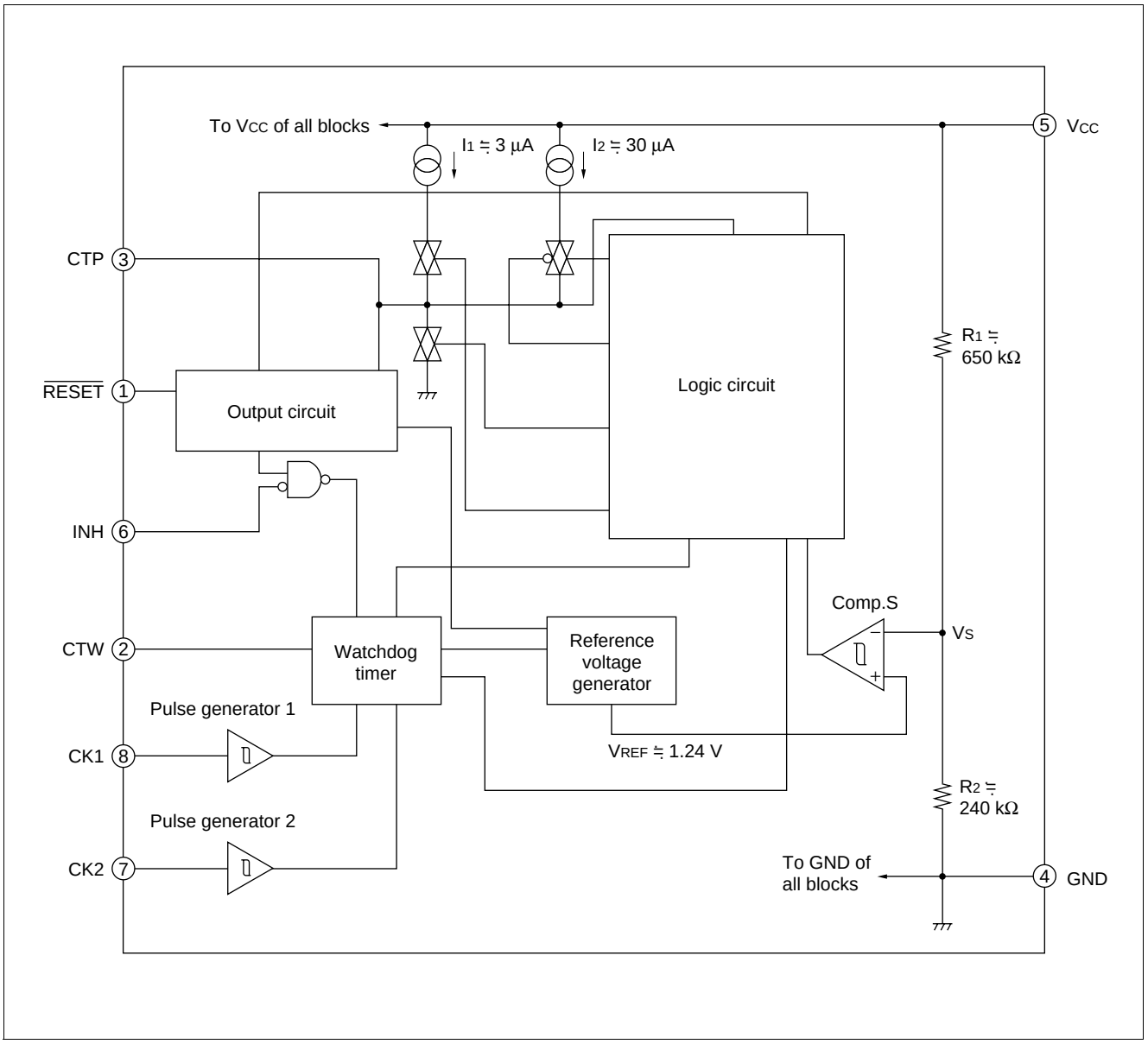
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Symbol	Descriptions	Pin no.	Symbol	Descriptions
1	$\overline{\text{RESET}}$	Outputs reset pin	5	V_{CC}	Power supply pin
2	CTW	Watchdog timer monitor time setting pin	6	INH	Inhibit pin
3	CTP	Power-on reset hold time setting pin	7	CK2	Inputs clock 2 pin
4	GND	Ground pin	8	CK1	Inputs clock 1 pin

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

1. Comp. S

Comp. S is a comparator with hysteresis to compare the reference voltage with a voltage (V_S) that is the result of dividing the power voltage (V_{CC}) by resistors 1 and 2. When V_S falls below 1.24 V, a reset signal is output. This function enables the MB3793 to detect an abnormality within 1 µs when the power is cut or falls abruptly.

2. Output circuit

The output circuit contains a $\overline{\text{RESET}}$ output control comparator that compares the voltage at the CTP pin to the threshold voltage to release the $\overline{\text{RESET}}$ output if the CTP pin voltage exceeds the threshold value.

Since the reset ($\overline{\text{RESET}}$) output buffer has CMOS organization, no pull-up resistor is needed.

3. Pulse generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 clock pins changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

4. Watchdog timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock pins to monitor a single clock pulse.

5. Inhibition pin

The inhibition (INH) pin forces the watchdog timer on/off. When this pin is High level, the watchdog timer is stopped.

6. Logic circuit

The logic circuit contains flip-flops.

Flip-flop RSFF1 controls the charging and discharging of the power-on reset time setting capacitor (C_{TP}).

Flip-flop RSFF2 turns on/off the circuit that accelerates charging of the power-on reset time setting capacitor (C_{TP}) at a reset. The RSFF2 operates only at a reset; it does not operate at a power-on reset when the power is turned on.

■ ABSOLUTE MAXIMUM RATINGS

(Ta = +25°C)

Parameter		Symbol	Conditions	Rating		Unit
				Min.	Max.	
Power supply voltage*		V_{CC}	—	–0.3	+7	V
Input voltage	CK1	V_{CK1}	—	–0.3	+7	V
	CK2	V_{CK2}	—			
	INH	I_{INH}	—			
Reset output current	$\overline{RESET}$	I_{OL} I_{OH}	—	–10	+10	mA
Allowable loss		P_D	Ta ≤ +85°C	—	200	mW
Storage temperature		Tstg	—	–55	+125	°C

*: The power supply voltage is based on the ground voltage (0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{CC}	—	1.2	—	6.0	V
Reset ($\overline{RESET}$) output current	I_{OL} I_{OH}	—	–5	—	+5	mA
Power-on reset hold time setting capacity	C_{TP}	—	0.001	—	10	µF
Watchdog-timer monitoring time setting capacity	C_{TW}	—	0.001	—	1	µF
Operating temperature	Ta	—	–40	—	+85	°C

*: The watchdog timer monitor time range depends on the rating of the setting capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{CC} = +5 V, Ta = +25°C)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Power supply current	I_{CC1}	After exit from reset		—	31	45	µA
Detection voltage	V_{SL}	V_{CC} falling	Ta = +25°C	4.40	4.50	4.60	V
			Ta = –40°C to +85°C	(4.35)*	4.50	(4.65)*	
	V_{SH}	V_{CC} rising	Ta = +25°C	4.50	4.60	4.70	V
			Ta = –40°C to +85°C	(4.45)*	4.60	(4.75)*	
Detection voltage hysteresis difference	V_{SHYS}	$V_{SH} – V_{SL}$		50	100	150	mV
Clock-input threshold voltage	V_{CIH}	CK rising		(1.4)*	1.9	2.5	V
	V_{CIL}	CK falling		0.8	1.3	(1.8)*	V
Clock-input hysteresis	V_{CHTS}	—		(0.4)*	0.6	(0.8)*	V
Inhibition-input voltage	V_{IIH}	—		3.5	—	—	V
	V_{IIL}	—		—	0	0.8	
Input current (CK1, CK2, INH)	I_{IH}	V_{CK} = 5 V		—	0	1.0	µA
	I_{IL}	V_{CK} = 0 V		–1.0	0	—	µA
Reset output voltage	V_{OH}	$I_{\overline{RESET}}$ = –5 mA		4.5	4.75	—	V
	V_{OL}	$I_{\overline{RESET}}$ = +5 mA		—	0.12	0.4	V
Reset-output minimum power voltage	V_{CCL}	$I_{\overline{RESET}}$ = +50 µA		—	0.8	1.2	V

*: The values enclosed in parentheses () are setting assurance values.

2. AC Characteristics

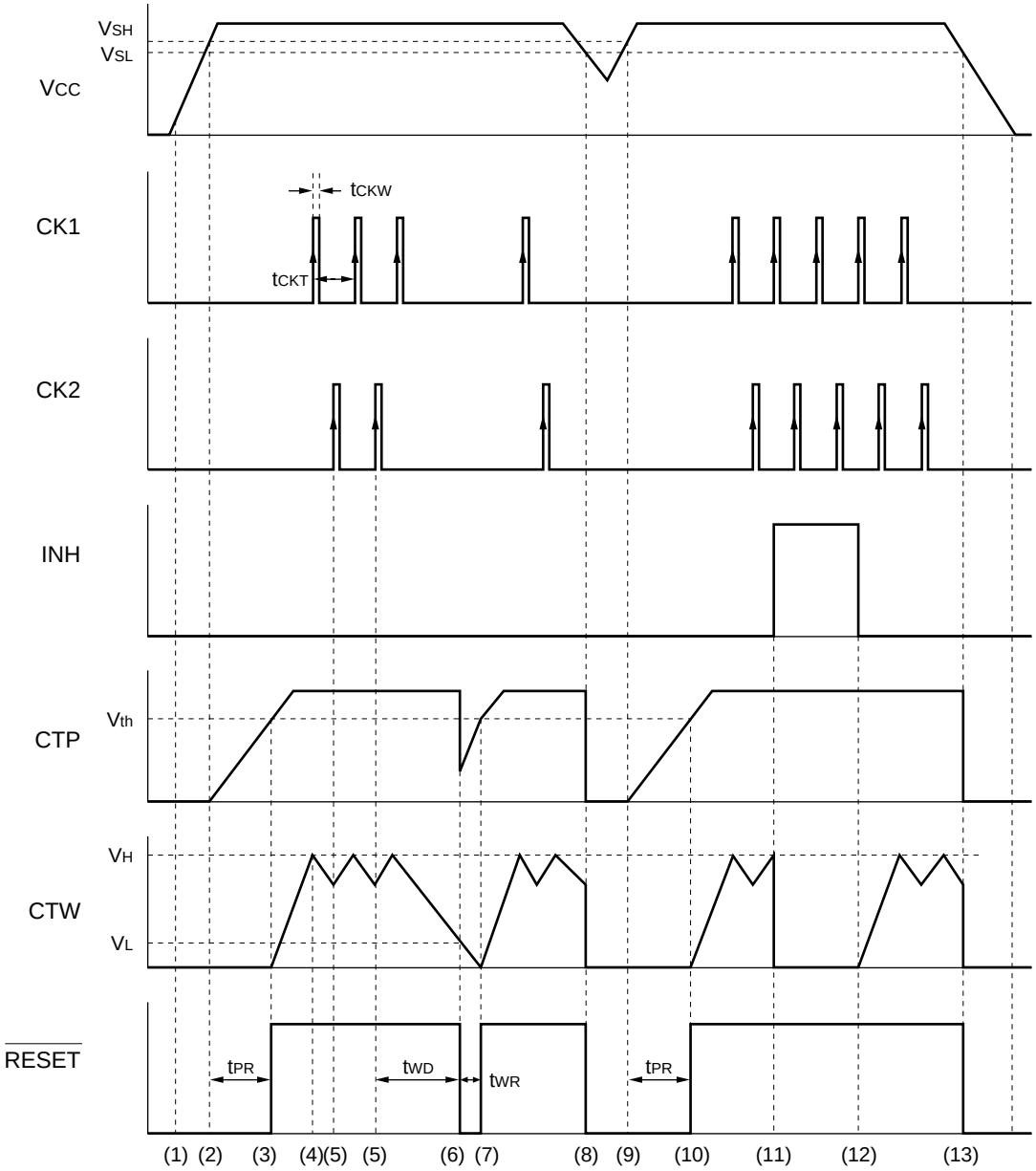
(V_{CC} = +5 V, Ta = +25°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power-on reset hold time		t_{PR}	C_{TP} = 0.1 µF	80	130	180	ms
Watchdog timer reset time		t_{WD}	C_{TW} = 0.01 µF, C_{TP} = 0.1 µF	7.5	15	22.5	ms
Watchdog timer reset time		t_{WR}	C_{TP} = 0.1 µF	5	10	15	ms
Clock input pulse width		t_{CKW}	—	500	—	—	ns
Clock input pulse cycle		t_{CKT}	—	20	—	—	µs
Reset ($\overline{RESET}$) output transition time*	Rising	t_r*	C_L = 50 pF	—	—	500	ns
	Falling	t_f*	C_L = 50 pF	—	—	500	ns

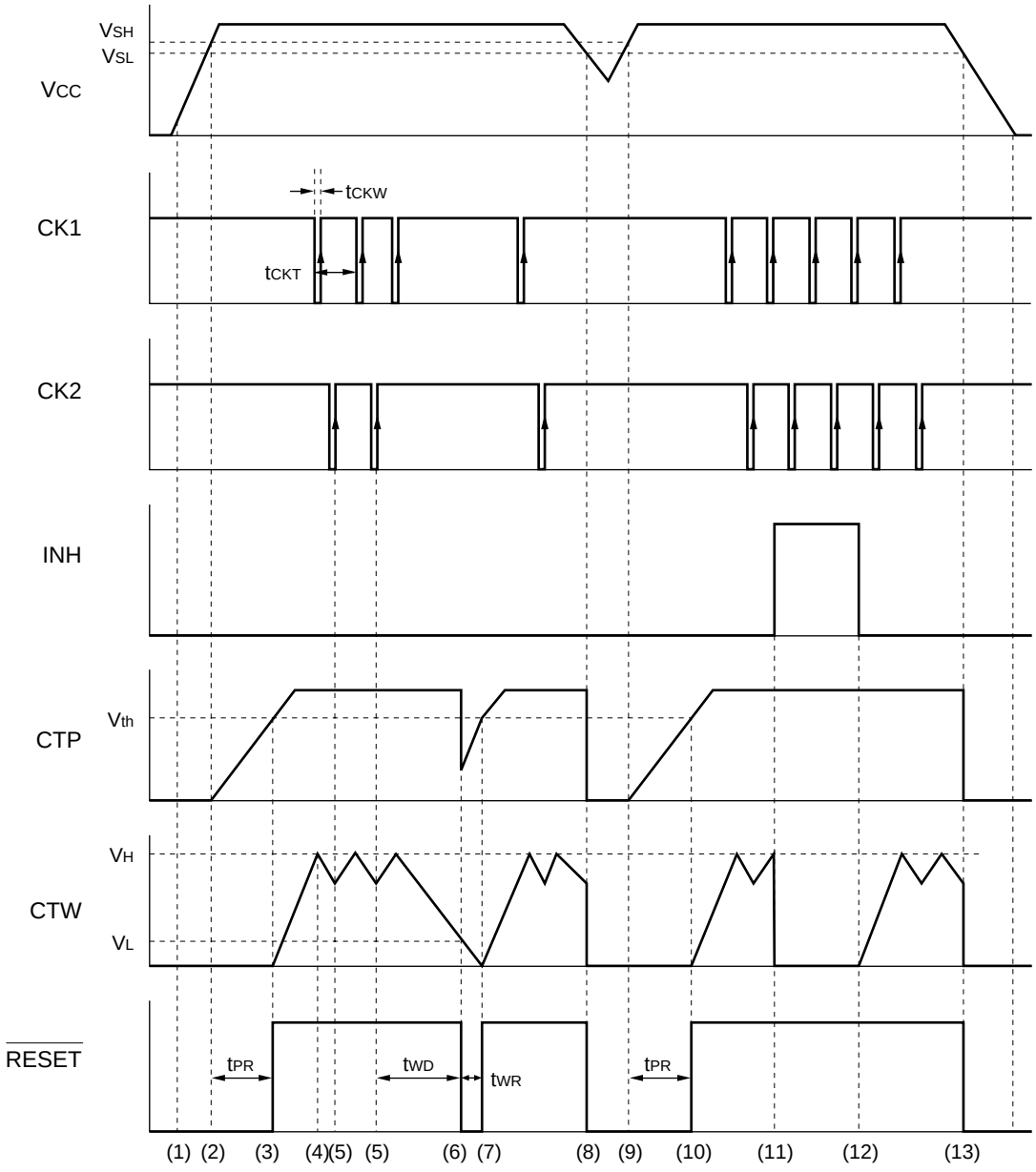
*: The voltage range is 10% to 90% at testing the reset output transition time.

■ DIAGRAM

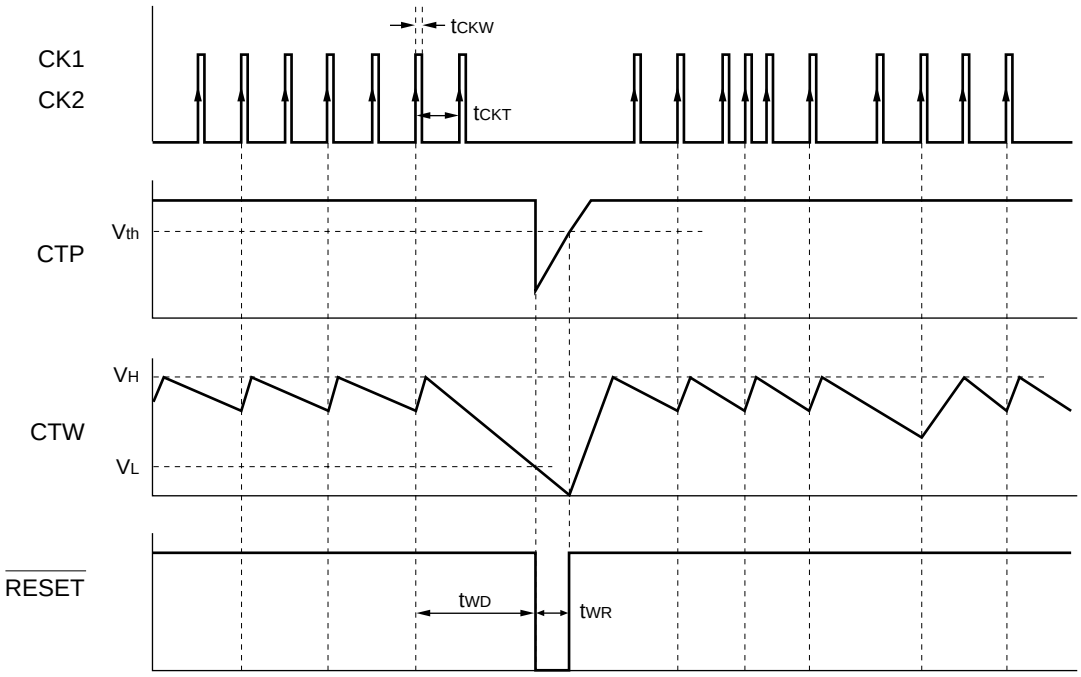
1. Basic operation (Positive clock pulse)



2. Basic operation (Negative clock pulse)

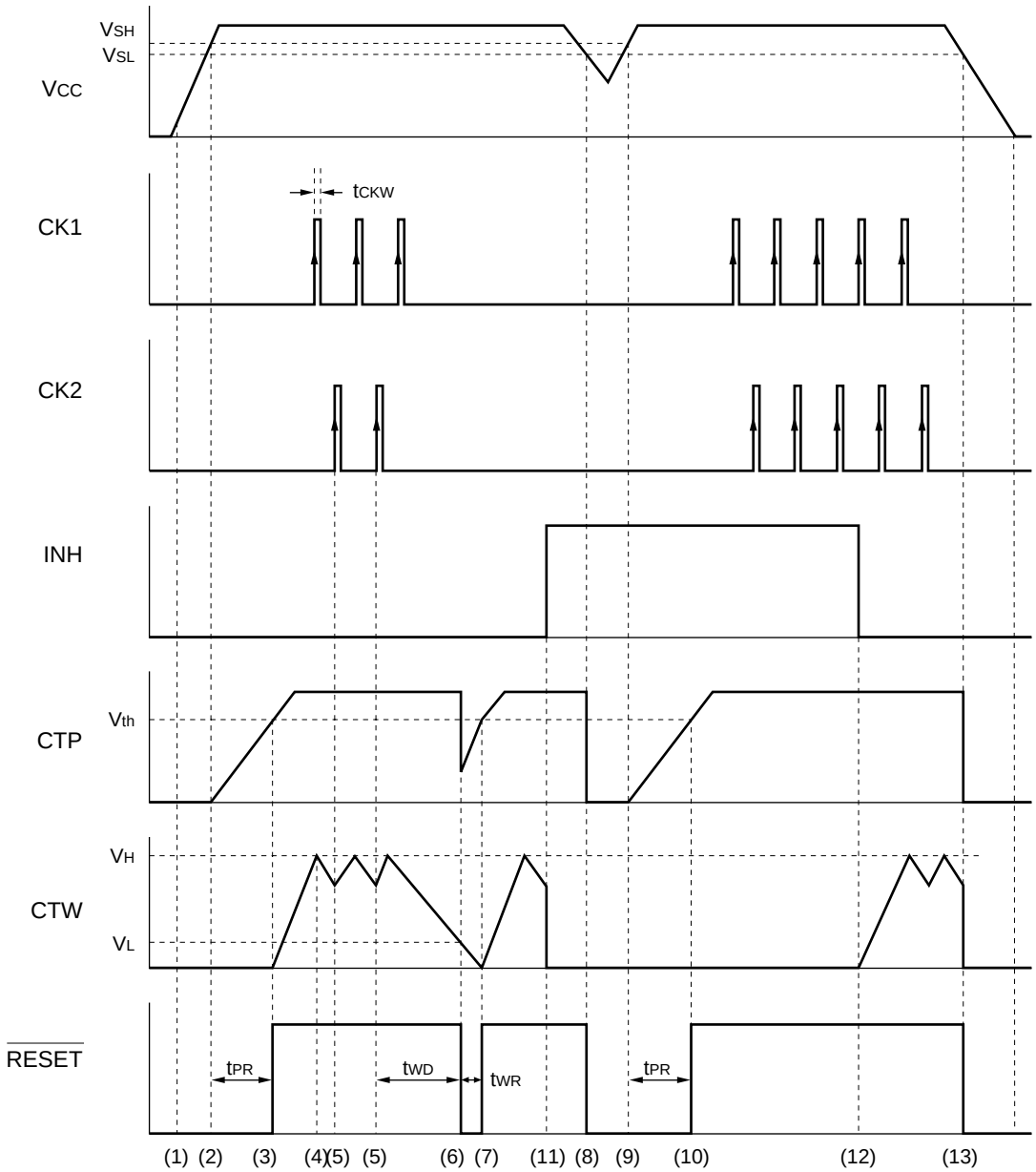


3. Single-clock input monitoring (Positive clock pulse)

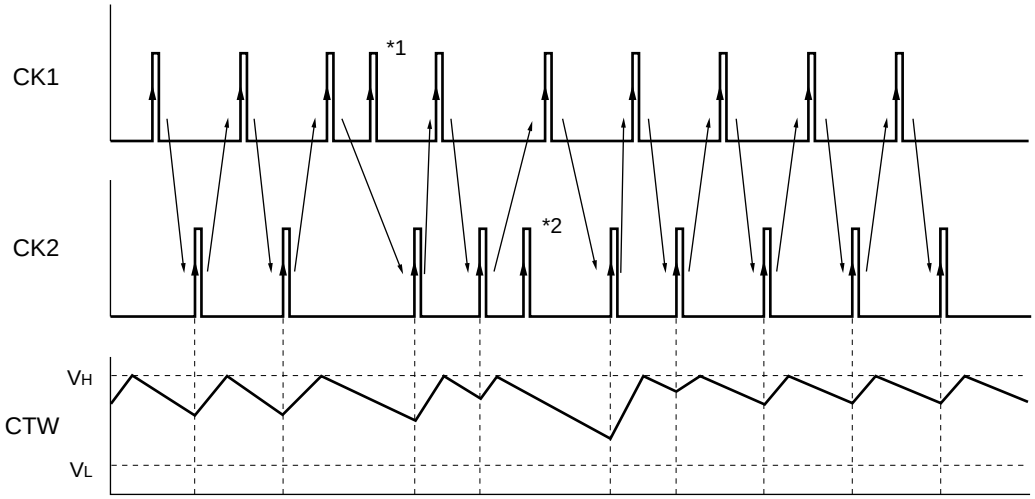


Note: The MB3793 can monitor only one clock.
The MB3793 checks the clock signal at every other input pulse. Therefore, set watchdog timer monitor time t_{WD} to the time that allows the MB3793 to monitor the period twice as long as the input clock pulse.

4. Inhibition operation (Positive clock pulse)



5. Clock pulse input supplementation (Positive clock pulse)



Note: The MB3793 watchdog timer monitors Clock1 (CK1) and Clock2 (CK2) pulses alternately.
When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (C_{TW}) switches to charging from discharging.
When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored.
In the above figure, pulse *1 and *2 are ignored.

■ OPERATION SEQUENCE

1. Positive clock pulse input

See “1. Basic operation (positive clock pulse)” under “■ DIAGRAM”.

2. Negative clock pulse input

See “2. Basic operation (negative clock pulse)” under “■ DIAGRAM”.

The MB3793 operates in the same way whether it inputs positive or negative pulses.

3. Clock monitoring

To use the MB3793 while monitoring only one clock, connect clock pins CK1 and CK2.

Although the MB3793 operates basically in the same way as when monitoring two clocks, it monitors the clock signal at every other input pulse.

See “3. Single-clock input monitoring (positive clock pulse)” under “■ DIAGRAM”.

4. Description of Operations

The numbers given to the following items correspond to numbers (1) to (13) used in “■ DIAGRAM”.

(1) The MB3793 outputs a reset signal when the supply voltage (V_{CC}) reaches about 0.8 V (V_{CCL})

(2) If V_{CC} reaches or exceeds the rise-time detected voltage V_{SH}, the MB3793 starts charging the power-on reset hold time setting capacitor C_{TP}. At this time, the output remains in a reset state. The V_{SH} value is about 4.60 V.

(3) When C_{TP} has been charged for a certain period of time T_{PR} (until the CTP pin voltage exceeds the threshold voltage (V_{th}) after the start of charging), the MB3793 cancels the reset (setting the $\overline{\text{RESET}}$ pin to “H” level from “L” level).

The V_{th} value is about 3.6 V with V_{CC} = 5.0 V

The power-on reset hold timer monitor time t_{PR} is set with the following equation:
t_{PR} (ms) ≒ A × C_{TP} (μF)
The value of A is about 1300 with V_{CC} = 5.0 V. The MB3793 also starts charging the watchdog timer monitor time setting capacitor (C_{TW}).

(4) When the voltage at the watchdog timer monitor time setting pin C_{TW} reaches the "H" level threshold voltage V_H, the C_{TW} switches from the charge state to the discharge state.
The value of V_H is always about 1.24 V regardless of the detected voltage.

(5) If the CK2 pin inputs a clock pulse (positive edge trigger) when the C_{TW} is being discharged in the CK1-CK2 order or simultaneously, the C_{TW} switches from the discharge state to the charge state.
The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses with the system logic circuit operating normally.

(6) If no clock pulse is fed to the CK1 or CK2 pin within the watchdog timer monitor time t_{WD} due to some problem with the system logic circuit, the CTW pin is set to the "L" level threshold voltage V_L or less and the MB3793 outputs a reset signal (setting the $\overline{\text{RESET}}$ pin to "L" level from "H" level).
The value of V_L is always about 0.24 V regardless of the detected voltage.

The watchdog timer monitor time t_{WD} is set with the following equation:
t_{WD} (ms) ≒ B × C_{TW} (μF)
The value of B is hardly affected by the supply voltage; it is about 1500 with V_{CC} = 5.0 V.

(7) When a certain period of time t_{WR} has passed (until the CTP pin voltage reaches or exceeds Vth again after recharging the C_{TP}), the MB3793 cancels the reset signal and starts operating the watchdog timer.
The watchdog timer monitor reset time t_{WR} is set with the following equation:
t_{WR} (ms) ≒ D x C_{TP} (μF)
The value of D is about 100 with V_{CC} = 5.0 V.
The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses. If no clock pulse is input, the MB3793 repeats operations (6) and (7).

(8) If V_{CC} is lowered to the fall-time detected voltage (V_{SL}) or less, the CTP pin voltage decreases and the MB3793 outputs a reset signal (setting the $\overline{\text{RESET}}$ pin to "L" level from "H" level).
The value of V_{SL} is 4.5 V

(9) When V_{CC} reaches or exceeds V_{SH} again, the MB3793 starts charging the C_{TP}.

(10) When the CTP pin voltage reaches or exceeds V_{th}, the MB3793 cancels the reset and restarts operating the watchdog timer. It repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses.

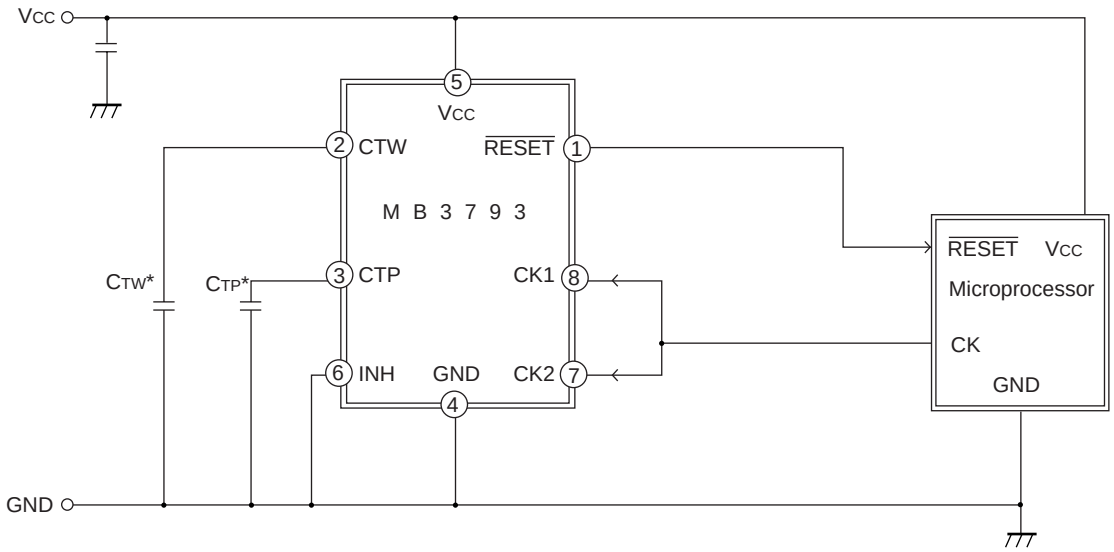
(11) Making the inhibit pin active (setting the INH pin to "H" from "L") forces the watchdog timer to stop operation. This stops only the watchdog timer, leaving the MB3793 monitoring V_{CC} (operations (8) to (10)).
The watchdog timer remains inactive unless the inhibit input is canceled.

(12) Canceling the inhibit input (setting the INH pin to "L" from "H") restarts the watchdog timer.

(13) The reset signal is output when the power supply is turned off to set V_{CC} to V_{SL} or less.

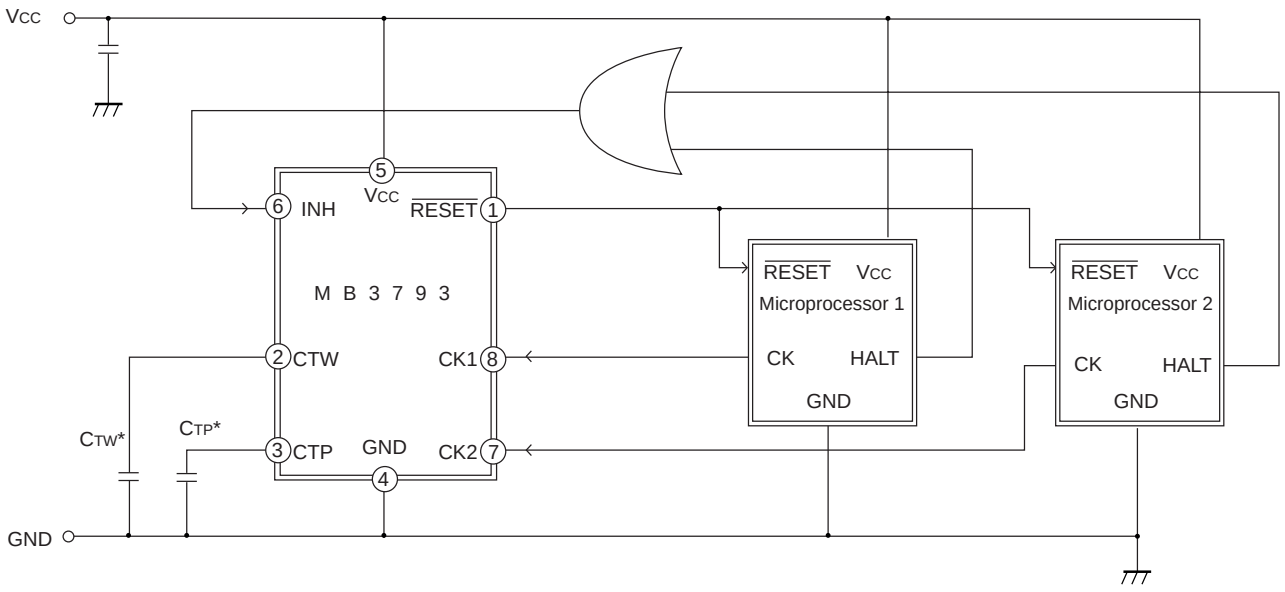
■ APPLICATION EXAMPLE

1. Supply voltage monitor and watchdog timer (1-clock monitor)



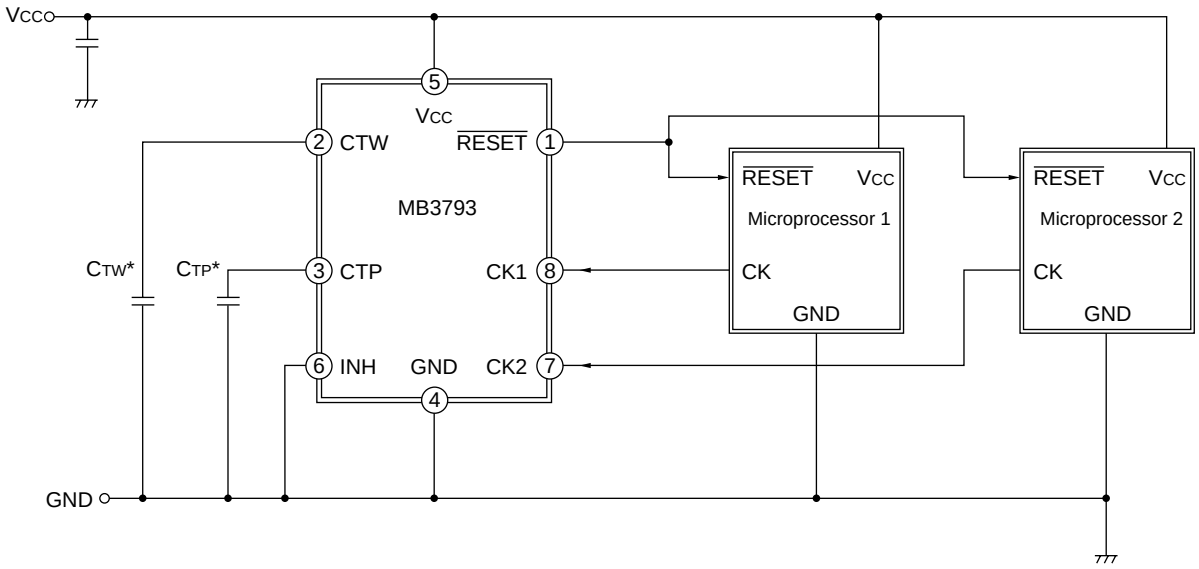
*: Use a capacitor with less leakage current.
The MB3793 monitors the clock (CK1/2) at every other input pulse.

2. Supply voltage monitor and watchdog timer stop



*: Use a capacitor with less leakage current.

■ TYPICAL APPLICATION



*: Use a capacitor with less leakage current.

1. Equation of time-setting capacitances (C_{TP} and C_{TW}) and set time

t_{PR} [ms] ≒ A × C_{TP} [µF]

t_{WD} [ms] ≒ B × C_{TW} [µF] + C × C_{TP} [µF]

However, when $\frac{C_{TP}}{C_{TW}} \leq$ about 10, t_{WD} [ms] ≒ B × C_{TW} [µF]

t_{WR} [ms] ≒ D × C_{TP} [µF]

Values of A, B, C, and D

A	B	C	D	Remark
1300	1500	3	100	V_{CC} = 5.0 V

2. (Example) when C_{TP} = 0.1 µF and C_{TW} = 0.01 µF

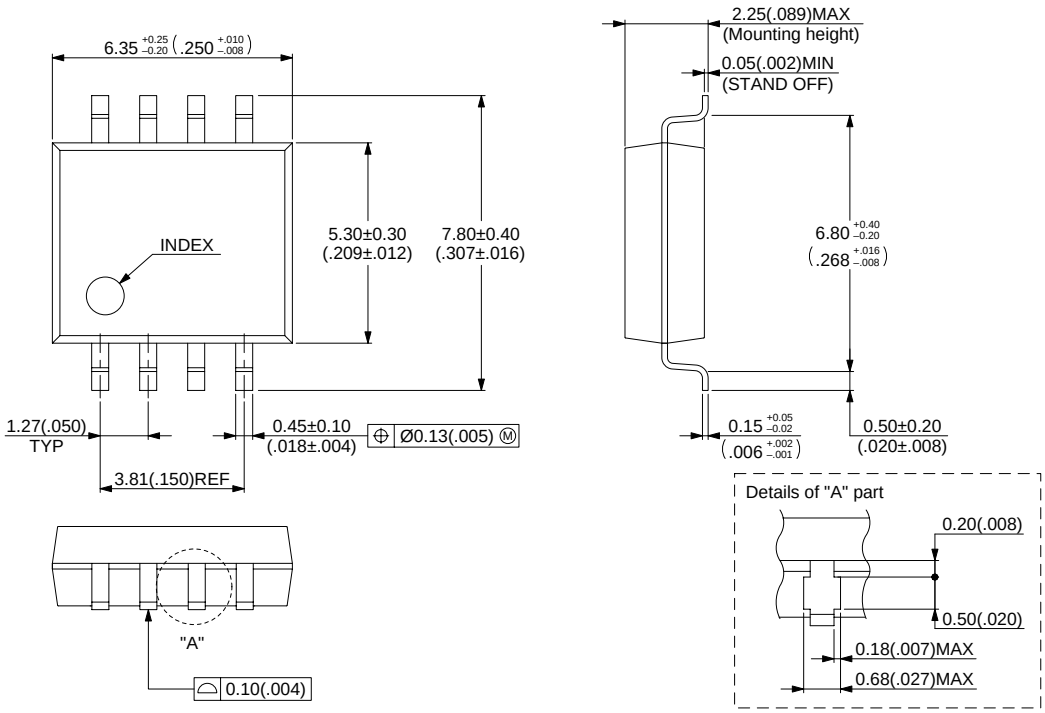
time (ms)	t_{PR}	≒ 130
	t_{WD}	≒ 15
	t_{WR}	≒ 10

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3793-45PF	8-pin Plastic SOP (FPT-8P-M01)	
MB3793-45PNF	8-pin Plastic SOL (FPT-8P-M02)	

■ PACKAGE DIMENSIONS

8-pin plastic SOP
(FPT-8P-M01)



Dimensions in mm (inches)

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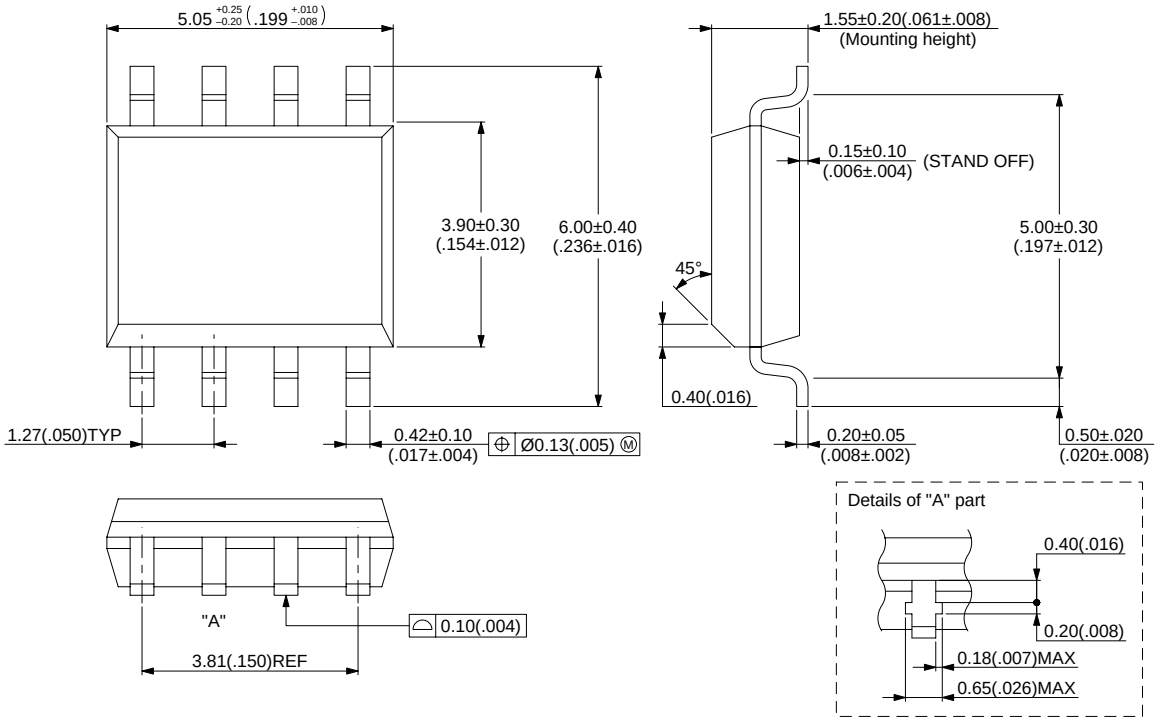
8-pin plastic SOL
(FPT-8P-M02)



Dimensions in mm (inches)

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