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# Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MP3V5004G series piezoresistive transducer is a state-of-the-art monolithic silicon pressure sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This sensor combines a highly sensitive implanted strain gauge with advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

#### **Features**

- Temperature Compensated over 10° to 60°C
- Available in Gauge Surface Mount (SMT) or Through-Hole (DIP) Configurations
- Durable Thermoplastic (PPS) Package

#### **Typical Applications**

- Washing Machine Water Level
- · Ideally Suited for Microprocessor or Microcontroller-Based Systems

ORDERING INFORMATION <sup>(1)</sup>						
Device Type						
Through- Hole	482C	MP3V5004GC7U	Rails	MP3V5004G		
Surface	482A	MP3V5004GC6U	Rails	MP3V5004G		
Mount	482A	MP3V5004GC6T1	Tape & Reel	MP3V5004G		
	1351	MP3V5004DP	Trays	MP3V5004G		
	1368	MP3V5004GVP	Trays	MP3V5004G		
	1369	MP3V5004GP	Trays	MP3V5004G		

MP3V5004G series pressure sensors are available with a pressure port. Three
packing options are offered for the surface mount configuration.

# MP3V5004G SERIES

INTEGRATED PRESSURE SENSOR 0 TO 3.92 kPA (0 TO 400 mm  $\rm H_2O$ ) 0.6 TO 3.0 V OUTPUT

# SMALL OUTLINE PACKAGES THROUGH-HOLE



MP3V5004GC7U CASE 482C-03

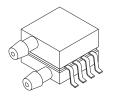
PIN NUMBERS <sup>(1)</sup>				
1	N/C	5	N/C	
2	V <sub>S</sub>	6	N/C	
3	GND	7	N/C	
4	V <sub>OUT</sub>	8	N/C	

 Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.

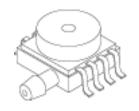
# SMALL OUTLINE PACKAGES SURFACE MOUNT



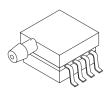
MP3V5004GC6U CASE 482A-01



MP3V5004DP CASE 1351-01



MP3V5004GVP CASE 1368-01



MP3V5004GP CASE 1369-01



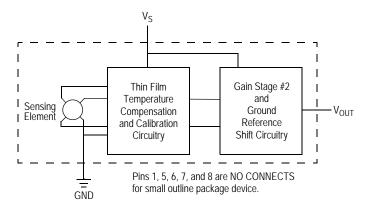


Figure 1. Fully Integrated Pressure Sensor Schematic

Table 1. Maximum Ratings<sup>(1)</sup>

Rating	Symbol	Value	Unit
Maximum Pressure (P1 > P2)	P <sub>MAX</sub>	16	kPa
Storage Temperature	T <sub>STG</sub>	-30 to +100	°C
Operating Temperature	T <sub>A</sub>	0 to +85	°C

<sup>1.</sup> Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Table 2. Operating Characteristics ( $V_S = 3.0 V_{DC}$ ,  $T_A = 25$ °C unless otherwise noted, P1 > P2)

	Characteristic	Symbol	Min	Тур	Max	Units
Pressure Range		P <sub>OP</sub>	0	_	3.92 400	kPa mm H <sub>2</sub> O
Supply Voltage <sup>(1)</sup>		Vs	2.7	3.0	3.3	V <sub>DC</sub>
Supply Current		I <sub>S</sub>	_	_	10	mAdc
Span at 306 mm H <sub>2</sub> O (	(3 kPa) <sup>(2)</sup>	V <sub>FSS</sub>	_	1.8	_	V
Offset <sup>(3) (4)</sup>		V <sub>OFF</sub>	0.45	0.6	0.75	V
Sensitivity		V/P	_	0.6 5.9	_	V/kPa mV/mm H <sub>2</sub> O
Accuracy <sup>(4) (5)</sup>	0 to 100 mm H <sub>2</sub> O (10 to 60°C) 100 to 400 mm H <sub>2</sub> O (10 to 60°C)	1 1	_ _		±1.5 ±2.5	%V <sub>FSS</sub> %V <sub>FSS</sub>

- 1. Device is ratiometric within this specified excitation range.
- 2. Span is defined as the algebraic difference between the output voltage at specified pressure and the output voltage at the minimum rated pressure.
- 3. Offset (Voff) is defined as the output voltage at the minimum rated pressure.
- 4. Accuracy (error budget) consists of the following:
  - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
  - Temperature Hysteresis:Output deviation at any temperature within the operating temperature range, after the temperature is cycled to
    and from the minimum or maximum operating temperature points, with zero differential pressure applied.
  - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the

minimum or maximum rated pressure, at 25°C.

Offset Stability: Output deviation, after 1000 temperature cycles, –30 to 100°C, and 1.5 million pressure cycles, with minimum

rated pressure applied.

- TcSpan: Output deviation over the temperature range of 10 to 60°C, relative to 25°C.
- TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 10 to 60°C, relative to 25°C.
- Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of V<sub>FSS</sub>, at 25°C.
- 5. Auto Zero at Factory Installation: Due to the sensitivity of the MP3V5004G, external mechanical stresses and mounting position can affect the zero pressure output reading. Autozeroing is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations. Reference AN1636 for specific information. The specified accuracy assumes a maximum temperature change of ± 5°C between autozero and measurement.

#### ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION AND SIGNAL CONDITIONING

www.Data The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the gauge configuration in the basic chip carrier (Case 482). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MP3V5004G series sensor operating characteristics are based on use of dry air as pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Internal reliability and qualification test for dry air, and other media, are available

from the factory. Contact the factory for information regarding media tolerance in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the output of the MP3V5004G to the A/D input of the microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 shows the sensor output signal relative to pressure input. Typical, minimum and maximum output curves are shown for operation over a temperature range of 10°C to 60°C using the decoupling circuit shown in Figure 3 The output will saturate outside of the specified pressure range.

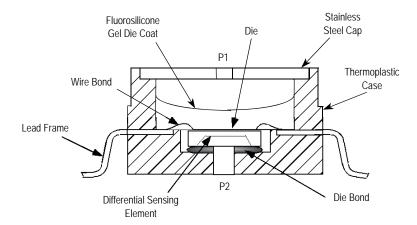


Figure 2. Cross-Sectional Diagram (Not to Scale)

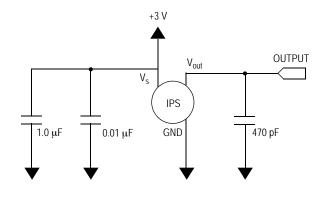


Figure 3. Recommended Power Supply Decoupling and Output Filtering.

(For additional output filtering, please refer to Application Note AN1646.)

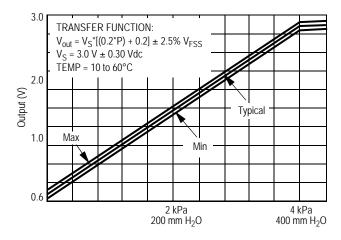


Figure 4. Output versus Pressure Differential at  $\pm 2.5\%$  V<sub>FSS</sub>

(See Note 5 in Operating Characteristics)

# PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

www.DataEreescale:Semiconductor designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing silicone gel which isolates the die from the environment. The

Freescale Semiconductor pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using the table below.

Part Number	Case Type	Pressure (P1) Side Identifier
MP3V5004GC6U/T1	482A	Side with Port Attached
MP3V5004GC7U	482C	Side with Port Attached
MP3V5004GP	1369	Side with Port Attached
MP3V5004DP	1351	Side with Port Marking
MP3V5004GVP	1368	Stainless Steel Cap

# INFORMATION FOR USING THE SMALL OUTLINE PACKAGE (CASE 482)

# MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface

between the board and the package. With the correct footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

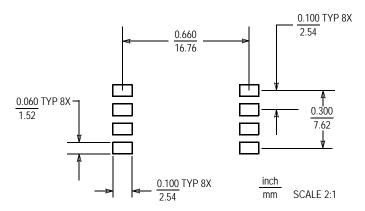
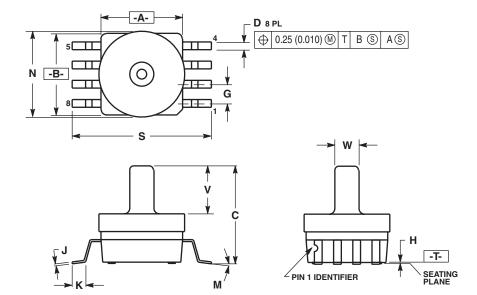


Figure 5. SOP Footprint (Case 482)

# **PACKAGE DIMENSIONS**



- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: INCH.

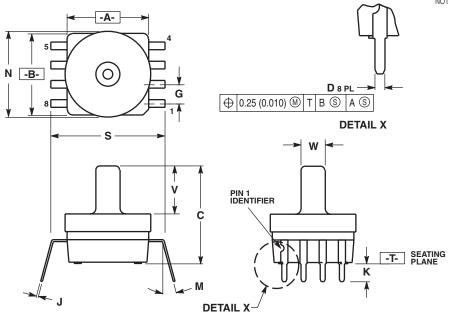
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).

  5. ALL VERTICAL SURFACES 5

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
Н	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
٧	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

**CASE 482A-01 ISSUE A SMALL OUTLINE PACKAGE SURFACE MOUNT** 



#### NOTES:

- ES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: INCH.

  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

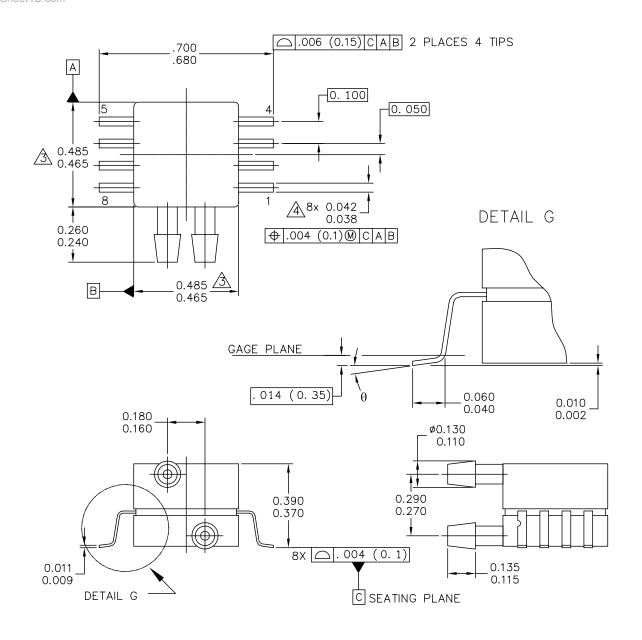
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).

  5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

  6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.500	0.520	12.70	13.21
D	0.026	0.034	0.66	0.864
G	0.100	BSC	2.54 BSC	
J	0.009	0.011	0.23	0.28
K	0.100	0.120	2.54	3.05
M	0°	15°	0°	15°
N	0.444	0.448	11.28	11.38
S	0.540	0.560	13.72	14.22
٧	0.245	0.255	6.22	6.48
w	0.115	0.125	2.92	3.17

**CASE 482C-03 ISSUE B SMALL OUTLINE PACKAGE THROUGH-HOLE** 



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8 LD SNSR, DUAL	PORT	CASE NUMBER	2: 1351–01	27 JUL 2005
		STANDARD: NO	N-JEDEC	

PAGE 1 OF 2

CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE SURFACE MOUNT

# **PACKAGE DIMENSIONS**

#### NOTES:

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.
- DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

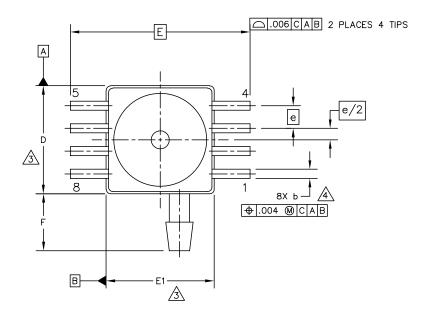
STYLE 1:		STYLE 2:		
PIN 1:	GND	PIN	1:	N/C
PIN 2:	+Vout	PIN	2:	٧s
PIN 3:	Vs	PIN	3:	GND
PIN 4:	-Vout	PIN	4:	Vout
PIN 5:	N/C	PIN	5:	N/C
PIN 6:	N/C	PIN	6:	N/C
PIN 7:	N/C	PIN	7:	N/C
PIN 8:	N/C	PIN	8:	N/C

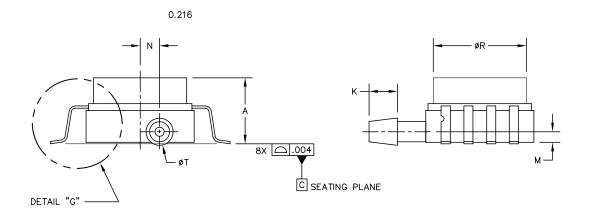
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TITLE:		DOCUMENT NO	): 98ASA99255D	REV: A
8 LD SNSR, DUAL	PORT	CASE NUMBER	R: 1351–01	27 JUL 2005
		STANDARD: NO	N-JEDEC	

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### CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE

# **PACKAGE DIMENSIONS**

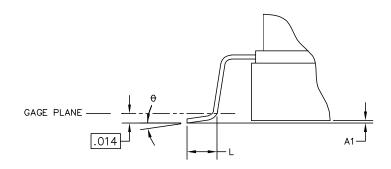




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8 LD SOP, GVP		CASE NUMBER	2: 1368–01	23 MAY 2005
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CASE 1368-01 ISSUE B SMALL OUTLINE PACKAGE SURFACE MOUNT



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8 LD SOP, GVP		CASE NUMBER	: 1368–01	23 MAY 2005
		STANDARD: NO	N-JEDEC	

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CASE 1368-01 ISSUE B SMALL OUTLINE PACKAGE SURFACE MOUNT

# **PACKAGE DIMENSIONS**

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

THIS DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

 $\stackrel{\blacktriangle}{\triangle}$  THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

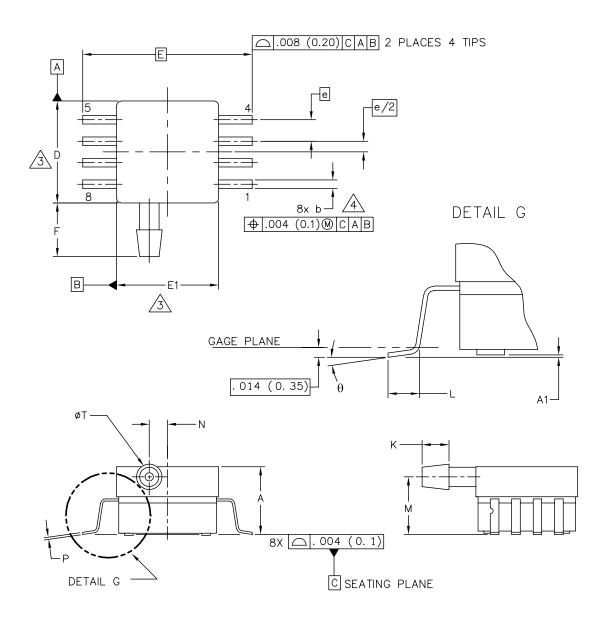
STYLE 1:		STYLE 2:		
PIN 1:	GND	PIN	1:	N/C
PIN 2:	+Vout	PIN	2:	٧s
PIN 3:	Vs	PIN	3:	GND
PIN 4:	-Vout	PIN	4:	Vout
PIN 5:	N/C	PIN	5:	N/C
PIN 6:	N/C	PIN	6:	N/C
PIN 7:	N/C	PIN	7:	N/C
PIN 8:	N/C	PIN	8:	N/C

	INCHES		MILLIMETERS			INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
Α	.280	.300	7.11	7.62	R	.405	.415	10.28	10.54
A1	.002	.010	0.05	0.25	θ	0.	7*	0.	7*
b	.038	.042	0.96	1.07	-				
D	.465	.485	11.81	12.32	-				
Ε	.690 BSC 17.52 BSC		-						
E1	.465	.485	11.85	12.32	-				
е	.100 BSC		2.54 BSC		-				
F	.240	.260	6.10	6.60	-				
Κ	.115	.135	2.92	3.43	-				
L	.040	.060	1.02	1.52	-				
М	.035	.055	1.90	2.41	-				
N	.075	.095	0.89	1.39	-				
Р	.009	.011	0.23	0.28	-				
Т	.110	.130	2.79	3.30	-				

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8 LD SOP, GVI	<b>&gt;</b>	CASE NUMBER	2: 1368–01	23 MAY 2005
		STANDARD: NO	N-JEDEC	

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**CASE 1368-01 ISSUE B SMALL OUTLINE PACKAGE SURFACE MOUNT** 



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## CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE

# **PACKAGE DIMENSIONS**

#### NOTES:

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- △ DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.

  MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.
- DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

	INCHES		MILLIMETERS			INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
Α	. 300	. 330	7. 11	7. 62	θ	0°	7°	0°	7 <b>°</b>
A 1	. 002	. 010	0. 05	0. 25	-				
b	. 038	. 042	0. 96	1. 07	_				
D	. 465	. 485	11. 81	12. 32	-				
E	E .717 BSC 18		.21 BSC	_					
E1	. 465	. 485	11. 81	12. 32	_				
e	. 100	BSC	2.	54 BSC	-				
F	. 245	. 255	6. 22	6. 47	_				
K	. 120	. 130	3. 05	3. 30	-				
L	. 061	. 071	1. 55	1. 80	_				
М	. 270	. 290	6. 86	7. 36	_				
N	. 080	. 090	2. 03	2. 28	_				
Р	. 009	. 011	0. 23	0. 28	-				
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8 LD SOP, SIDE PORT				CASE NUMBER: 1369-01 24 MAY 2005				24 MAY 2005	
				STANDARD: NON-JEDEC					

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CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE

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