FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-29122-1E

Spread Spectrum Clock Generator

MB88162

■ DESCRIPTION

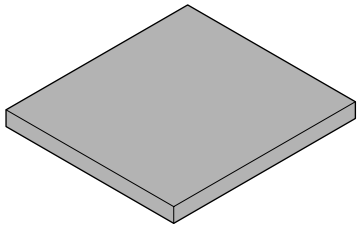
MB88162 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator.

■ FEATURES

- Input frequency : 12 MHz to 28 MHz (Multiplied by 1), 20 MHz to 42 MHz (Multiplied by 4)
- Multiplication rate : 1, 4
- Output frequency : 12 MHz to 28 MHz (Multiplied by 1), 80 MHz to 168 MHz (Multiplied by 4)
- Modulation rate : no modulation, ±0.5%, ±1.0%, ±2.0%, −1.0%, −2.0%, −4.0% (The terminal can be selected.)
- Equipped with oscillation circuit : Range of oscillation 12 MHz to 42 MHz
- Built-in oscillation stabilization capacitance : 4 pF (Typ)
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Less than 100 ps
- Low power consumption by CMOS process : 7.0 mA (24 MHz : no load, Typ-sample, Typ-condition)
- Power supply voltage : 2.7 V to 3.6 V (Multiplied by 1), 3.0 V to 3.6 V (Multiplied by 4)
- Operating temperature : − 40 °C to + 85 °C
- Package : BCC 18-pin

■ PACKAGE

18-pin plastic BCC

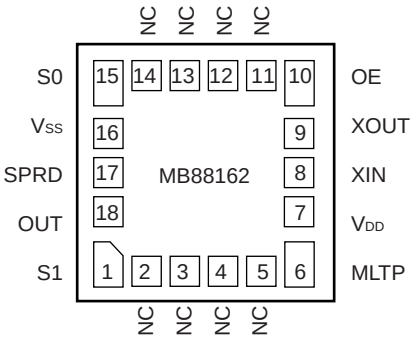


(LCC-18P-M05)

FUJITSU

■ PIN ASSIGNMENT

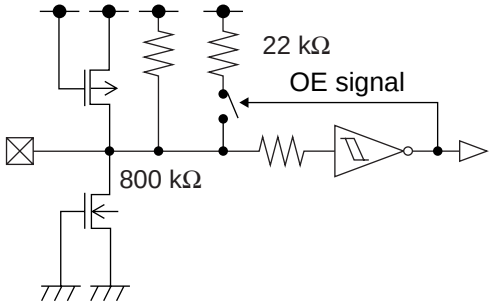
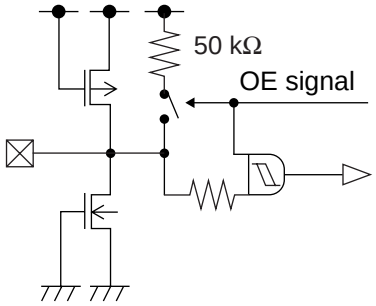
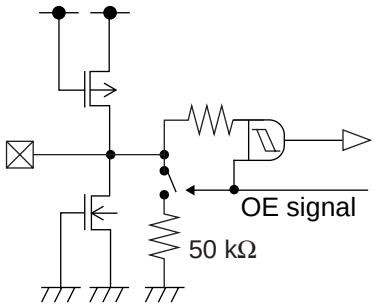
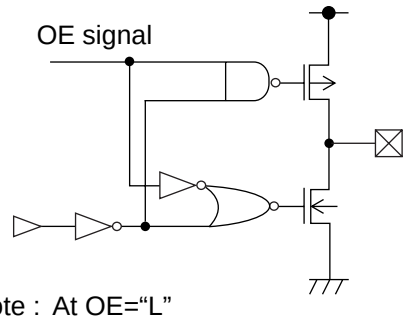
(TOP VIEW)



■ PIN DESCRIPTION

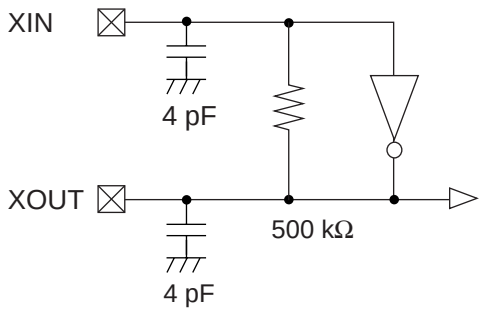
Pin no.	Pin name	I/O	Description
1	S1	I	Modulation rate setting pin (with pull-up resistance)
2	NC	—	Non-connection pin (do not connect anything)
3	NC	—	Non-connection pin (do not connect anything)
4	NC	—	Non-connection pin (do not connect anything)
5	NC	—	Non-connection pin (do not connect anything)
6	MLTP	I	Multiplication rate setting pin (with pull-down resistance)
7	V_{DD}	—	Power supply voltage pin
8	XIN	I	Resonator connection pin/clock input pin
9	XOUT	O	Resonator connection pin
10	OE	I	Clock output enable pin (with pull-up resistance)
11	NC	—	Non-connection pin (do not connect anything)
12	NC	—	Non-connection pin (do not connect anything)
13	NC	—	Non-connection pin (do not connect anything)
14	NC	—	Non-connection pin (do not connect anything)
15	S0	I	Modulation rate setting pin (with pull-up resistance)
16	V_{SS}	—	GND pin
17	SPRD	I	Modulation type setting pin (with pull-up resistance)
18	OUT	O	Modulation clock output pin (OE= “L” Hi-Z output)

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
OE	 Note : At OE="L" 22kΩ Pull Up cut	• With pull-up resistor The value of pull-up resistor is switched by the input level of OE signal. 800 kΩ at OE= "L" (Typ) 22 kΩ at OE= "H" (Typ) • CMOS hysteresis input
S0, S1, SPRD	 Note : At OE="L" Pull Up cut	• With pull-up resistor 50 kΩ (Typ) • CMOS hysteresis input • Pull-up resistor is disconnected at OE= "L", and internal signal is fixed to "L".
MLTP	 Note : At OE="L" Pull Down cut	• With pull-down resistor 50 kΩ (Typ) • CMOS hysteresis input • Pull-down resistor is disconnected at OE= "L", and internal signal is fixed to "L".
OUT	 Note : At OE="L" Hi-Z output	• CMOS output • I_{OL} = 8.0 mA • Hi-Z output at OE = "L"

(Continued)

(Continued)

Pin	Circuit type	Remarks
XIN, XOUT		• Oscillation circuit • Built-in feedback resistance : 500 kΩ (Typ) • Built-in oscillation stabilization capacitance : 4 pF (Typ)

■ HANDLING DEVICES

Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than power supply voltage or a voltage lower than GND is applied to an input or output pin or (b) a voltage higher than the rating is applied between power supply and GND. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

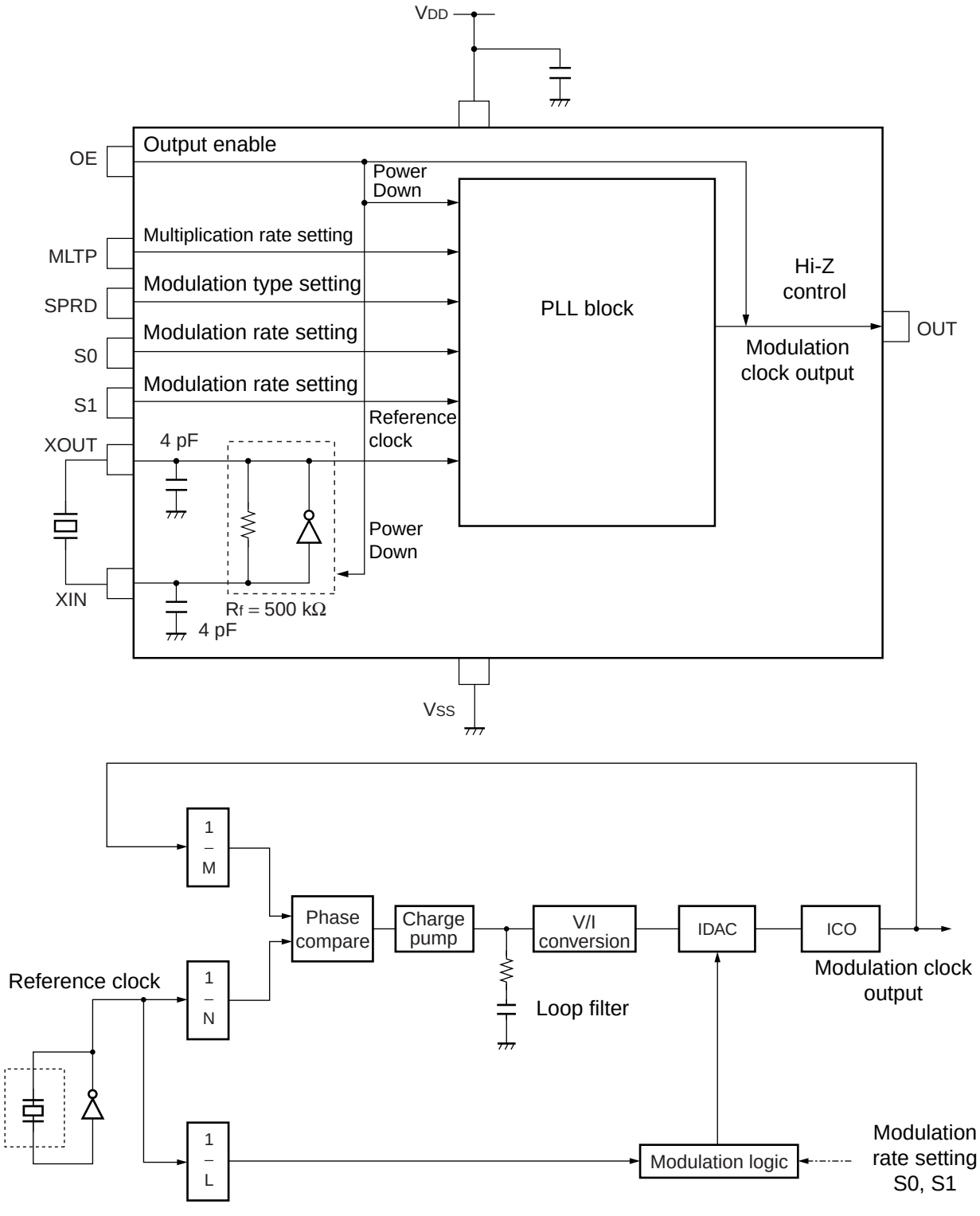
We recommend connecting electrolytic capacitor (about 10 µF) and the ceramic capacitor (about 0.01 µF) in parallel between power supply and GND near the device, as a bypass capacitor.

Oscillation circuit

Noise near the XIN pin and XOUT pin may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN pin or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN pin and XOUT pin with ground.

■ BLOCK DIAGRAM



MB88162 PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

■ PIN SETTING

After the pin setting is changed, the stabilization wait time of the modulation clock is required. The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time in "• AC Characteristics" in ■ ELECTRICAL CHARACTERISTICS.

Each setting pin contains the pull-up resistor or pull-down resistor. Therefore, these pins is set to default state for input opened.

MLTP multiplication setting

MLTP	Multiplication rate	Input Frequency	Output Frequency	Remarks
L	Multiplied by 1	12 MHz to 28 MHz	12 MHz to 28 MHz	Default
H	Multiplied by 4	20 MHz to 42 MHz	80 MHz to 168 MHz	—

Note : Set MLTP pin to "L" for input opened because MLTP pin has the pull-down resistor.

OE clock output enable

OE	Status	Remarks
L	Modulation clock output (OUT pin) Hi-Z/Power down status	—
H	Operation status	Default

Note : When OE pin is set to "L", all oscillation circuits/PLL stop and enter power down mode, low-power consumption mode. Modulation clock output (OUT pin) becomes Hi-Z state during the power down. Set OE pin to "H" for input opened because OE pin has the pull-up resistor.

SPRD modulation type setting

SPRD	Modulation type	Remarks
L	Center spread	—
H	Down spread	Default

Note : Set SPRD pin to "H" for input opened because SPRD pin has the pull-up resistor.

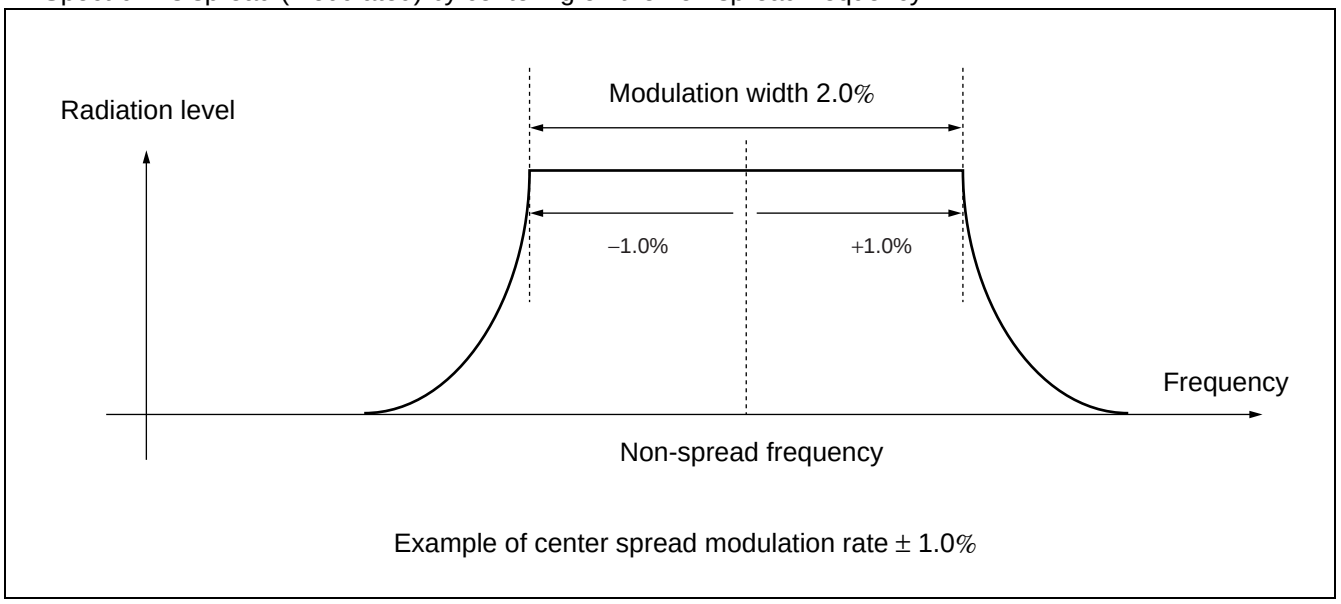
S0/S1 modulation rate setting

S1	S0	Modulation rate		Remarks
		At down spread	At center spread	
L	L	No modulation	No modulation	—
L	H	– 1.0%	± 0.5%	—
H	L	– 2.0%	± 1.0%	—
H	H	– 4.0%	± 2.0%	Default

Note : Set S1 and S0 pins to "H" for input opened because the pins have the pull-up resistor.

• Center spread

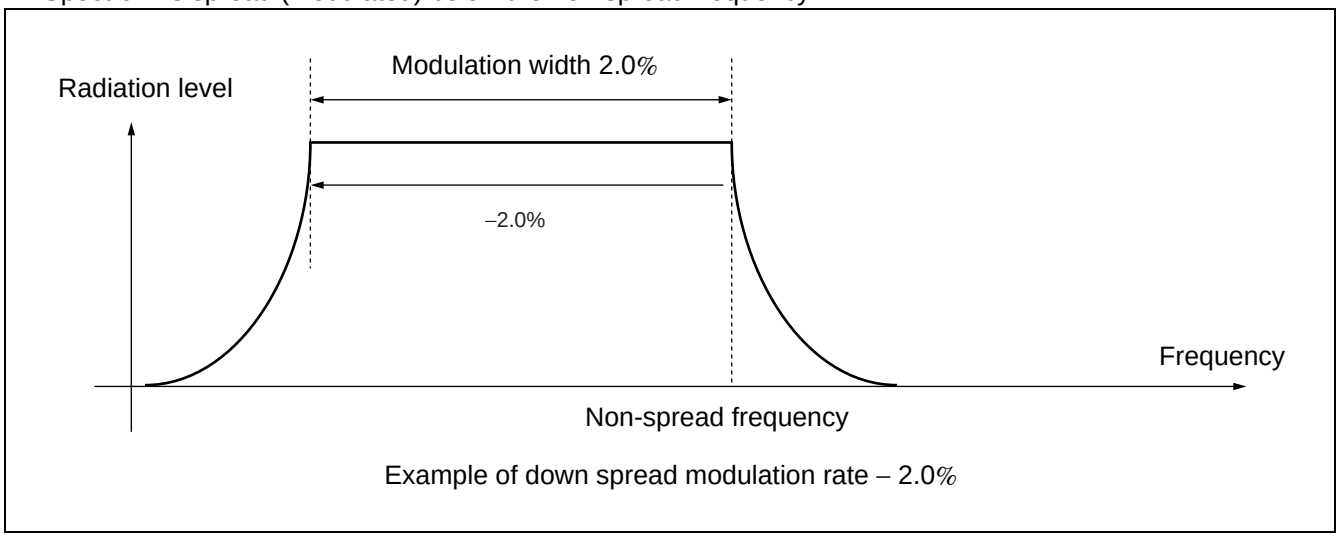
Spectrum is spread (modulated) by centering on the non-spread frequency.



Example of center spread modulation rate ± 1.0%

• Down spread

Spectrum is spread (modulated) below the non-spread frequency.



Example of down spread modulation rate – 2.0%

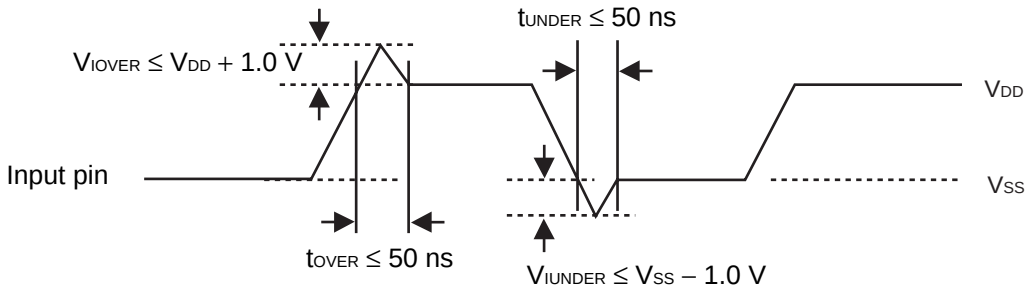
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+ 4.0	V
Input voltage*	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	– 55	+ 125	°C
Operation junction temperature	T_J	– 40	+ 125	°C
Output current	I_O	– 14	+ 14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS}–1.0 (t_{UNDER} ≤ 50 ns)	—	V

* : The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

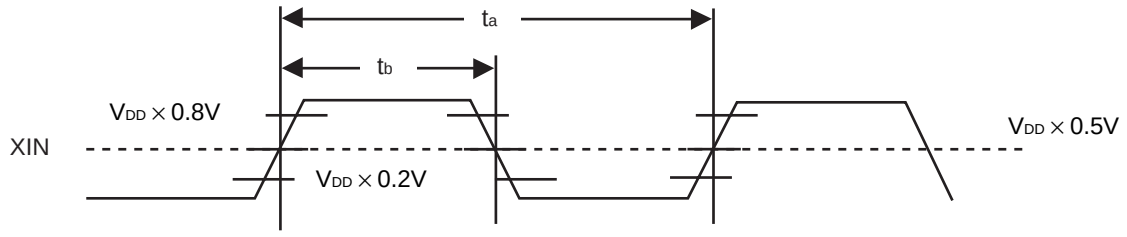
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	At MLTP = "L"	2.7	3.3	3.6	V
			At MLTP = "H"	3.0	3.3	3.6	
"H" level input voltage	V_{IH}	XIN, MLTP, OE, SPRD, S1, S0	—	$V_{DD} \times 0.80$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}		—	V_{SS}	—	$V_{DD} \times 0.20$	V
Input clock duty cycle	t_{DCI}	XIN	Input frequency 12 MHz to 42 MHz	40	50	60	%
Operating temperature	Ta	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



■ ELECTRICAL CHARACTERISTICS

- DC Characteristics

(Ta = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	V_{DD}	24 MHz output no load capacitance	—	7.0	11.0	mA
Power down current	I_{PD}	V_{DD}	At power down (At OE="L")	—	5	20	µA
Output voltage	V_{OH}	OUT	"H" level output, I_{OH}= – 8 mA	0.8 × V_{DD}	—	V_{DD}	V
	V_{OL}		"L" level output, I_{OL} = 8 mA	V_{SS}	—	0.2 × V_{DD}	V
Output impedance	Z_{OC}	OUT	MLTP = L, 12 MHz to 28 MHz output, V_{DD} = 2.7 V to 3.6 V	—	30	—	Ω
			MLTP = H, 80 MHz to 168 MHz output, V_{DD} = 3.0 V to 3.6 V	—	20	—	Ω
Load capacitance	C_L	OUT	MLTP = L, 12 MHz to 28 MHz output, V_{DD} = 2.7 V to 3.6 V	—	—	15	pF
			MLTP = H, 80 MHz to 168 MHz output, V_{DD} = 3.0 V to 3.6 V	—	—	15	pF
Built-in oscillation stabilization capacitance	C_{OSC}	XIN, XOUT	—	—	4	—	pF
Input pull-up resistance	R_{PUOEH}	OE	V_{IH} = 0.8 × V_{DD}	10	25	100	kΩ
	R_{PUOEL}	OE	V_{IL} = 0.0 V	500	800	1200	kΩ
	R_{PU}	SPRD, S1, S0	V_{IL} = 0.0 V	25	50	200	kΩ
Input pull-down resistance	R_{PD}	MLTP	V_{IH} = V_{DD}	25	50	200	kΩ

Note : When OE pin is set to "L", the pull-up resistor connected to SPRD pin, S1 pin, and S0 pin and the pull-down resistor connected to MLTP pin are disconnected, and internal signal is fixed to "L".
See "■ I/O CIRCUIT TYPE" for details.

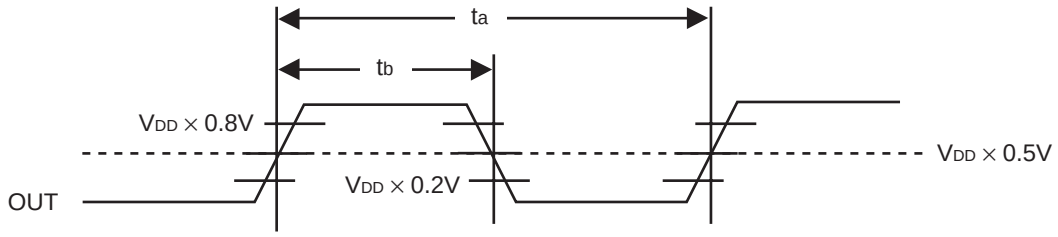
• AC Characteristics

(Ta = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0.0 V)

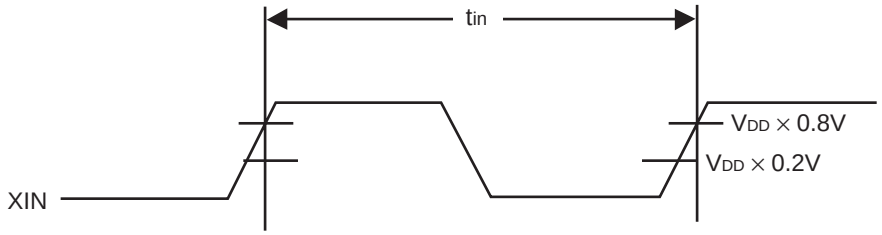
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f_{in}	XIN	MLTP= "L", V_{DD} = 2.7 V to 3.6 V, Crystal oscillation input	12	—	28	MHz
			MLTP= "H", V_{DD} = 3.0 V to 3.6 V, Crystal oscillation input	20	—	42	
Crystal oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation, MLTP= "L", V_{DD} = 2.7 V to 3.6 V	12	—	28	MHz
			Fundamental oscillation, MLTP= "H", V_{DD} = 3.0 V to 3.6 V	20	—	42	
Output frequency	f_{OUT}	OUT	MLTP= "L", V_{DD} = 2.7 V to 3.6 V	12	—	28	MHz
			MLTP= "H", V_{DD} = 3.0 V to 3.6 V	80	—	168	
Output clock rise time	tr	OUT	0.2 × V_{DD} to 0.8 × V_{DD} Load capacitance 15 pF	0.4	—	4.0	ns
Output clock fall time	tf	OUT	0.2 × V_{DD} to 0.8 × V_{DD} Load capacitance 15 pF	0.4	—	4.0	ns
Output clock duty cycle	t_{DCC}	OUT	0.5 × V_{DD}	40	—	60	%
Modulation frequency	f_{MOD}	OUT	Input frequency at 24MHz, MLTP = "L"	—	32.0	—	kHz
			Input frequency at 24MHz, MLTP = "H"	—	21.3	—	
Lock-Up time	t_{LK}	OUT	—	—	4	10	ms
Cycle-Cycle jitter	t_{JC}	OUT	Ta= + 25°C, V_{DD}=3.3V, No load capacitance, Standard deviation σ	—	—	100	ps
Output enable "L" width	t_{OELW}	OE	—	1	—	—	µs
Power supply rise time	t_{VDR}	V_{DD}	MLTP= L, 0.0 V to 2.7 V	100	—	—	µs
			MLTP= H, 0.0 V to 3.0 V	100	—	—	
Output Hi-Z start time after power down entry	t_{PEZ}	OUT	Rise time or fall time of "OE" at 5 ns	—	—	10	ns
Output Hi-Z release time after power down exit	t_{PIZ}	OUT	Rise time or fall time of "OE" at 5 ns	0	—	—	ns
Output start time after power down exit	t_{PIO}	OUT	Rise time or fall time of "OE" at 5 ns Load capacitance 15 pF	—	—	10	ns

Note : The stabilization wait time of the modulation clock is required after the power is turned on or when the clock output enable setting (OE pin), multiplication setting (MLTP pin) or modulation rate setting (S1 pin and S0 pin) is changed. The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time.

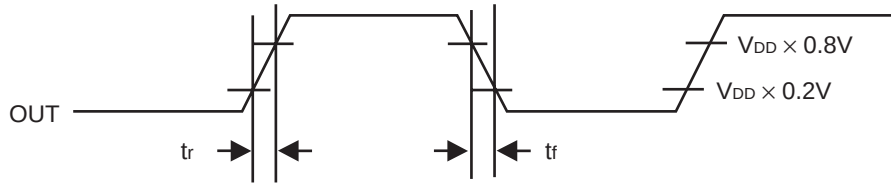
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)



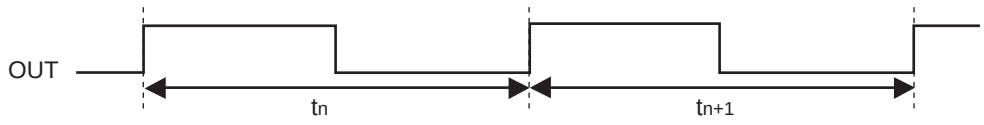
■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)



■ OUTPUT CLOCK RISE TIME/OUTPUT CLOCK FALL TIME (t_r/t_f)

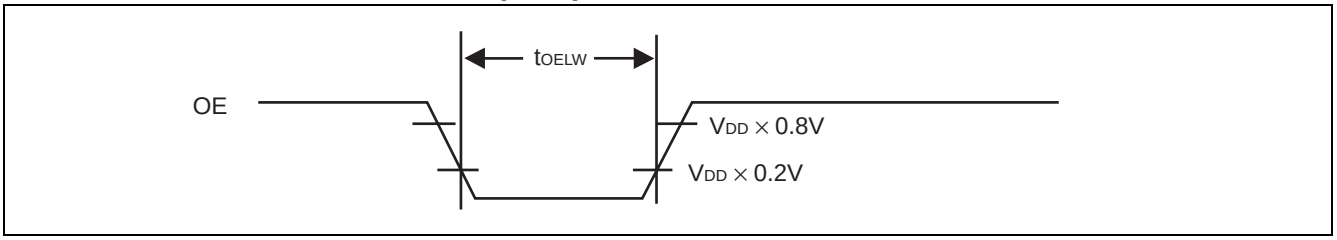


■ CYCLE-CYCLE JITTER ($t_{JC} = | t_n - t_{n+1} |$)

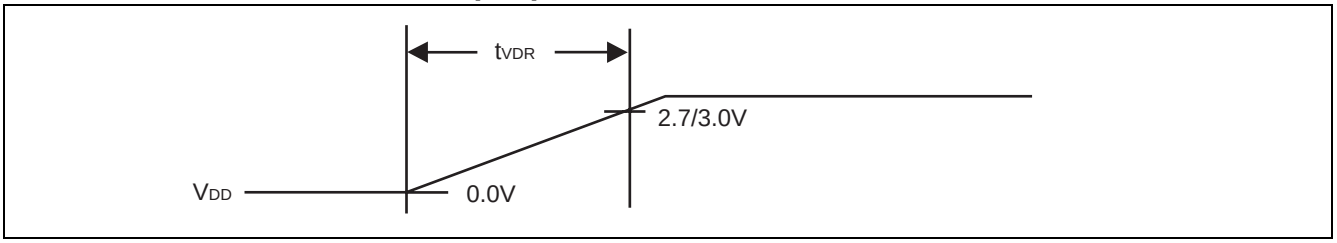


Note : Cycle-cycle jitter indicates the difference between a certain cycle and the immediately succeeding (or preceding) cycle.

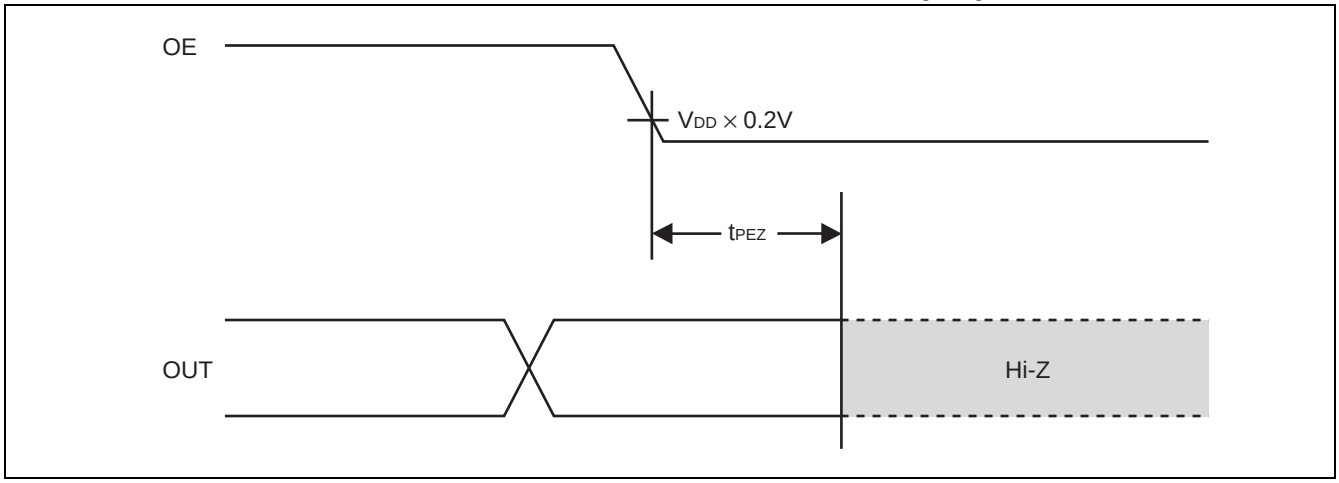
■ OUTPUT ENABLE "L" WIDTH (t_{OELW})



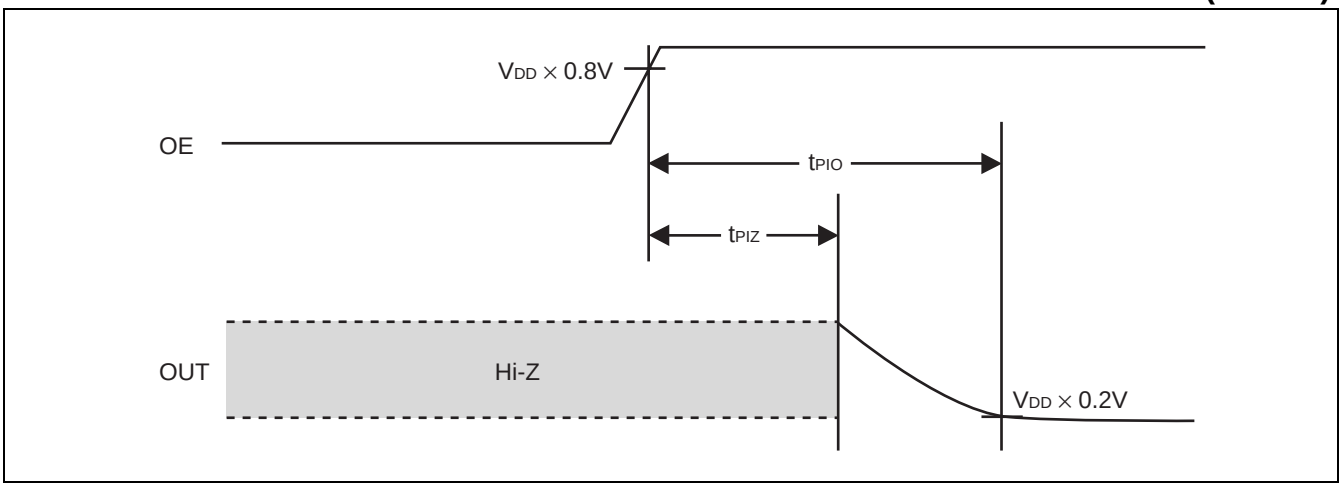
■ POWER SUPPLY RISE TIME (t_{VDR})



■ OUTPUT Hi-Z START TIME AFTER POWER DOWN ENTRY (t_{PEZ})

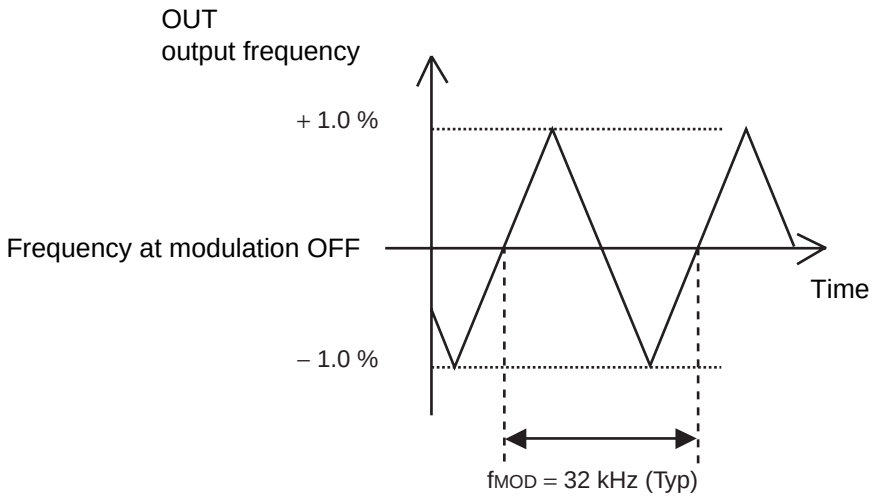


■ OUTPUT Hi-Z RELEASE TIME • OUTPUT START TIME AFTER POWER DOWN EXIT (t_{PIZ} • t_{PIO})

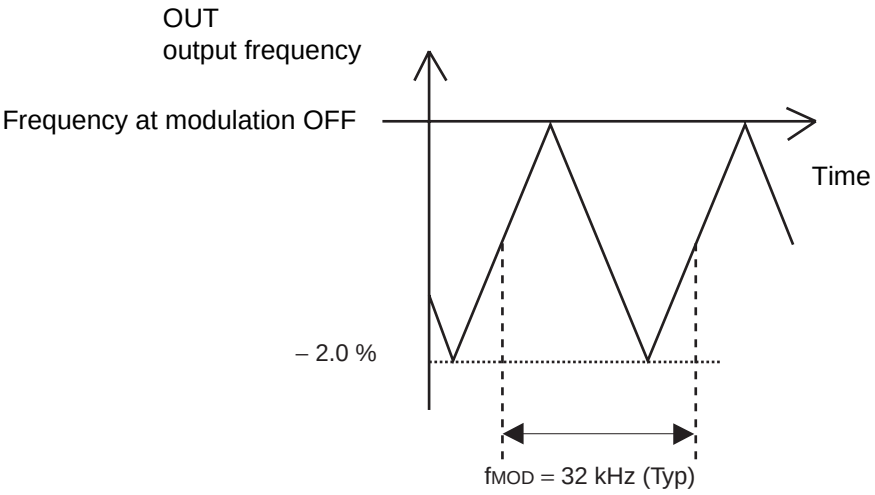


■ MODULATION WAVEFORM

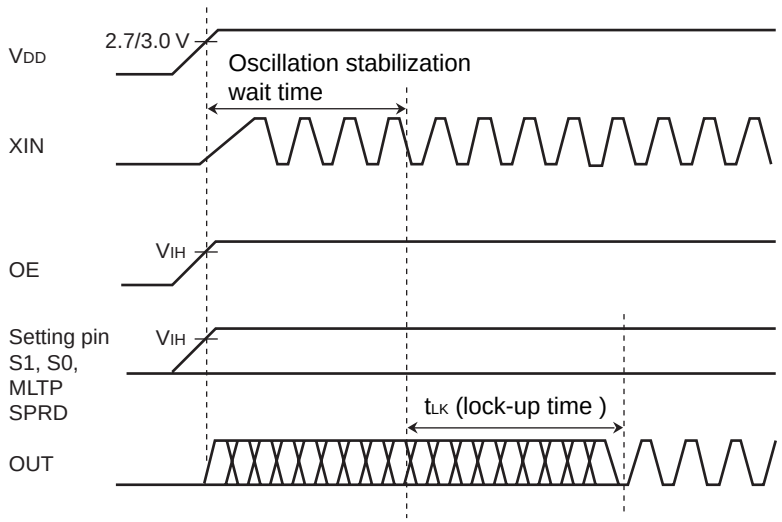
• Modulation rate ±1.0%, example of center spread



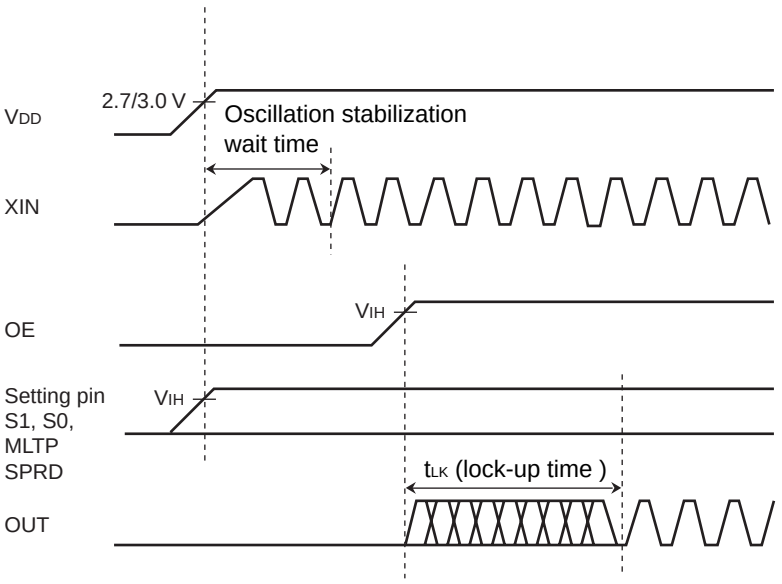
• Modulation rate –2.0%, example of down spread



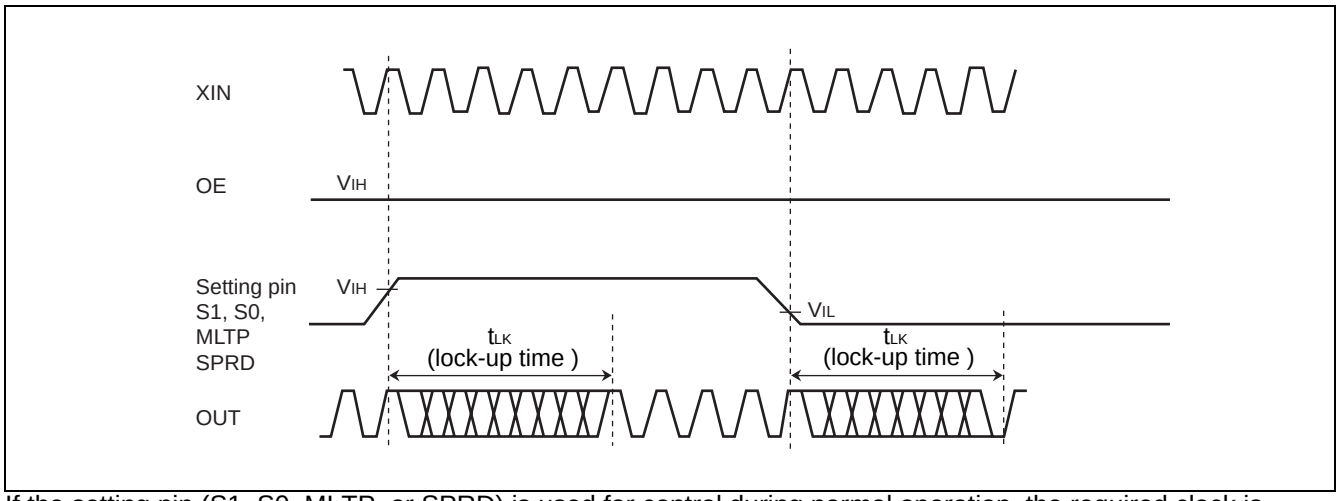
■ LOCK-UP TIME



The clock oscillation stabilization wait time is required when the power is turned on.
If the OE pin is fixed at “H” level, the maximum time after the power is turned on until the required clock is obtained is (the oscillation stabilization wait time of input clock to XIN pin) + (the lock-up time “t_{LK}”) .
For the stabilization wait time of input clock to the XIN pin, check the characteristics of the resonator or oscillator used.



If the OE pin is used for power down control, the required clock is obtained at most the lock-up time “t_{LK}” after the OE pin goes “H” level.

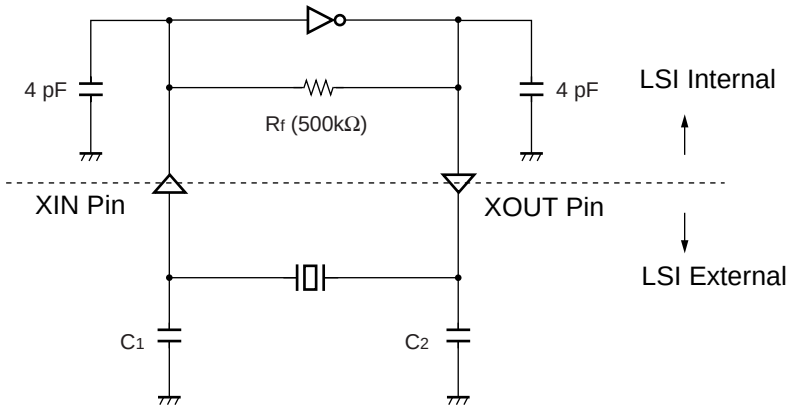


If the setting pin (S1, S0, MLTP, or SPRD) is used for control during normal operation, the required clock is obtained at most the lock-up time "t_{LK}" after the level at the pin is determined.

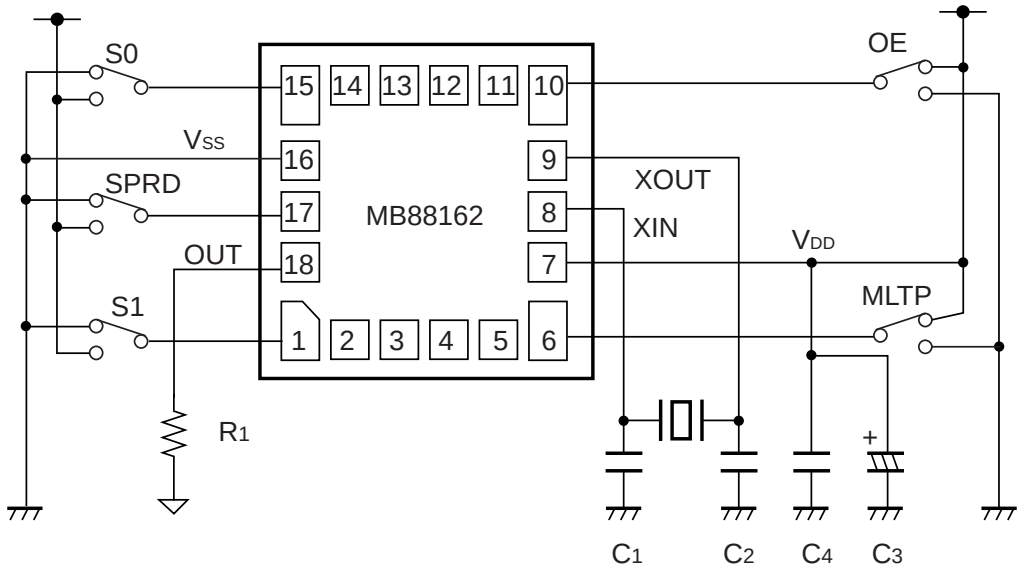
Note : The wait time for the clock signal output from the OUT pin to become stable is required after the IC is released from power-down mode by the OE pin or after another pin's setting is changed. During the period until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and Cycle-Cycle jitter characteristic cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.

■ CRYSTAL OSCILLATION CIRCUIT

The figure below shows the connection example about general crystal resonator. The oscillation circuit has the built-in feedback resistor (500kΩ) and oscillation stabilization capacitance (4 pF) . Because the value of oscillation stabilization capacitance must be adjusted to the most suitable value of the individual oscillator, add the capacitance (C1 and C2) to LSI external if necessary.



■ INTERCONNECTION CIRCUIT EXAMPLE



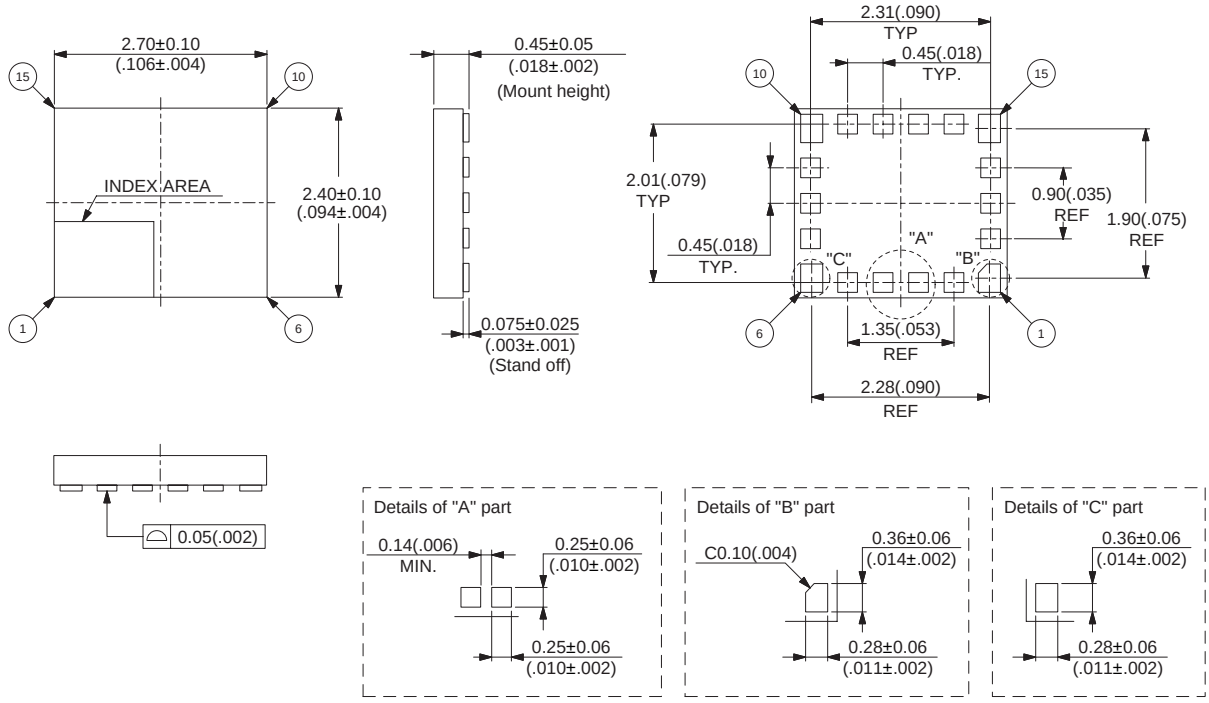
C_1, C_2	: Oscillation stabilization capacitance (see "■ CRYSTAL OSCILLATION CIRCUIT".)
C_3	: Capacitor of 10 µF or higher
C_4	: Capacitor of about 0.01 µF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
R_1	: Impedance matching resistor for board pattern

■ ORDERING INFORMATION

Part no.	Package	Emboss taping
MB88162PVB-G-EFE1	18-pin plastic BCC (LCC-18P-M05)	EF type
MB88162PVB-G-ERE1		ER type

■ PACKAGE DIMENSION

18-pin plastic BCC
(LCC-18P-M05)



Dimensions in mm (inches)
Note: The values in parentheses are reference values.

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0602