MB86S02 CIF CMOS Sensor Camera Module

1 Chip CIF CMOS Sensor & Color Processor

Description

MB86S02 is a 10K pixel (CIF size) CMOS image sensor with integrated color signal processor. Integration of CMOS image sensor and color signal processor into 1 chip enables low power consumption and small size. MB86S02 is optimized for applications such as cellular phones and PDA.

Features

Optical format	: 1/7 inch
Pixel array number	: 357 x 293
Color filter	: RGB mosaic (with micro lens)
Supply voltage	: 2.8V (single voltage)
Power consumption	: 30mW (fOSCIN=9MHz, fPCLK=4.5MHz, 15 fps)
Input Clock Frequency	: 9MHz standard
Digital Input voltage	: CMOS level
Digital output voltage	: CMOS level (D0~D7 : High impedance output available)
Video output format	: YCbCr422 / YUV422 (8bit output)
Color signal processor	: Auto gain control (AGC) Auto exposure control (AE) Auto white balance (AWB) Gamma correction Aperture correction
Additional function	: CIF (352 x 288) / QCIF (176 x 144) Switch function CCIR656 standard header output (Only with CIF function) Anti-flicker function (50Hz / 60Hz) Power save mode Scanning direction variation Stand-by function(22uW)
Serial Interface	: I2C serial Interface
Camera Module	: 21 pin flexible cable (7.80mm x 6.98mm x 4.31mm)
Applications	: Cellular phones, PDA camera

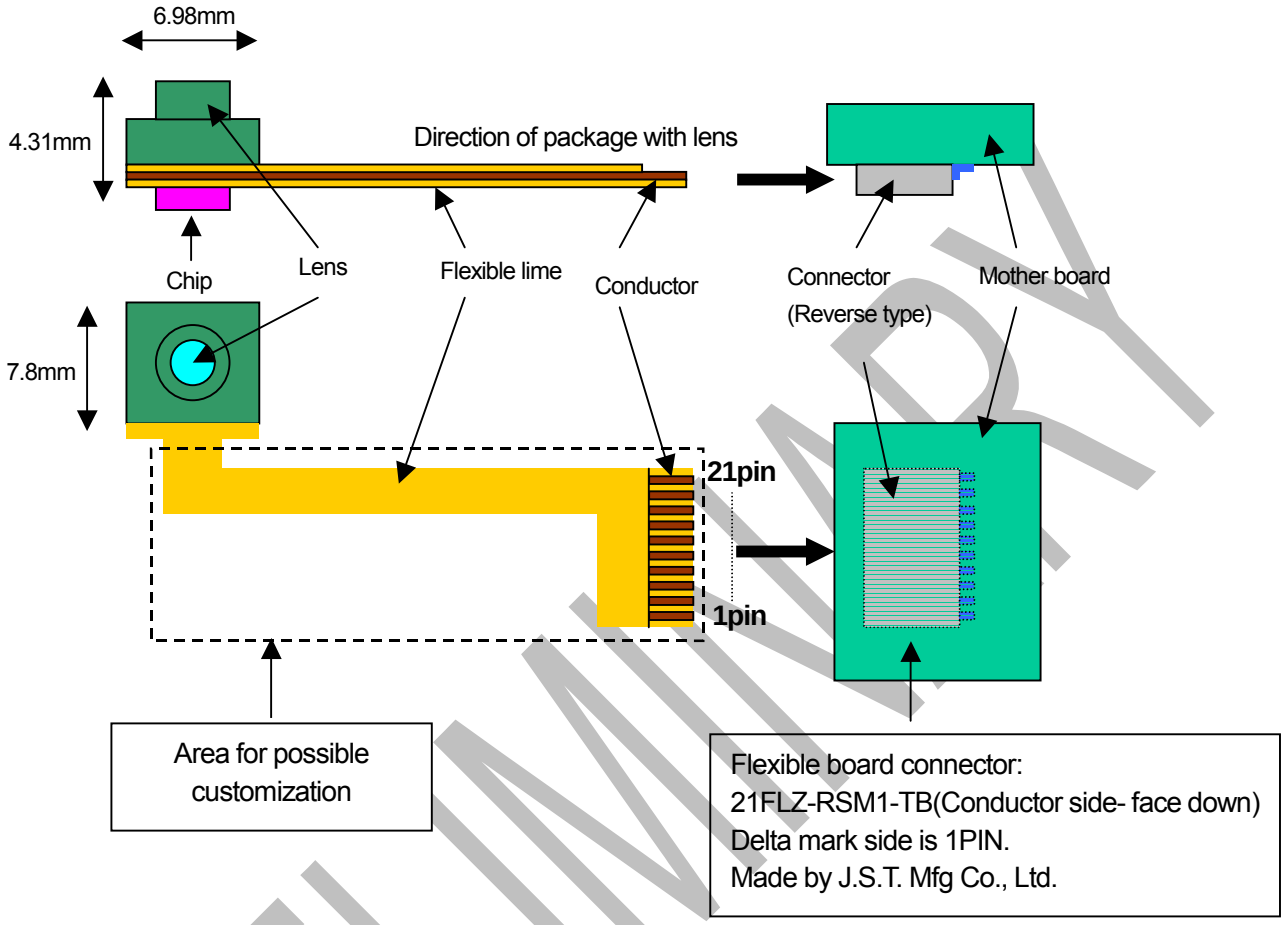
Optical Specifications

Total array size	373(H) x 301(V)
Effective pixel size	357(H) x 293(V)
Pixel area	1.96mm x 1.61mm (Diagonal length: 2.54mm)
Pixel size	5.5 um x 5.5 um
Sensitivity	60mV/lx @66ms (15 fps), 5100K, F number 2.6with micro lens
Saturation voltage	600mV
SN ratio	45dB

Lens Specifications

Optical size	1/7 inch
Lens composition	1 piece (Plastic non-spherical surface)
F number	2.6
Focal length	2.0mm
Focus range	5cm~10m
View angle (Horizontal)	60 degree
Peripheral light ratio	About 60% (at corner edge)
TV distortion	About 3.5%
MTF (center)	More than 100lp/mm (on axis)
MTF (peripheral)	85lp/mm (60%)

Flexible pin positions



Regarding Customization of module

Above broken line area can be customized. Length and size of flexible cable can be customized. Maximum I/O pin number is 21.
Please ask our sales people for further details.

Flexible board I/O pins

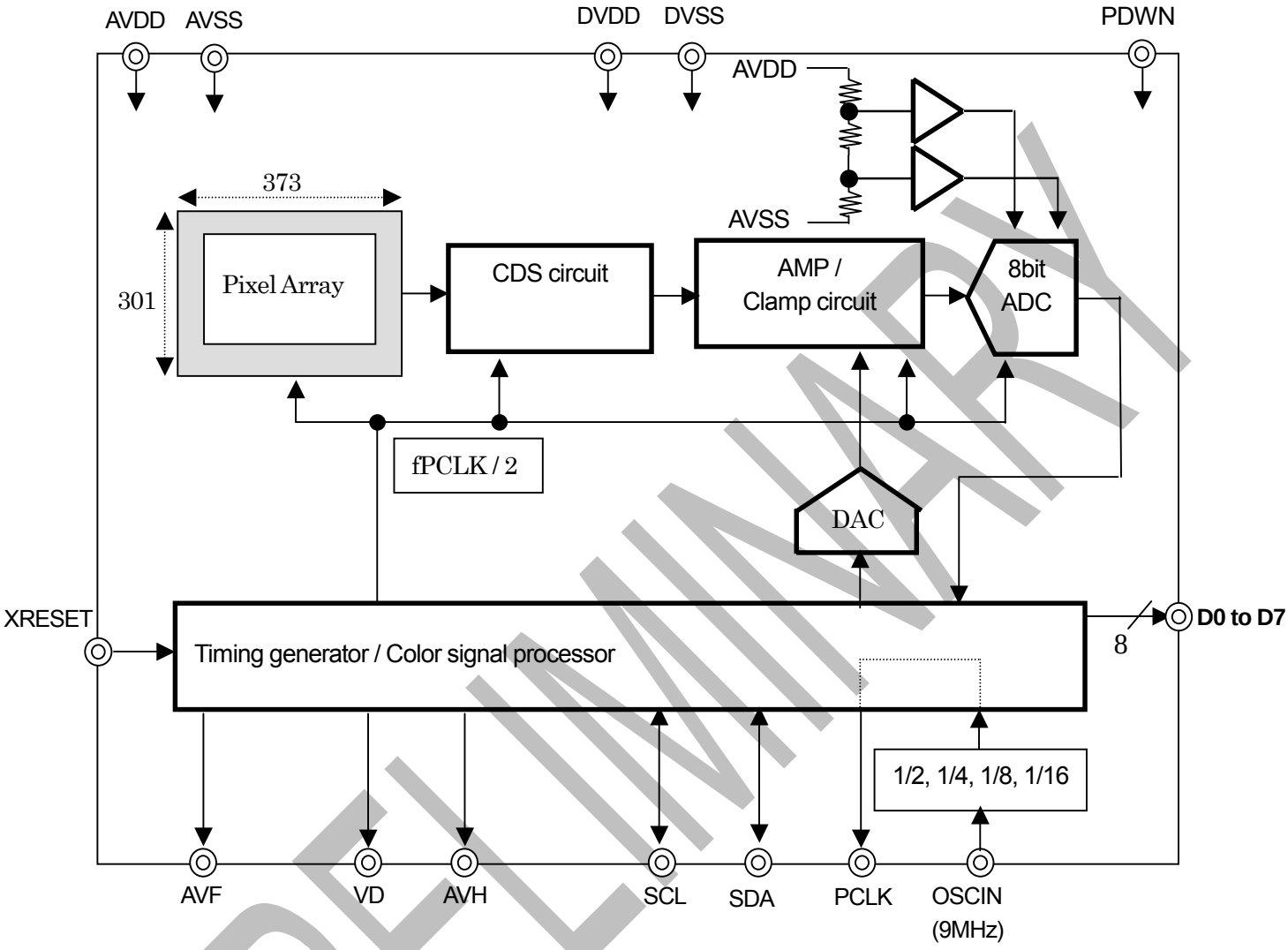
Pin Name	I/O	Pin Number	Description
OSCIN	I	1	Clock input pin (9MHz)
XRESET	I	2	Device reset signal input pin ”L” input : Device reset status (Change to default setting) ”H” input : Operation status
PDWN	I	3	Power down signal input pin ”L” input : Operation status ”H” input : Power down status (Stand-by) *Hold status before power down)
D0 (LSB)	O	4	Digital video output pin Video output format : YCbCr422 / YUV422 (8bit output)
D1	O	5	
D2	O	6	
D3	O	7	
D4	O	8	
D5	O	9	
D6	O	10	
D7 (MSB)	O	11	
PCLK	O	12	Clock output pin
DVSS	-	13	Digital ground pin
DVDD	-	14	Digital power supply pin (2.8V)
SCL	I/O	15	I2C CLK I/O pin
SDA	I/O	16	I2C DATA I/O pin
AVF	O	17	Active video frame (Effective frame vertical synchronization output)
AVH	O	18	Horizontal effective pixel synchronization output pin
VD	O	19	Vertical synchronization signal output pin
AVSS	-	20	Analog ground pin
AVDD	-	21	Analog power supply pin (2.8V)

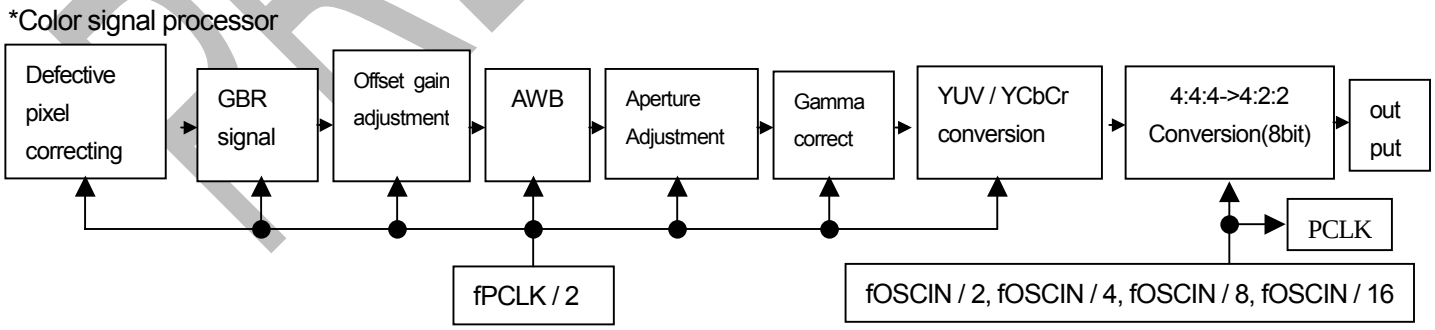
Note:

*Please bypass AVDD and DVDD pins to GND (VSS) with a condenser for high frequency (>1uF).
Please attach a condenser for high frequency as near as possible to pins.

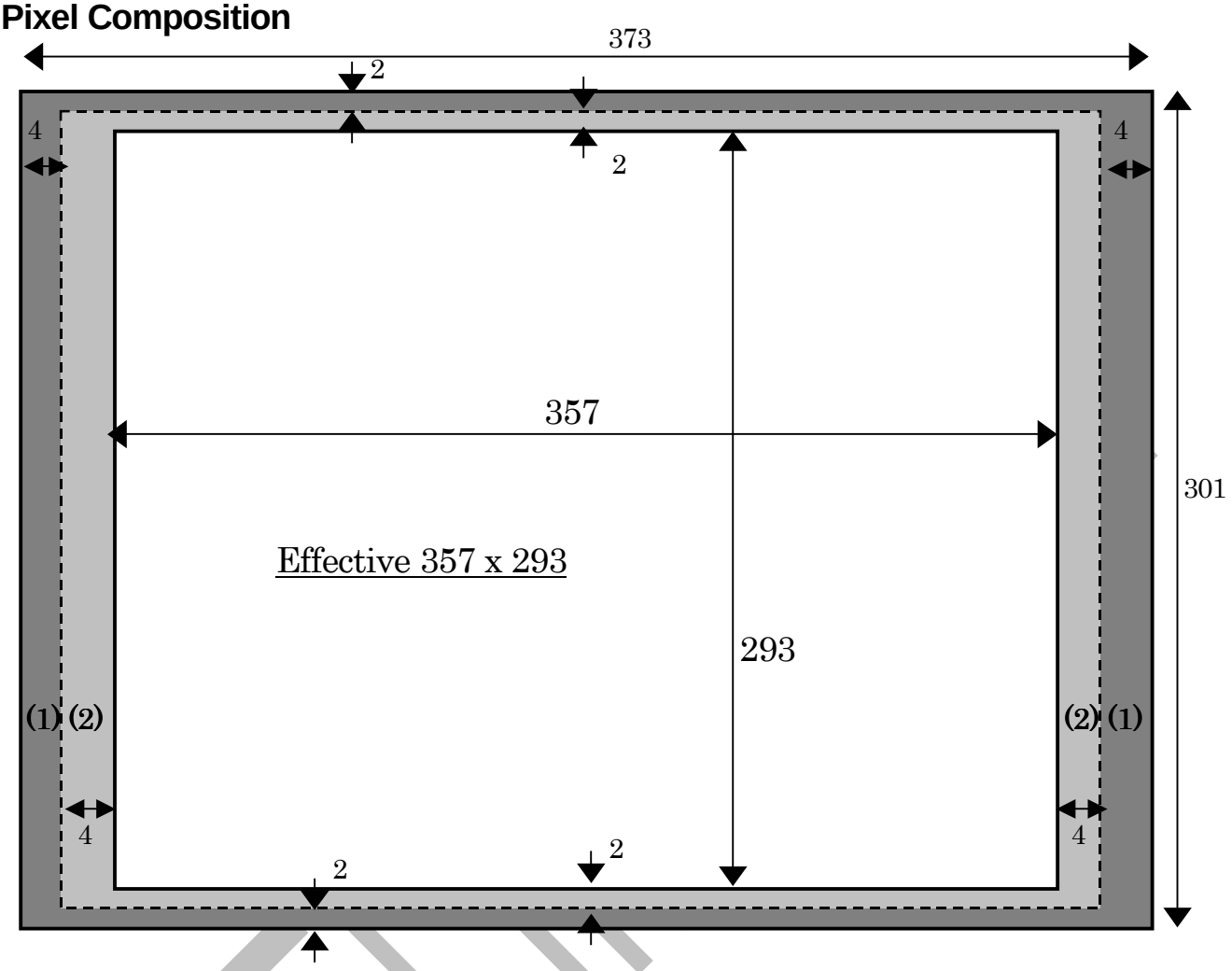
*I2C access is slave operation only. Slave address is fixed at C2h(Write) and C3h(Read).

Block Diagram





Pixel Composition



(1) Shading pixel portion 1
(2) Shading pixel portion 2 (for TEST)

Color Filter Composition

	1	2	3	4	---	354	355	356	357
293	R	G	R	G	---	G	R	G	R
292	G	B	G	B	---	B	G	B	G
291	R	G	R	G	---	G	R	G	R
290	G	B	G	B	---	B	G	B	G
---	---	---	---	---	---	---	---	---	---
4	G	B	G	B	---	B	G	B	G
3	R	G	R	G	---	G	R	G	R
2	G	B	G	B	---	B	G	B	G
1	R	G	R	G	---	G	R	G	R

Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	AVDD, DVDD	-0.3	4.0	V
Input and output voltage	D0 to D7, OSCIN, PCLK, VD, XRESET, PDWN, AVH, AVF, SDA, SCL	-0.3	DVDD+0.3 *1	V
Storage temperature	Tstg	-35	85	C

*1: Not to exceed +4.0V

WARNING : Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Condition

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage		AVDD, DVDD	2.6	2.8	3.0	V
Difference between analog voltage and digital voltage		dVDD	-	0	0.3	V
Clock frequency		fOSCIN	-	9	20	MHz
Digital 'H' input voltage	OSCIN, XRESET, PDWN	VIHD	DVDD-0.5	DVDD	-	V
Digital 'L' input voltage		VILD	-	0	0.5	V
I2C ”H” input voltage	SDA, SCL	VIHI2C	0.7DVDD	-	-	V
I2C ”L” input voltage		VILI2C	-	-	0.3DVDD	V
Operating temperature*		Ta	-25	-	65	C
I2C clock frequency		fSCL	-	-	100	kHz

*:There must not be dewy.

ELECTRICAL CHARACTERISTIC

DC Electrical Characteristic

(AVDD=DVDD=2.8V, Ta=25C)

Parameter			Symbol	Value			Unit
				Min.	Typ.	Max.	
Analog power supply current	Condition: fOSCIN=9MHz, fPCLK=4.5MHz, 15fps		AIDD		7		mA
Digital power supply current			DIDD		3.5		mA
Digital "H" output voltage (IOH=-0.4mA)	D0 to D7, PCLK, VD, AVH, AVF		VOHD	DVDD-0.4	-	-	V
Digital "L" output voltage (IOL=1mA)			VOLD	-	-	0.4	V
Digital input current			IID	-20	-	5	uA
I2C ”H” output voltage(DVDD pull up resistance10kohm)		SDA, SCL	VOHI2C	DVDD-0.4	-	-	V
I2C ”L” output voltage			VOLI2C	-	-	0.4	V
Standby current			Istb	-	8	-	uA

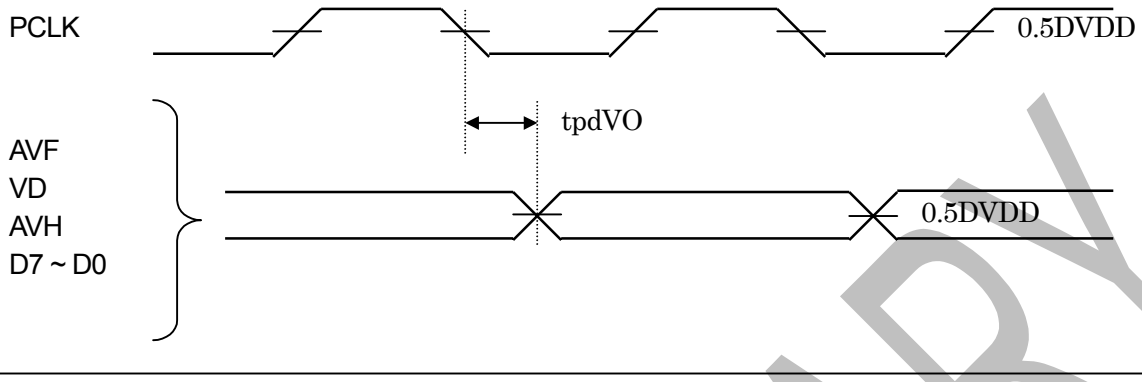
AC Electrical Characteristic

(AVDD=DVDD=2.8V, Ta=25C)

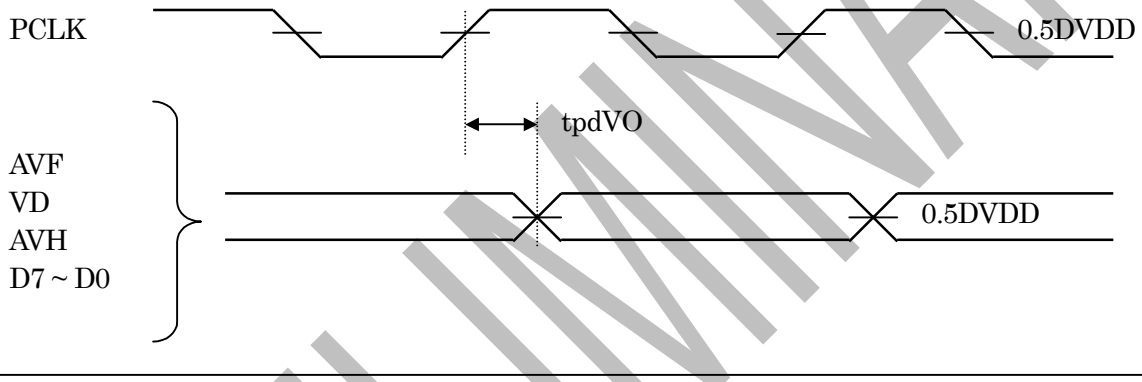
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Clock frequency	System clock 1/2	fPCLK	-	fOSCIN / 2	-	Hz
	System clock 1/4		-	fOSCIN / 4	-	Hz
	System clock 1/8		-	fOSCIN / 8	-	Hz
	System clock 1/16		-	fOSCIN / 16	-	Hz
PCLK - Data out delay		tpd		2		ns

Timing Diagram

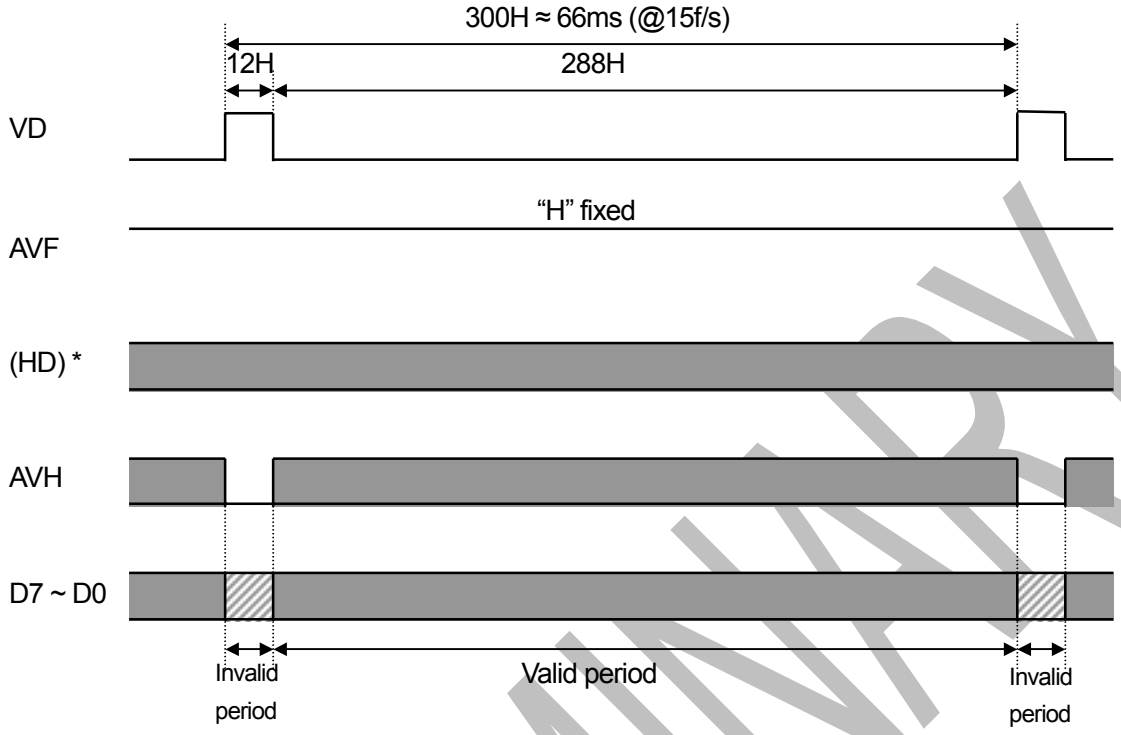
PCLK : Positive (default setting)



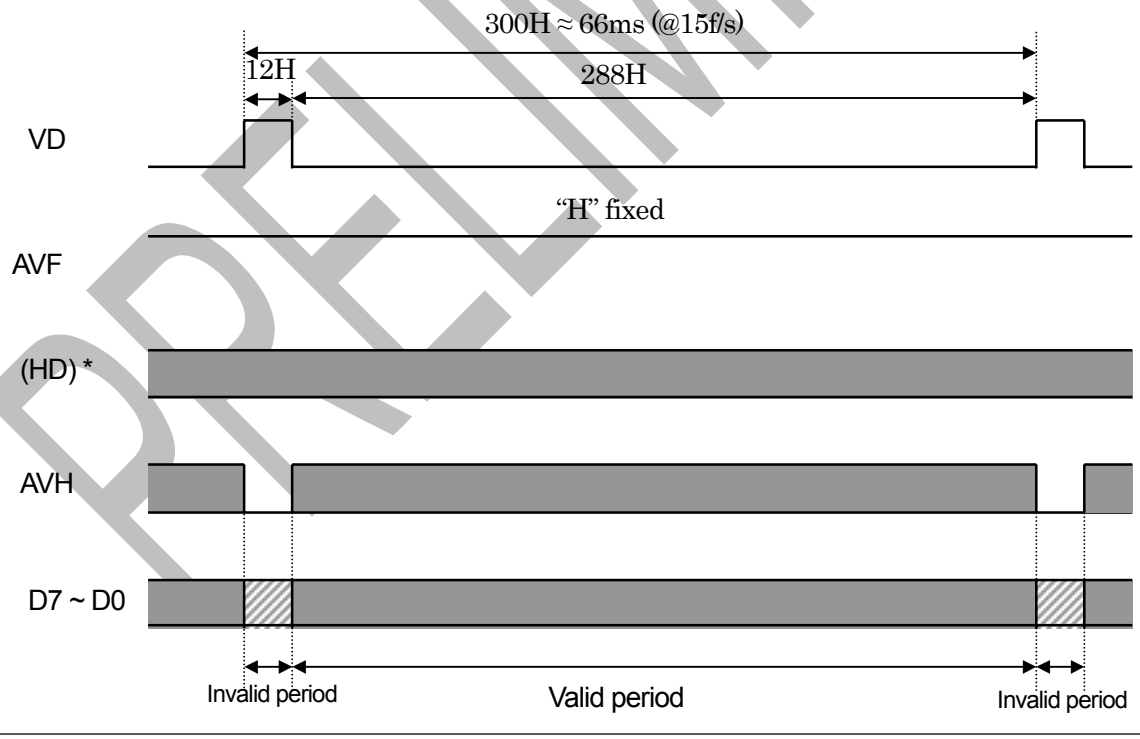
PCLK : Negative



Vertical Timing (default, fOSCIN = 9MHz, fPCLK = 4.5MHz, frame rate = 15f/s)

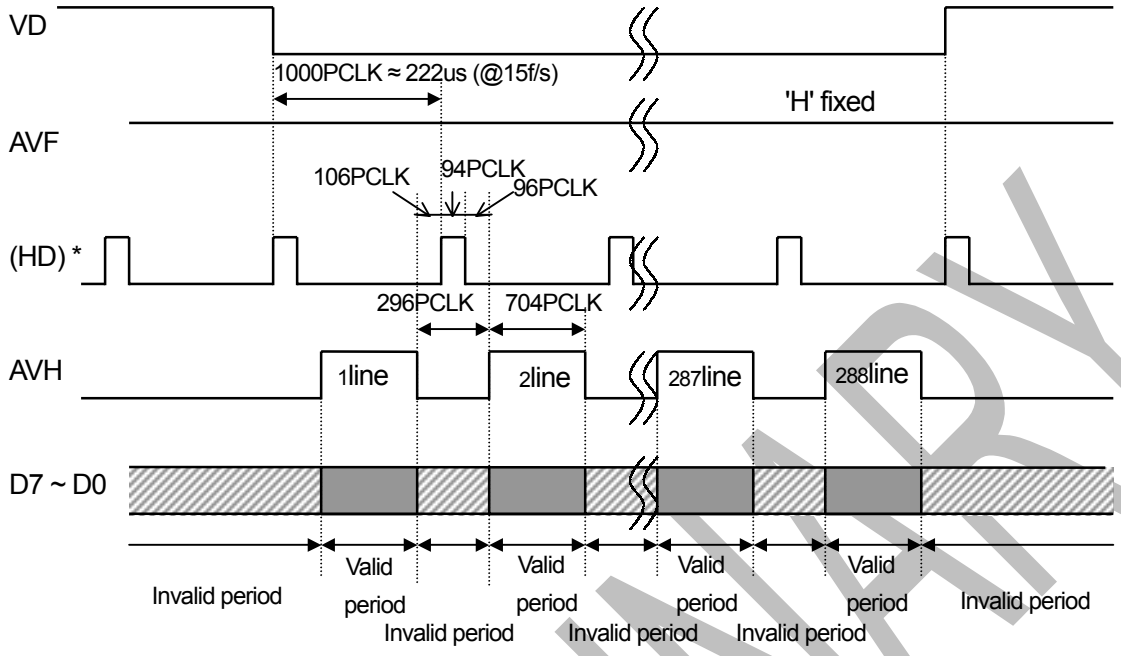


Vertical Timing (QCIF function, OSCIN = 9MHz, fPCLK = 2.25MHz, frame rate = 15f/s)

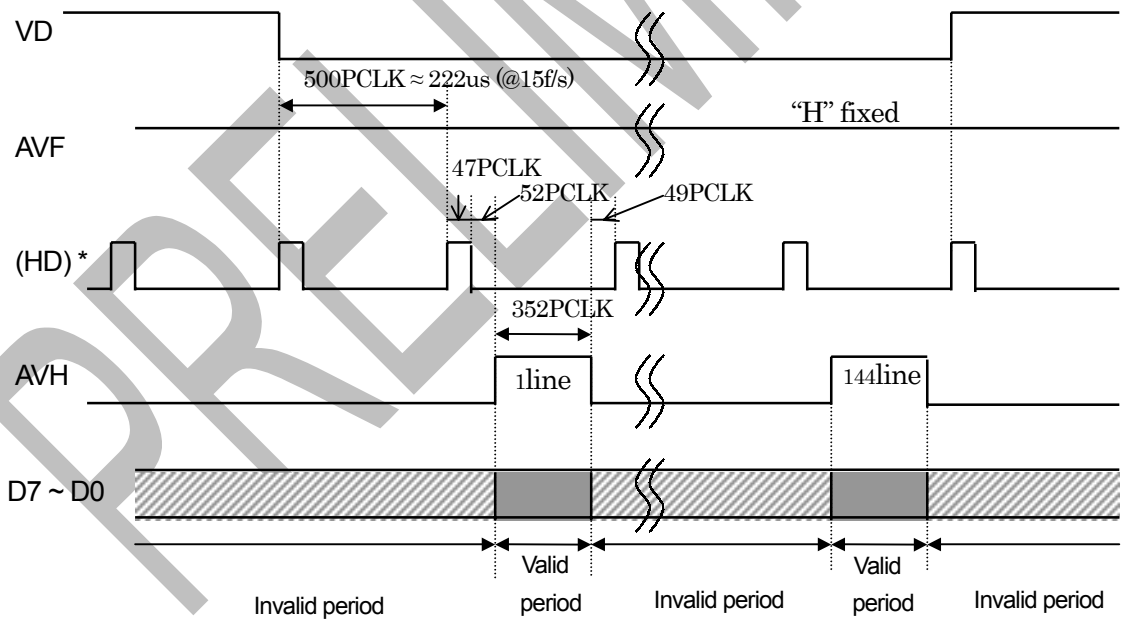


(HD) * : No output of camera module

Horizontal Timing (default, fOSCIN = 9MHz, fPCLK = 4.5MHz, frame rate = 15f/s)

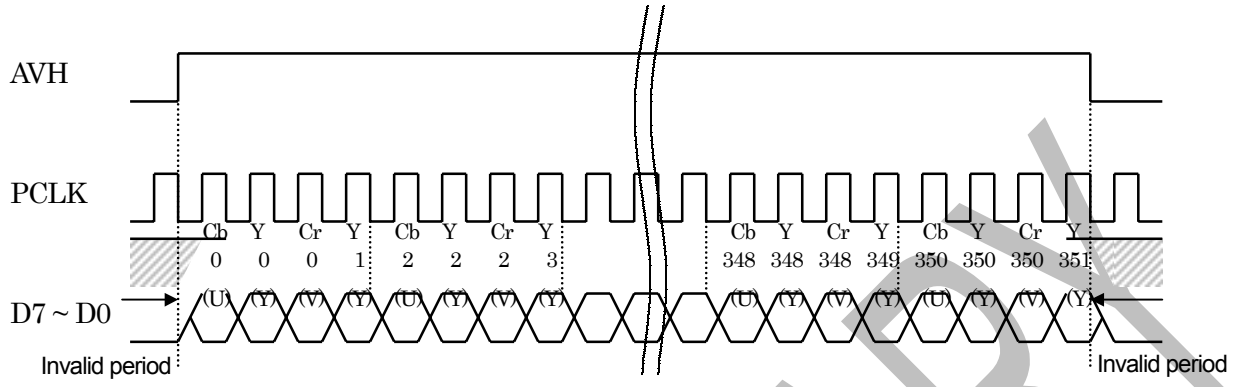


Horizontal Timing (QCIF function, OSCIN = 9MHz, fPCLK = 2.25MHz, frame rate = 15f/s)

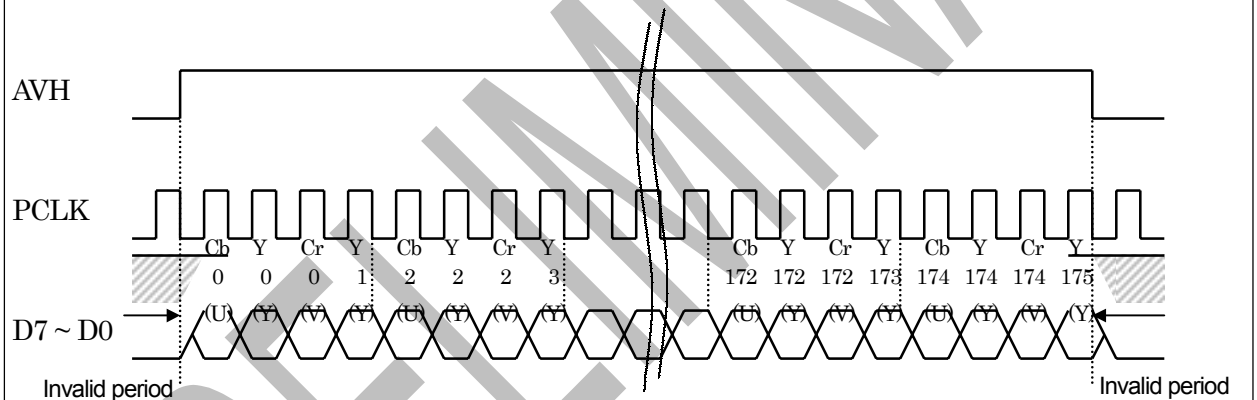


(HD) * : No output of camera module

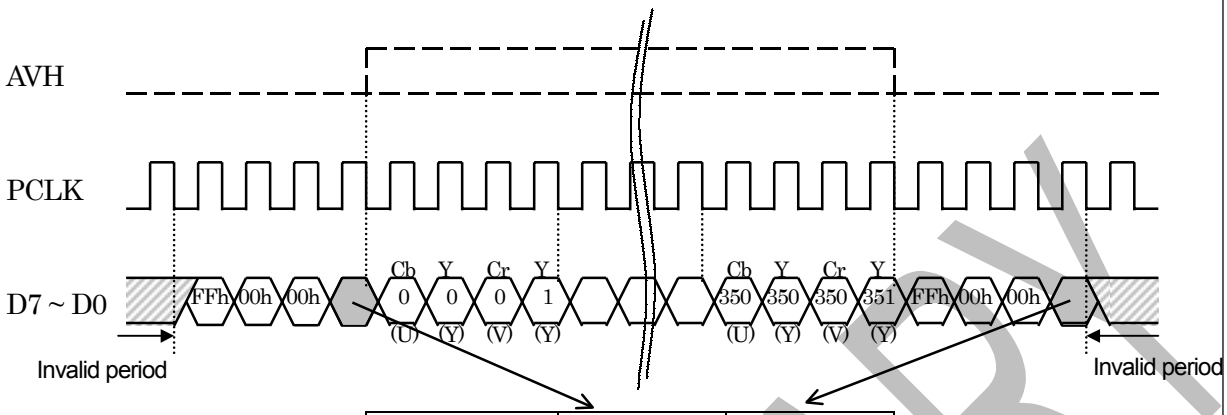
Digital Video output timing (Default setting : CIF, fOSCIN = 9MHz, fPCLK = 4.5MHz, frame rate = 15f/s)



Digital Video output timing (QCIF, fOSCIN = 9MHz, fPCLK = 2.25MHz, frame rate = 15f/s)

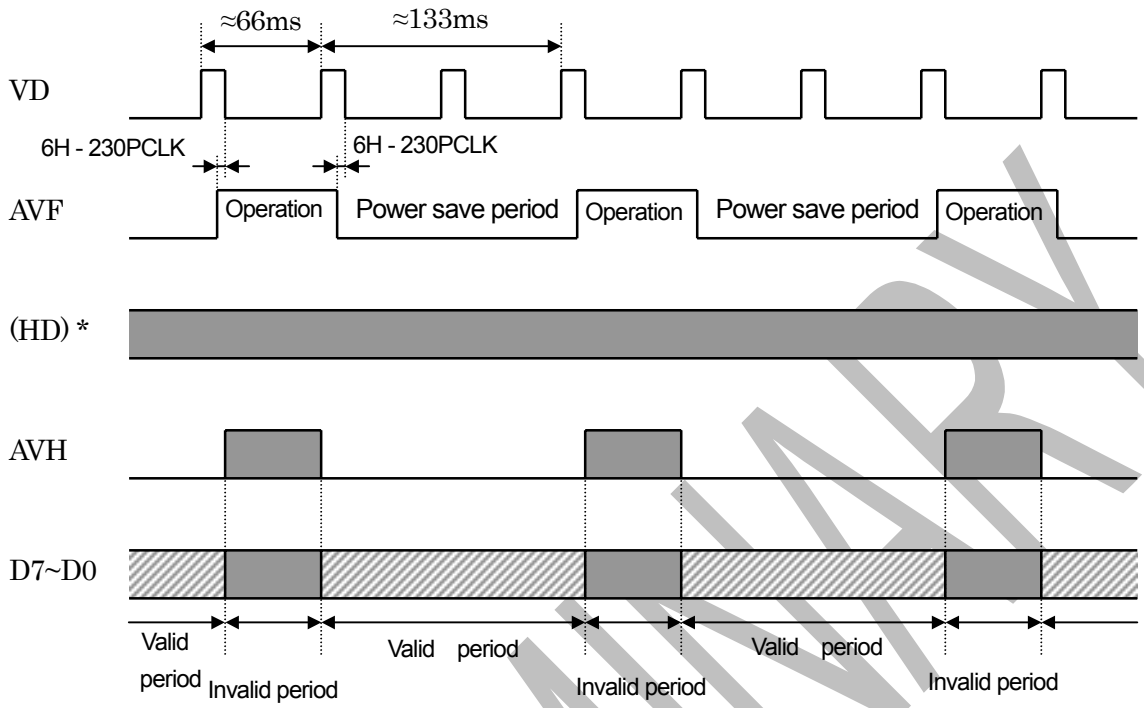


Digital Video output timing (SAV/EAV mode)
(Default setting, fOSCIN = 9MHz, fPCLK = 4.5MHz, frame rate = 15f/s)



	SAV	EAV
Active	80h	9Dh
V blank	ABh	B6h

Power save mode (fOSCIN = 9MHz, fPCLK = 4.5MHz, frame rate = 5f/s)



(HD)* No output of camera module

Power consumption at power save mode and stand-by function.

	15fps	5fps(at power save mode)	Stand-by function
Power consumption	30mW	15mW	22uW

Resister Setting

Group	Address	Name	Bit	Data	Default	R/W	Description
CTRL	00	VER	07-00		-	R	Version information
	01	IDR	07	0 : ROM Read fail data 1 : ROM Read success	-	R	EEPROM data loading status
			06-03	Unused	-	-	Unused
			02-01	00 : 1/2dividing frequency (fPCLK = fOSCIN/2) 01 : 1/4dividing frequency (fPCLK = fOSCIN/4) 10 : 1/8dividing frequency (fPCLK = fOSCIN/8) 11 : 1/16dividing frequency (fPCLK = fOSCIN/16)	00	R/W	Clock divider
			00	0 : Operation usually 1 : Timing reset on	0	W	Timing reset
	02	MD1	07	0 : with SAV/EAV, 1 : no header	0	R/W	CCIR656 Header
			06	0 : Gamma correction ON, 1 : OFF	0	R/W	Gamma correction (Range : 23-29)
			05	0 :Aperture correction ON ,1 : OFF	0	R/W	Aperture correction (Range : 20-22)
			04	0 : color, 1 :G=B=R	0	R/W	Mosaic into GBR
			03	0 : Filter ON, 1 : OFF	1	R/W	Defective pixel correcting filter
			02	0 : CIF, 1 : QCIF	0	R/W	CIF/QCIF Function select
			01	0 : Normal, 1 : Upper side down	0	R/W	Vertical scanning direction
			00	0 : Normal, 1 : Mirror	0	R/W	Horizontal scanning direction
	03	MD2	07-06	00 : Auto, 01 : Auto 10 : Fixed line, 11 : Manual	00	R/W	AGC mode (Range 32-40)
			05-04	00 : Auto , 01 : Fixed1 10 : Fixed, 11 : Fixed 3	00	R/W	White balance coefficient (Range 44-54)
			03	0 : AWB on, 1 : AWB off	0	R/W	Auto white balance
			02	0 : Offset binary 1 : Straight binary	0	R/W	YUV/YCbCr Output binary
			01	0 : UV/CbCr Out ahead 1 : Y Out ahead	0	R/W	Video out put
			00	0 : YCbCr, 1 : YUV	0	R/W	Video output format
	04	POLR	07	0 : Active "H", 1 : Active "L"	0	R/W	AVF Polarity
			06	0 : Active "H", 1 : Active "L"	0	R/W	AVH Polarity
			05	0 : Active "H", 1 : Active "L"	0	R/W	HD Polarity (Camera module internal signal)
			04	0 : Active "H", 1 : Active "L"	0	R/W	VD Polarity
			03	0 : Positive , 1 : Negative	0	R/W	PCLK Polarity
			02	0 : Positive, 1 : Negative	0	R/W	D0-D7 Polarity
			01	Unused	-	-	Unused
			00	0 : D0-D7Output usually 1 : D0-D7Output high impedance	0	R/W	D0-D7Output high impedance
RSV	05	RSV05	07-00	Unused	-	-	Unused

Group	Address	Name	Bit	Data	Default	R/W	Description
TMG	06	T_HSTT	07-00	Range : 0 to 255(d) 0(d) : 0CLK, 14(d) : 14CLK	14(d)	R/W	Horizontal start position of AVH CIF:14CLK, QCIF:18CLK (recommended)
	07	T_HWID	07-00	Range : 0 to 255(d) 0(d) : 0pixel, 176(d) : 352pixel	176(d)	R/W	Width of AVH (Width of AVH = Set value * 2)
	08	T_VSTT	07-00	Range : 0 to 255(d) 0(d) : 0line, 8(d) : 8line	8(d)	R/W	Vertical start position of AVH
	09	T_VWID	07-00	Range : 0 to 255(d) 0(d) : 128line, 160(d) : 288line	160(d)	R/W	Effective line of AVH (AVH output line number = Set value + 128)
LUT	0A	L_I1G	07-00	Range : 0 to 255(d)	16(d)	R/W	G Black level (Green)
	0B	L_I1B	07-00		16(d)	R/W	B Black level (Blue)
	0C	L_I1R	07-00		16(d)	R/W	R Black level (Red)
	0D	L_G1G	07-00	Range : -128 to 127(d) -128(d) : (-128 + 128) / 128 = 0 0(d) : (0 + 128) / 128 = 1 127(d) : (127 + 128) / 128 ≈ 2	9(d)	R/W	Low level gain set(Green)
	0E	L_G1B	07-00		98(d)	R/W	Low level gain set (Blue)
	0F	L_G1R	07-00		49(d)	R/W	Low level gain set (Red)
	10	L_I2G	07-00	Range : 0 to 255(d)	128(d)	R/W	High level threshold code setting (Green)
	11	L_I2B	07-00		128(d)	R/W	High level threshold code setting (Blue)
	12	L_I2R	07-00		128(d)	R/W	High level threshold code setting (Red)
	13	L_G2G	07-00	Range : -128 to 127(d) -128(d) : (-128 + 128) / 128 = 0 0(d) : (0 + 128) / 128 = 1 127(d) : (127 + 128) / 128 ≈ 2	9(d)	R/W	High level gain set (Green)
	14	L_G2B	07-00		98(d)	R/W	High level gain set (Blue)
	15	L_G2R	07-00		49(d)	R/W	High level gain set (Red)
COL	16	C_GG	07-00	Range : -128 to 127(d)	19(d)	R/W	Matrix elements of color Correction GO=GI+(GI*C_GG)+(BI*C_GB)+(RI*C_GR) BO=BI+(GI*C_BG)+(BI*C_BB)+(RI*C_BR) RO=RI+(GI*C_RG)+(RI*C_RB)+(RI*C_RR)
	17	C_GB	07-00		-7(d)	R/W	
	18	C_GR	07-00		-12(d)	R/W	
	19	C_BG	07-00		-35(d)	R/W	
	1A	C_BB	07-00		36(d)	R/W	
	1B	C_BR	07-00		-1(d)	R/W	
	1C	C_RG	07-00		-11(d)	R/W	
	1D	C_RB	07-00		5(d)	R/W	
	1E	C_RR	07-00		6(d)	R/W	
RSV	1F	RSV1F	07-00	Unused	-	-	Unused
APR	20	A_KG	07-00	Range : -128 to 127(d) -128(d) : Soft (-128/64) 0(d) : No correction (0/64) 127(d) : Sharp (127/64)	32(d)	R/W	Outline emphasis (Green)
	21	A_KB	07-00		32(d)	R/W	Outline emphasis (Blue)
	22	A_KR	07-00		32(d)	R/W	Outline emphasis (Red)

Group	Address	Name	Bit	Data	Default	R/W	Description
GMM	23	G_I2	07-00	Range : 0 to 255(d)	4(d)	R/W	Range of the Middle level min set (I2)
	24	G_I3	07-00		150(d)	R/W	Range of the Middle level max set (I3), I2<I3
	25	G_G1	07-00	Range : 0 to 255(d) 0(d) : g1 = 0/16 16(d) : g1 = 16/16 255(d) : g1 = 255/16	16(d)	R/W	Low-level gain (g1)
	26	G_C2	07-01	Unused	-	-	Unused
			00	0:gamma = 0.45, 1:gamma = 1.0	0(d)	R/W	Gamma coefficient (select 0.45 or 1)
	27	G_G2	07-00	Range : 0 to 255(d) 0(d) : g2 = 1 + 0/256 92(d) : g2 = 1 + 92/256 255(d) : g2 = 1 + 255/256	92(d)	R/W	The middle level gain setting (g2)
	28	G_G3	07-00	Range : -128 to 127(d) -128(d) : g3 = 1 + (-128/128) 0(d) : g3 = 1 + (0/128) 127(d) : g3 = 1 + (127/128)	-96(d)	R/W	The high-level gain (g3)
	29	G_OFF2	07-00	Range : -128 to 127(d)	44(d)	R/W	The middle level offset (of2)
YUV	2A	Y_GU	07-00	Range : 0 to 255(d) 0(d) : 0/256 126(d) : 126/256 255(d) : 255/256	126(d)	R/W	Gain of chrominance(U)
	2B	Y_GV	07-00	Range : 0 to 255(d) 0(d) : 0/256 225(d) : 225/256 255(d) : 255/256	225(d)	R/W	Gain of chrominance(V)
	2C	Y_LIM_YL	07-00	Range : 0 to 255(d)	0(d)	R/W	Y value low-level limit
	2D	Y_LIM_YH	07-00		255(d)	R/W	Y value high-level limit
	2E	Y_LIM_UL	07-00		0(d)	R/W	U value low-level limit
	2F	Y_LIM_UH	07-00		255(d)	R/W	U value high-level limit
	30	Y_LIM_VL	07-00		0(d)	R/W	V value low-level limit
	31	Y_LIM_VH	07-00		255(d)	R/W	V value high-level limit

Group	Address	Name	Bit	Data	Default	R/W	Description
AGC	32	A_HSTT	07-00	Range : 0 to 255(d) 29(d) : 58pixel	29(d)	R/W	Horizontal start position of the AGC active window (Start pixel = set vale * 2)
	33	A_VSTT	07	Unused	-	-	Unused
			06-00	Range : 0 to 95(d) 27(d) : 54pixel	27(d)	R/W	Vertical start position of the AGC active window (Start line = Set vale * 2)
	34	A_WID	07-04	0000 : none, 0110 : 32line 0111 : 48line, 1000 : 64line 1001 : 96line, 1010 : 128line 1011 : 192line, 1100 : 256line	1011	R/W	Vertical width of the AGC active window
			03-00	0000 : none, 0110 : 32pix 0111 : 48pix, 1000 : 64pix 1001 : 96pix, 1010 : 128pix 1011 : 192pix, 1100 : 256pix	1100	R/W	Horizontal width of the AGC active window
	35	A_INTVL	07-00	Range : 0 to 255(d) 0(d) : 0frame	0(d)	R/W	AGC Detection frame interval
	36	A_DEAD	07-06	Unused	-	-	Unused
			05-00	Range : 0 to 63(d)	20(d)	R/W	Dead value width of the AGC feed back gain
	37	A_GAIN	07-00	Range : 0 to 255(d) 0(d) : 0/256, 32(d) : 32/256 255(d) : 255/256	32(d)	R/W	AGC feed back gain
	38	A_LINEU	07-00	Range : 0 to 150(d) 0(d) : 0 line 149(d) : 298line 150(d) : 300line	149(d)	R/W	Upper limit of the number of integration lines. Set the number of line / 2 At AGC off this value is exposure lines
	39	A_LINEB	07-00	Range : 0 to 150(d) 0(d) : 0 line 1(d) : 2 line 150(d) : 300 line	1(d)	R/W	Lower limit of the number of integration lines. Set the number of line / 2
	3A	A_INTG	07-05	Unused	-	-	Unused
			04-00	Range : 0 to 24(d) 0(d) : 0dB, 12(d) : 12dB 24(d) : 24dB	12(d)	R/W	Amp gain setting at AGC off
	3B	A_MAXG	07-05	Unused	-	-	Unused
			04-00	Range : 0 to 24(d) 0(d) : 0dB, 21(d) : 21dB 24(d) : 24dB	21(d)	R/W	AGC Amp gain limiter
	3C	A_LEVEL	07-00	Range : 0 to 255(d)	120(d)	R/W	Y level target value
	3D	A_AVRG	07-00	Read only	-	R	Y Level average (read only)
	3E	A_INTGL	07-00	Read only	-	R	AGC Integration line number (read only)
	3F	A_INTGH	07-00	Read only	-	R	
	40	A_AGAIN	07-00	Read only	-	R	AGC Amp Gain (read only)

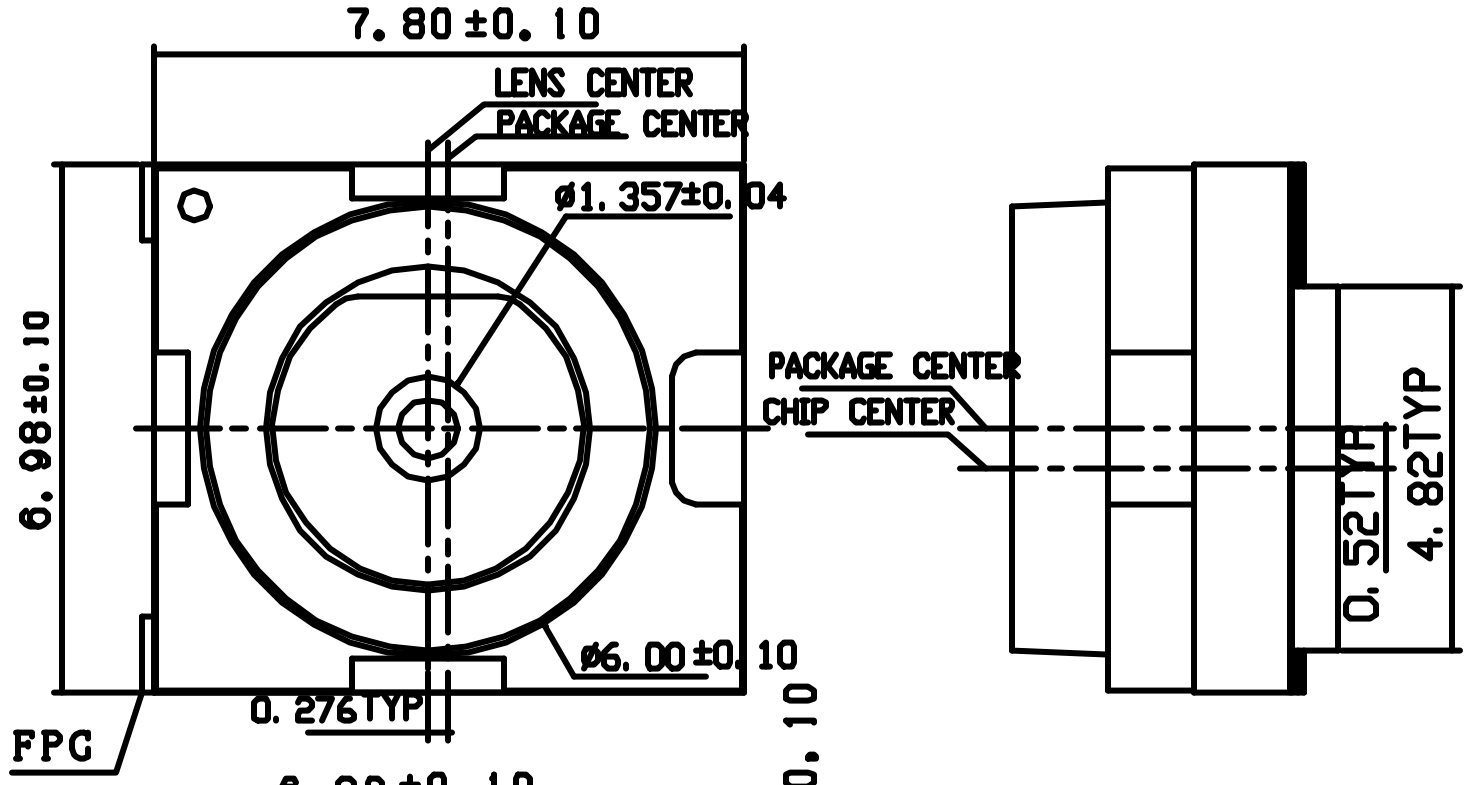
Group	Address	Name	Bit	Data	Default	R/W	Description
FLC	41	FMD	07	Read only	-	R	Flicker mode reading 0 : Flicker removal stop 1 : Flicker removal active
			06	Read only	-	R	0 : 60Hz detection, 1 : 50Hz detection
			05-02	Unused	-	-	Unused
			01	0 : - 1 : Flicker restart	0	R/W	Flicker start
			00	0 : Flicker mode auto 1 : Flicker mode off	0	R/W	Flicker mode on/off
	42	FTHR	07-04	Range : 1 to 15(d) 1(d) : 4count, 2(d) : 8count	2(d)	R/W	Counter setting of flicker detection (The times =setting valuex4)
			03-00	Range : 1 to 15(d) 1(d) : 4code, 5(d) : 20code	5(d)	R/W	Threshold of flicker detection (The threshold =setting valuex4)
	43	FACT	07-04	Range : 1 to 15(d) 1(d) : 4frame, 8(d) : 32frame	8(d)	R/W	Delay for starting auto flicker detection (The delay =setting valuex4)
			03-00	Range : 1 to 15(d) 1(d) : 4frame, 10(d) : 40frame	10(d)	R/W	Maximum frame number of AFD (The maximum frame =setting valuex4)

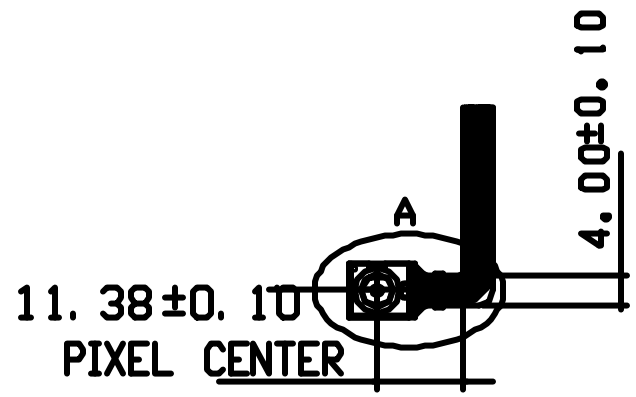
Group	Address	Name	Bit	Data	Default	R/W	Description
AWB	44	W_HSTT	07-00	Range : 0 to 255(d)	29(d)	R/W	Horizontal start position of the AWB window (The start pixel =setting valuex2)
	45	W_VSTT	07-00	Range : 0 to 255(d)	27(d)	R/W	Vertical start position of the AWB window (The start line =setting valuex2)
	46	W_WID	07-04	0000 : none, 0110 : 32line 0111 : 48line, 1000 : 64line 1001 : 96line, 1010 : 128line 1011 : 192line, 1100 : 256line	1011	R/W	Vertical line number of the AWB window.
			03-00	0000 : none, 0110 : 32pix 0111 : 48pix, 1000 : 64pix 1001 : 96pix, 1010 : 128pix 1011 : 192pix, 1100 : 256pix	1100	R/W	Horizontal pixel number of the AWB window.
	47	W_INTVL	07-00	Range : 0 to 255(d) 0(d) : 0frame	0(d)	R/W	AWB frame interval
	48	W_LIMB	07-00	Range : 0 to 255(d)	25(d)	R/W	Limit of blue signal of white area
	49	W_LIMR	07-00	Range : 0 to 255(d)	25(d)	R/W	Limit of red signal of white area
	4A	W_DEADB	07-00	Range : 0 to 255(d)	2(d)	R/W	Dead band width of AWB feed-back (Blue)
	4B	W_DEADR	07-00	Range : 0 to 255(d)	2(d)	R/W	Dead band width of AWB feed-back (Red)
	4C	W_GAIN	07-00	Range : 0 to 255(d) 0(d) : gain = 0 / 256 16(d) : gain = 16 / 256 255(d) : gain = 255 /256	16(d)	R/W	AWB feed back gain
	4D	W_GB0	07-00	Range : -128 to 127(d)	0(d)	R/W	4150K initial gain (Blue)
	4E	W_GR0	07-00		0(d)	R/W	4150K Initial gain (Red)
	4F	W_GB1	07-00		-32(d)	R/W	6500K Fixed gain setting (Blue)
	50	W_GR1	07-00		26(d)	R/W	6500K Fixed gain setting (Red)
	51	W_GB2	07-00		-16(d)	R/W	5000K Fixed gain setting (Blue)
	52	W_GR2	07-00		6(d)	R/W	5000K Fixed gain setting (Red)
	53	W_GB3	07-00		27(d)	R/W	2856K Fixed gain setting (Blue)
	54	W_GR3	07-00		-54(d)	R/W	2856K Fixed gain setting (Red)
	55	W_AVGB	07-00	Read only	-	R	Average of B - Y
	56	W_AVGR	07-00	Read only	-	R	Average of R - Y
RSV	57	RSV57	07-00	Unused	-	-	Unused

Group	Address	Name	Bit	Data	Default	R/W	Description
TG	58	HTC	07-00	Range : 0 to 255(d) 0(d) : 500ck, 255(d) : 1010ck	0(d)	R/W	Horizontal counters (Counter = set value * 2 + 500)
	59	HSYS	07-00	Range : 0 to 255(d) 0(d) : 0ck, 50(d) : 50ck	50(d)	R/W	HD start position
	5A	HSYE	07-00	Range : 0 to 255(d) 0(d) : 0pix, 46(d) : 46pix	46(d)	R/W	HD pixel width
	5B	RSV5B	07-00	Unused	-	-	Unused
	5C	-	07-06	Unused	-	-	Unused
		VSYS	05-03	Range : 0 to 7(d)	1(d)	R/W	VD start position
		VSYE	02-00	Range : 0 to 7(d)	0(d)	R/W	VD end position
	5D	VSYHADJ	07-06	Range : 0 to 3(d) VD edge alignment	0(d)	R/W	00: Align both rising and falling edge to the rising edge of HSYNC 01: Align rising edge to the falling edge of AVH, and falling edge to the rising of AVH 10: Align rising edge to the rising edge of AVH, and falling edge to the falling of AVH 11: Align rising edge to the falling edge of AVH, and falling edge to the falling of AVH
			05-03	Range : 0 to 7(d) 0(d) : -5CLK 5(d) : 0CLK 7(d) : +2CLK	5(d)	R/W	VD rising edge timing adjustment
			02-00	Range : 0 to 7(d) 0(d) : +5CLK 5(d) : 0CLK 7(d) : -2CLK	5(d)	R/W	VD falling edge timing adjustment
	5E	AV_HS	07	Unused	-	-	Unused
			06-00	Range : 0 to 127(d) 0(d) : 0pix 1(d) : 1pix 127(d) : 127pix	1(d)	R/W	Horizontal start position of AVH in pixels
	5F	AV_HE	07	Unused	-	-	Unused
			06-00	Range : 0 to 127(d) 0(d) : 0pix 1(d) : 1pix 127(d) : 127pix	1(d)	R/W	Horizontal end position of AVH in pixels
	60	AV_VS	07	Unused	-	-	Unused
			06-00	Range : 0 to 127(d) 0(d) : 0pix 127(d) : 127pix	0(d)	R/W	Vertical start position of AVH in pixels
	61	AV_VE	07	Unused	-	-	Unused
			06-00	Range : 0 to 127(d) 0(d) : 0pix 127(d) : 127pix	0(d)	R/W	Vertical end position of AVH in pixels

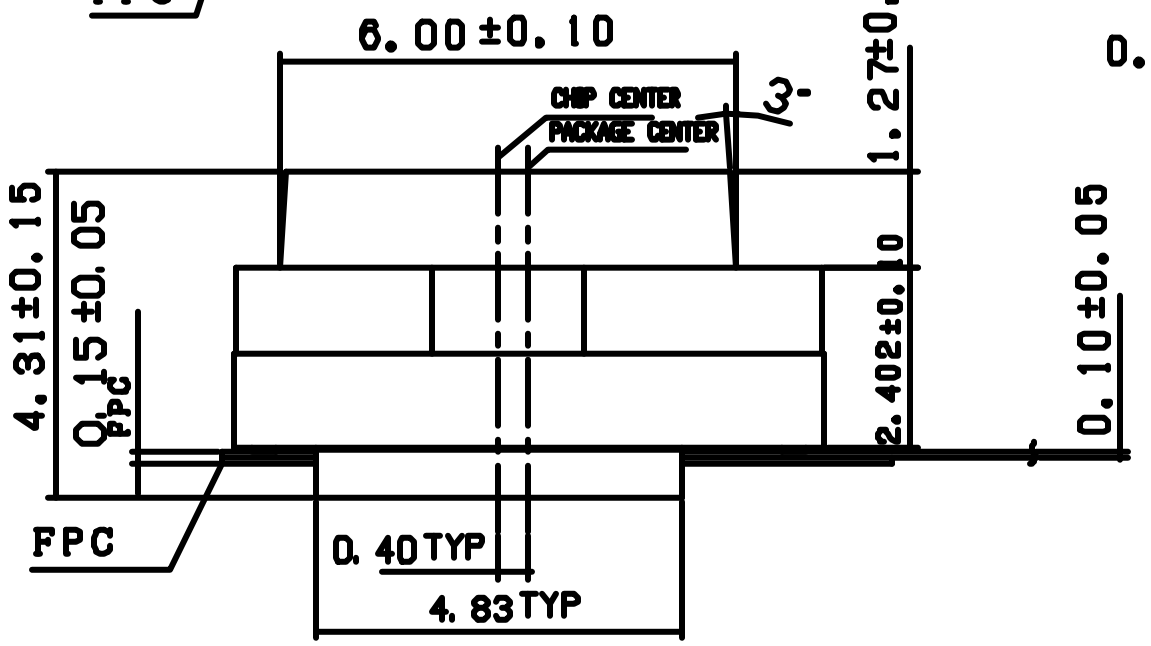
Group	Address	Name	Bit	Data	Default	R/W	Description
IMGR	62	PWRSV	07	Unused	-	-	Unused
			06	0 : off, 1 : on	0	R/W	Power save mode on/off
			05	0:Continuous operation 1:long exposure (at power save period)	0	R/W	Long exposure mode
			04-00	Range : 2 to 31(d) 2(d) : 2frame	2(d)	R/W	Power save period(frame number)
	63	BKLVL	07-00	Range : 0 to 255(d) 16(d) : 16code (1.064V)	16(d)	R/W	Black clamp level
	64	BKCLP	07	0 : on, 1 : off	0	R/W	Black clamp on/off
			06	0 : every line, 1 : every frame	1	R/W	Black clamp mode
			05-03	Range : 0 to 7(d) 1(d) : 1pixel	1(d)	R/W	Start pixel of black clamp
			02-00	Range : 0 to 7(d) 4(d) : 3pixel (=7-X)	4(d)	R/W	End pixel of black clamp X: setting difference from start position(7)
	65	ANLG1	07-06	Unused	-	-	Unused
			05-04	00 : 4ck, 01 : 5ck 10 : 6ck, 11 : 7ck	00	R/W	Reserved for timing adjustment (Please use default setting)
			03-01	Unused	-	-	Unused
			00	0:gain twice, 1:gain 4times	0	R/W	Aperture gain
	66	ANLG2	07-06	Unused	-	-	Unused
			05-04	00 : 0ns, 01 : 3.6ns 10 : 7ns, 11 : 10.4ns	00	R/W	OCLP rising edge delay
			03-02	00 : 30ns, 01 : 39ns 10 : 43ns, 11 : 47ns	00	R/W	OSH rising edge delay
			01-00	00 : 0ns, 01 : 1ns 10 : 2ns, 11 : 3ns	00	R/W	CLKAD phase delay
	67	ANLG3	07-06	Unused	-	-	Unused
			05	0 : 2/2, 1 : 1/2	0	R/W	Analog power reduction mode
			04	0 : just setting, 1 : 1frame delay	0	R/W	Please use default setting
			03	0 : gain x 1.5, 1 : gain x 2.2	1	R/W	Gain of AMP1 setting
			02	0 : no reduction, 1 : reduction mode	0	R/W	ADC power reduction (HBLANK OFF)
			01-00	00 : gamma off 01 : gamma1 (192code = 0.4V) 10 : gamma2 (192code= 0.5V) 11 : Unused	00	R/W	Gamma of AD converter
	68	TEST	07	test	0	R/W	test
			06	test	0	R/W	test
			05-02	Unused	-	-	Unused
			01	0:normaly, 1:FCLK=VCLK	0	R/W	VCLK
			00	0:normaly, 1:FCLK=HCLK	0	R/W	HCLK
	69	ANLG4	07	Unused	-	-	-
			06	0:off, 1:om			Digital clamp correcting on / off
			05	0:average, 1:weighted			Choosing correcting method
			04-00	0:0dB - 24dB 20:20dB - 24dB 24:24dB	20(d)	R/W	Defective pixel correcting filter on / off

Group	Address	Name	Bit	Data	Default	R/W	Description
TEST	6A	Reserved	07-00	Unused	-	-	Unused
	6B	RSV6B	07-00	Unused	-	-	Unused
	6C	TEST1	07-00	test	-	R/W	test
	6D	TEST2	07-00	test	-	R/W	test
	6E	TEST3	07-00	test	-	R/W	test
	6F	TEST4	07-00	test	-	R/W	test

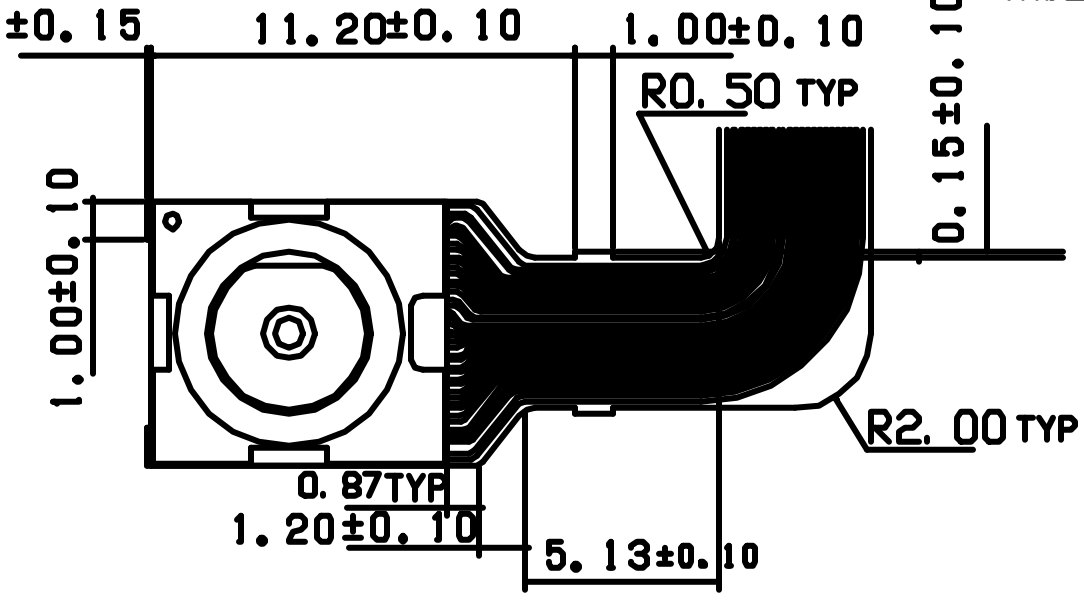




外形図(SCL×1)



PACKAGE FIGURE(SCLX10)



DETAIL VIEW(A)

Type 1 REFERENCE FIGURE

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