FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50105-2E

*MCP (Multi-Chip Package) FLASH MEMORY & SRAM*

**CMOS**

# 8M (× 8/× 16) FLASH MEMORY & 2M (× 8) STATIC RAM

# MB84VA2002-10/MB84VA2003-10



## ■ FEATURES

- **Power supply voltage of 2.7 to 3.6 V**
- **High performance**
  100 ns maximum access time
- **Operating Temperature**
  –20 to +85°C

### — FLASH MEMORY

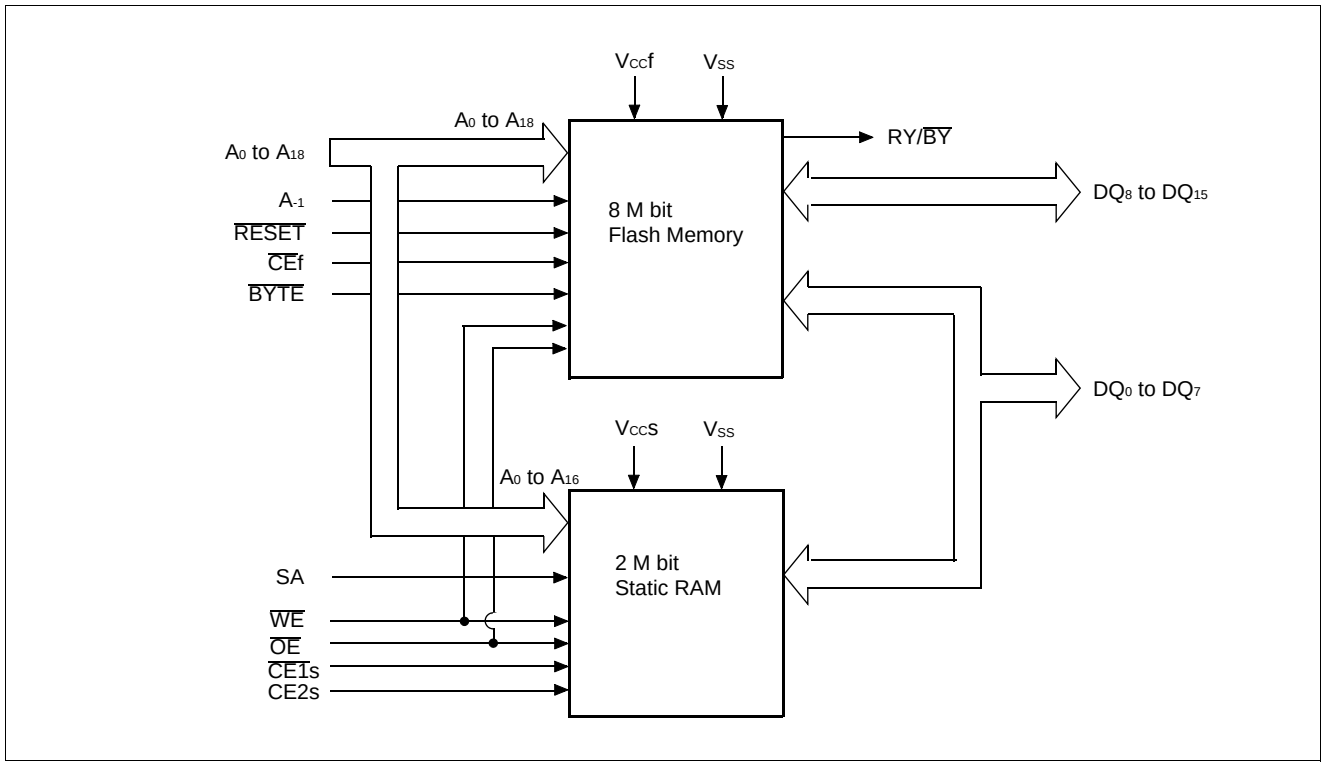
- **Minimum 100,000 write/erase cycles**
- **Sector erase architecture**
  One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  MB84VA2002: Top sector
  MB84VA2003: Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready-Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low $V_{CC}$ write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Please refer to "MBM29LV800TA/BA" data sheet in detailed function**

### — SRAM

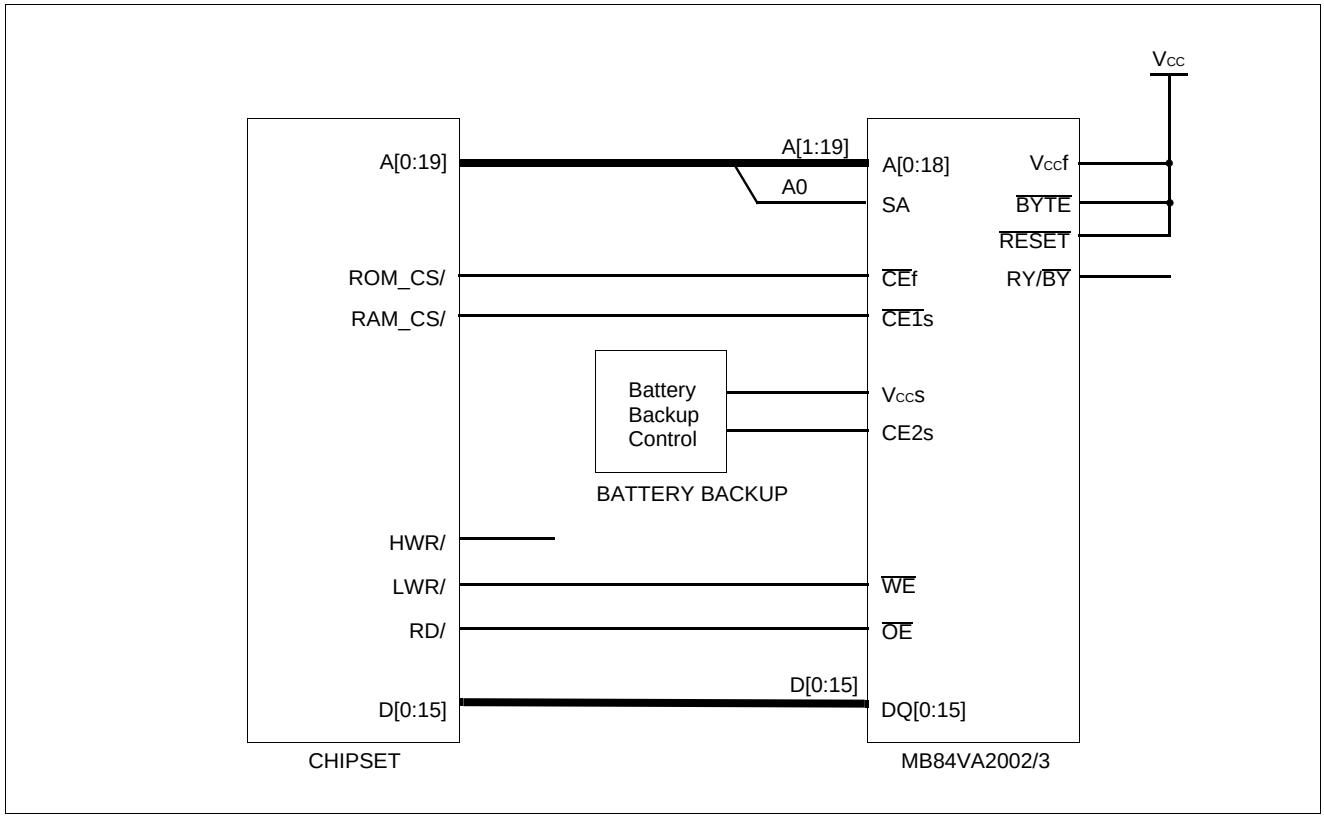
- **Power dissipation**
  Operating : 35 mA max.
  Standby : 50 µA max.
- **Power down features using $\overline{\text{CE1}}$s and CE2s**
- **Data retention supply voltage: 2.0 V to 3.6 V**

Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

## ■ BLOCK DIAGRAM




## ■ EXAMPLE OF CONNECTION WITH CHIPSET



## ■ PIN ASSIGNMENTS

(Top View)

| | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 6 | $\overline{CE1}$s | $V_{SS}$ | $DQ_1$ | $A_1$ | $A_2$ | $A_4$ | CE2s | $A_9$ |
| 5 | $A_{10}$ | $DQ_5$ | $DQ_2$ | $A_0$ | $A_3$ | $A_7$ | RY/$\overline{BY}$ | $A_{14}$ |
| 4 | $\overline{OE}$ | $DQ_7$ | $DQ_4$ | $DQ_0$ | $A_6$ | $A_{18}$ | $\overline{RESET}$ | $A_{15}$ |
| 3 | $A_{11}$ | $A_8$ | $A_5$ | $DQ_8$ | $DQ_3$ | $DQ_{12}$ | $A_{12}$ | $\overline{BYTE}$ |
| 2 | $A_{13}$ | $A_{17}$ | SA* | $\overline{CE}$f | $DQ_{10}$ | $V_{CC}$f | $DQ_6$ | $DQ_{15}/A_{-1}$ |
| 1 | $\overline{WE}$ | $V_{CC}$s | $A_{16}$ | $V_{SS}$ | $DQ_9$ | $DQ_{11}$ | $DQ_{13}$ | $DQ_{14}$ |

*: $A_{17}$ for SRAM

**Table 1 Pin Configuration**

| Pin | Function | Input/ Output |
|---|---|---|
| $A_0$ to $A_{16}$ | Address Inputs (Common) | I |
| $A_{-1}$, $A_{17}$ to $A_{18}$ | Address Input (Flash) | I |
| SA | Address Input (SRAM) | I |
| $DQ_0$ to $DQ_7$ | Data Inputs/Outputs (Common) | I/O |
| $DQ_8$ to $DQ_{15}$ | Data Inputs/Outputs (Flash) | I/O |
| $\overline{CE}$f | Chip Enable (Flash) | I |
| $\overline{CE1}$s | Chip Enable (SRAM) | I |
| CE2s | Chip Enable (SRAM) | I |
| $\overline{OE}$ | Output Enable (Common) | I |
| $\overline{WE}$ | Write Enable (Common) | I |
| RY/$\overline{BY}$ | Ready/Busy Outputs (Flash) | O |
| $\overline{BYTE}$ | Selects 8-bit or 16-bit mode (Flash) | I |
| $\overline{RESET}$ | Hardware Reset Pin/Sector Protection Unlock (Flash) | I |
| N.C. | No Internal Connection | — |
| $V_{SS}$ | Device Ground (Common) | Power |
| $V_{CC}$f | Device Power Supply (Flash) | Power |
| $V_{CC}$s | Device Power Supply (SRAM) | Power |

## ■ PRODUCT LINE UP

| | | Flash Memory | SRAM |
|---|---|---|---|
| Ordering Part No. | $V_{CC}$ = 3.0 V $^{+0.6\ V}_{-0.3\ V}$ | MB84VA2002-10/MB84VA2003-10 | |
| Max. Address Access Time (ns) | | 100 | 100 |
| Max. $\overline{CE}$ Access Time (ns) | | 100 | 100 |
| Max. $\overline{OE}$ Access Time (ns) | | 40 | 50 |

## ■ BUS OPERATIONS

**Table 2 User Bus Operations ($\overline{BYTE}$=$V_{IL}$)**

| Operation (1), (3) | $\overline{CEf}$ | $\overline{CE1s}$ | CE2s | $\overline{OE}$ | $\overline{WE}$ | $DQ_0$ to $DQ_7$ | $DQ_8$ to $DQ_{15}$ | $\overline{RESET}$ |
|---|---|---|---|---|---|---|---|---|
| Full Standby | H | H | X | X | X | HIGH-Z | HIGH-Z | H |
| | | X | L | | | | | |
| Output Disable | X | X | X | H | H | HIGH-Z | HIGH-Z | H |
| Read from Flash (2) | L | H | X | L | H | $D_{OUT}$ | HIGH-Z | H |
| | | X | L | | | | | |
| Write to Flash | L | H | X | H | L | $D_{IN}$ | HIGH-Z | H |
| | | X | L | | | | | |
| Read from SRAM | H | L | H | L | H | $D_{OUT}$ | HIGH-Z | H |
| Write to SRAM | H | L | H | X | L | $D_{IN}$ | HIGH-Z | H |
| Flash Hardware Reset | X | H | X | X | X | HIGH-Z | HIGH-Z | L |
| | | X | L | | | | | |

**Table 3 User Bus Operations ($\overline{BYTE}$=$V_{IH}$)**

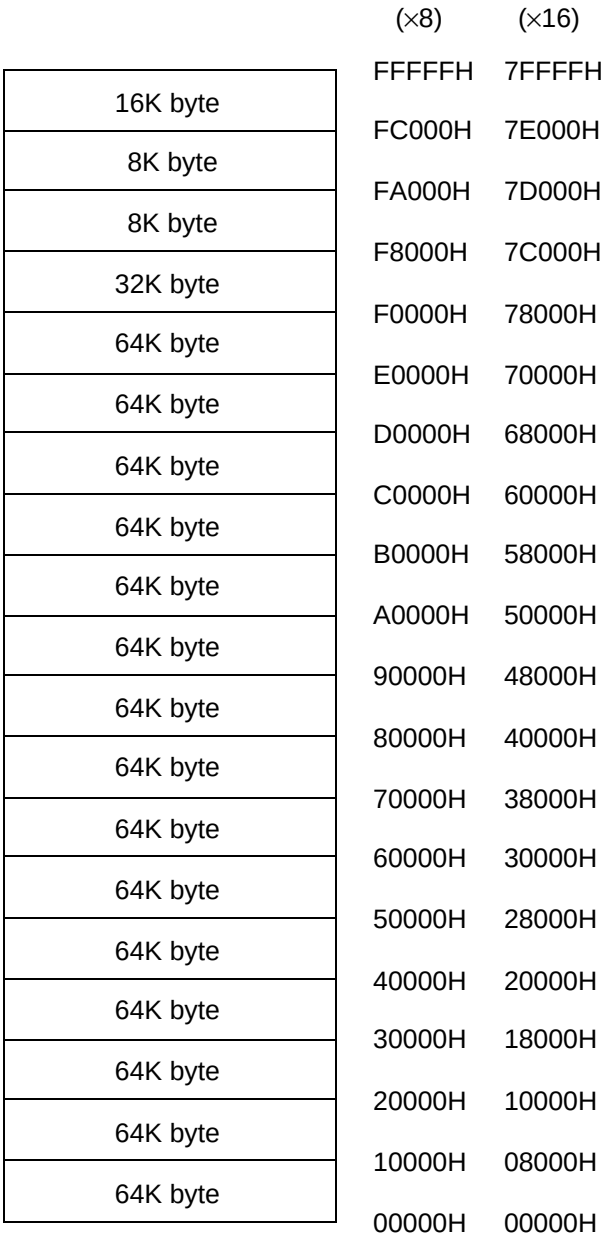
| Operation (1), (3) | $\overline{CEf}$ | $\overline{CE1s}$ | CE2s | $\overline{OE}$ | $\overline{WE}$ | $DQ_0$ to $DQ_7$ | $DQ_8$ to $DQ_{15}$ | $\overline{RESET}$ |
|---|---|---|---|---|---|---|---|---|
| Full Standby | H | H | X | X | X | HIGH-Z | HIGH-Z | H |
| | | X | L | | | | | |
| Output Disable | X | X | X | H | H | HIGH-Z | HIGH-Z | H |
| Read from Flash (2) | L | H | X | L | H | $D_{OUT}$ | $D_{OUT}$ | H |
| | | X | L | | | | | |
| Write to Flash | L | H | X | H | L | $D_{IN}$ | $D_{IN}$ | H |
| | | X | L | | | | | |
| Read from SRAM | H | L | H | L | H | $D_{OUT}$ | HIGH-Z | H |
| Write to SRAM | H | L | H | X | L | $D_{IN}$ | HIGH-Z | H |
| Flash Hardware Reset | X | H | X | X | X | HIGH-Z | HIGH-Z | L |
| | | X | L | | | | | |

**Legend:** L = $V_{IL}$, H = $V_{IH}$, X = $V_{IL}$ or $V_{IH}$. See DC Characteristics for voltage levels.

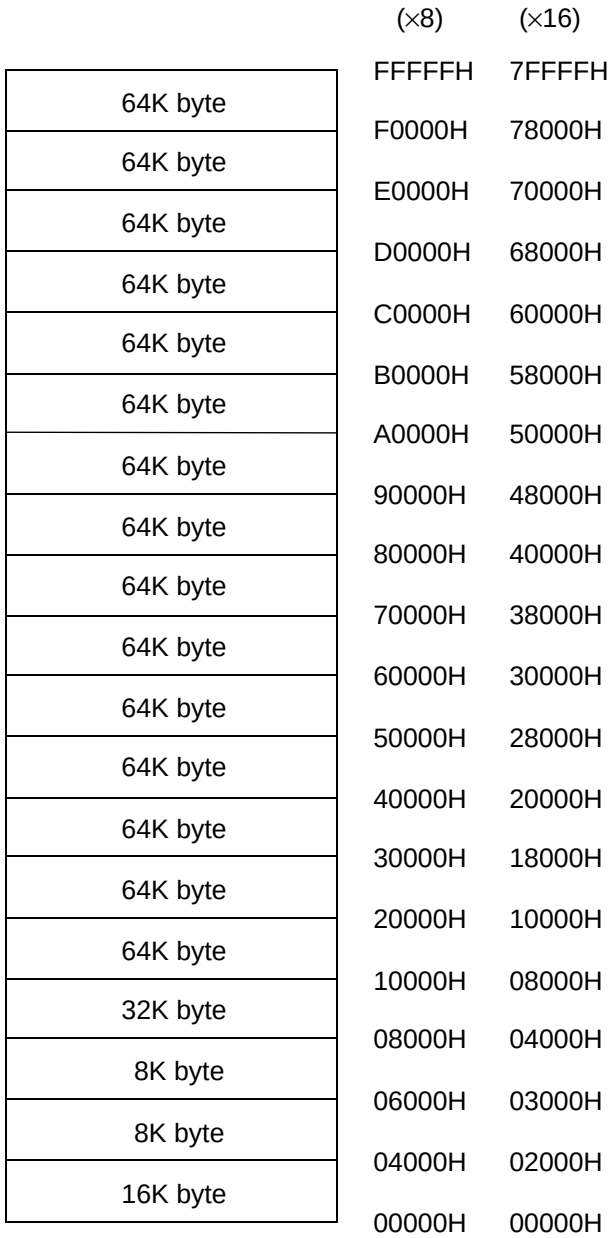
**Notes:** 1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be $V_{IL}$ if $\overline{OE}$ is $V_{IL}$, $\overline{OE}$ at $V_{IH}$ initiates the write operations.
4. Do not apply $\overline{CEf}$ = $V_{IL}$, $\overline{CE1s}$ = $V_{IL}$ and CE2s = $V_{IH}$ at a time.

## ■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes.
- Individual-sector, multiple-sector, or bulk-erase capability.




**MB84VA2002 Sector Architecture**




**MB84VA2003 Sector Architecture**

**Table 4 Sector Address Tables (MB84VA2002)**

| Sector Address | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | Address Range (×8) | Address Range (×16) |
|---|---|---|---|---|---|---|---|---|---|
| SA0 | 0 | 0 | 0 | 0 | X | X | X | 00000H to 0FFFFH | 00000H to 07FFFH |
| SA1 | 0 | 0 | 0 | 1 | X | X | X | 10000H to 1FFFFH | 08000H to 0FFFFH |
| SA2 | 0 | 0 | 1 | 0 | X | X | X | 20000H to 2FFFFH | 10000H to 17FFFH |
| SA3 | 0 | 0 | 1 | 1 | X | X | X | 30000H to 3FFFFH | 18000H to 1FFFFH |
| SA4 | 0 | 1 | 0 | 0 | X | X | X | 40000H to 4FFFFH | 20000H to 27FFFH |
| SA5 | 0 | 1 | 0 | 1 | X | X | X | 50000H to 5FFFFH | 28000H to 2FFFFH |
| SA6 | 0 | 1 | 1 | 0 | X | X | X | 60000H to 6FFFFH | 30000H to 37FFFH |
| SA7 | 0 | 1 | 1 | 1 | X | X | X | 70000H to 7FFFFH | 38000H to 3FFFFH |
| SA8 | 1 | 0 | 0 | 0 | X | X | X | 80000H to 8FFFFH | 40000H to 47FFFH |
| SA9 | 1 | 0 | 0 | 1 | X | X | X | 90000H to 9FFFFH | 48000H to 4FFFFH |
| SA10 | 1 | 0 | 1 | 0 | X | X | X | A0000H to AFFFFH | 50000H to 57FFFH |
| SA11 | 1 | 0 | 1 | 1 | X | X | X | B0000H to BFFFFH | 58000H to 5FFFFH |
| SA12 | 1 | 1 | 0 | 0 | X | X | X | C0000H to CFFFFH | 60000H to 67FFFH |
| SA13 | 1 | 1 | 0 | 1 | X | X | X | D0000H to DFFFFH | 68000H to 6FFFFH |
| SA14 | 1 | 1 | 1 | 0 | X | X | X | E0000H to EFFFFH | 70000H to 77FFFH |
| SA15 | 1 | 1 | 1 | 1 | 0 | X | X | F0000H to F7FFFH | 78000H to 7BFFFH |
| SA16 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | F8000H to F9FFFH | 7C000H to 7CFFFH |
| SA17 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FA000H to FBFFFH | 7D000H to 7DFFFH |
| SA18 | 1 | 1 | 1 | 1 | 1 | 1 | X | FC000H to FFFFFH | 7E000H to 7FFFFH |

**Table 5 Sector Address Tables (MB84VA2003)**

| Sector Address | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | Address Range (×8) | Address Range (×16) |
|---|---|---|---|---|---|---|---|---|---|
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 00000H to 03FFFH | 00000H to 01FFFH |
| SA1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 04000H to 05FFFH | 02000H to 02FFFH |
| SA2 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 06000H to 07FFFH | 03000H to 03FFFH |
| SA3 | 0 | 0 | 0 | 0 | 1 | X | X | 08000H to 0FFFFH | 04000H to 07FFFH |
| SA4 | 0 | 0 | 0 | 1 | X | X | X | 10000H to 1FFFFH | 08000H to 0FFFFH |
| SA5 | 0 | 0 | 1 | 0 | X | X | X | 20000H to 2FFFFH | 10000H to 17FFFH |
| SA6 | 0 | 0 | 1 | 1 | X | X | X | 30000H to 3FFFFH | 18000H to 1FFFFH |
| SA7 | 0 | 1 | 0 | 0 | X | X | X | 40000H to 4FFFFH | 20000H to 27FFFH |
| SA8 | 0 | 1 | 0 | 1 | X | X | X | 50000H to 5FFFFH | 28000H to 2FFFFH |
| SA9 | 0 | 1 | 1 | 0 | X | X | X | 60000H to 6FFFFH | 30000H to 37FFFH |
| SA10 | 0 | 1 | 1 | 1 | X | X | X | 70000H to 7FFFFH | 38000H to 3FFFFH |
| SA11 | 1 | 0 | 0 | 0 | X | X | X | 80000H to 8FFFFH | 40000H to 47FFFH |
| SA12 | 1 | 0 | 0 | 1 | X | X | X | 90000H to 9FFFFH | 48000H to 4FFFFH |
| SA13 | 1 | 0 | 1 | 0 | X | X | X | A0000H to AFFFFH | 50000H to 57FFFH |
| SA14 | 1 | 0 | 1 | 1 | X | X | X | B0000H to BFFFFH | 58000H to 5FFFFH |
| SA15 | 1 | 1 | 0 | 0 | X | X | X | C0000H to CFFFFH | 60000H to 67FFFH |
| SA16 | 1 | 1 | 0 | 1 | X | X | X | D0000H to DFFFFH | 68000H to 6FFFFH |
| SA17 | 1 | 1 | 1 | 0 | X | X | X | E0000H to EFFFFH | 70000H to 77FFFH |
| SA18 | 1 | 1 | 1 | 1 | X | X | X | F0000H to FFFFFH | 78000H to 7FFFFH |

**Table 6. 1 Flash Memory Autoselect Codes**

| Type | | | $A_6$ | $A_1$ | $A_0$ | $A_{-1}$*1 | Code (HEX) |
|---|---|---|---|---|---|---|---|
| Manufacturer's Code | | | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | 04H |
| Device Code | MB84VA2002 | Byte | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | DAH |
| | | Word | | | | X | 22DAH |
| | MB84VA2003 | Byte | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | 5BH |
| | | Word | | | | X | 225BH |

*1: $A_{-1}$ is for Byte mode.

**Table 6. 2 Expanded Autoselect Code Table**

| Type | | Code | $DQ_{15}$ | $DQ_{14}$ | $DQ_{13}$ | $DQ_{12}$ | $DQ_{11}$ | $DQ_{10}$ | $DQ_9$ | $DQ_8$ | $DQ_7$ | $DQ_6$ | $DQ_5$ | $DQ_4$ | $DQ_3$ | $DQ_2$ | $DQ_1$ | $DQ_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | | 04H | $A_{-1}$/0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Device Code | MB84VA2002 (B) (W) | DAH 22DAH | $A_{-1}$ 0 | HI-Z 0 | HI-Z 1 | HI-Z 0 | HI-Z 0 | HI-Z 0 | HI-Z 1 | HI-Z 0 | 1 1 | 1 1 | 0 0 | 1 1 | 1 1 | 0 0 | 1 1 | 0 0 |
| | MB84VA2003 (B) (W) | 5BH 225BH | $A_{-1}$ 0 | HI-Z 0 | HI-Z 1 | HI-Z 0 | HI-Z 0 | HI-Z 0 | HI-Z 1 | HI-Z 0 | 0 0 | 1 1 | 0 0 | 1 1 | 1 1 | 0 0 | 1 1 | 1 1 |

(B): Byte mode
(W): Word mode

**Table 7 Flash Memory Command Definitions**

| Command Sequence | | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Read/Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data |
| Read/ Reset | word | 1 | XXXH | F0H | — | — | — | — | — | — | — | — | — | — |
| | Byte | | | | | | | | | | | | | |
| Read/ Reset | word | 3 | 555H | AAH | 2AAH | 55H | 555H | F0H | RA | RD | — | — | — | — |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Autoselect | word | 3 | 555H | AAH | 2AAH | 55H | 555H | 90H | — | — | — | — | — | — |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Program | word | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA | PD | — | — | — | — |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Chip Erase | word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| | Byte | | AAAH | | 555H | | AAAH | | AAAH | | 555H | | AAAH | |
| Sector Erase | word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | SA | 30H |
| | Byte | | AAAH | | 555H | | AAAH | | AAAH | | 555H | | | |
| Sector Erase Suspend | | | Erase can be suspended during sector erase with Addr ("H" or "L"). Data (B0H) | | | | | | | | | | | |
| Sector Erase Resume | | | Erase can be resumed after suspend with Addr ("H" or "L"). Data (30H) | | | | | | | | | | | |
| Set to Fast Mode | word | 3 | 555H | AAH | 2AAH | 55H | 555H | 20H | — | — | — | — | — | — |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Fast Program (Note) | word | 2 | XXXH | A0H | PA | PD | — | — | — | — | — | — | — | — |
| | Byte | | XXXH | | | | | | | | | | | |
| Reset from Fast Mode | word | 2 | XXXH | 90H | XXXH | F0H | — | — | — | — | — | — | — | — |
| | Byte | | XXXH | | XXXH | | | | | | | | | |
| Extended Sector Protect | word | 4 | XXXH | 60H | SPA | 60H | SPA | 40H | SPA | SD | — | — | — | — |
| | Byte | | | | | | | | | | | | | |

Address bits $A_{11}$ to $A_{20}$ = X = "H" or "L" for all address commands except for Program Address (PA) and Sector Address (SA).

Bus operations are defined in Table 2.

Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

RA =Address of the memory location to be read.

PA =Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.

SA =Address of the sector to be erased. The combination of $A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, and $A_{13}$ will uniquely select any sector.

RD =Data read from location RA during read operation.

PD =Data to be programmed at location PA.

SPA =Sector address to be protected. Set sector address (SA) and ($A_6$, $A_1$, $A_0$) = (0, 1, 0).

SD =Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

**Note:** This command is valid while Fast Mode.

## ■ ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | –55°C to +125°C |
| Ambient Temperature with Power Applied | –25°C to +85°C |
| Voltage with Respect to Ground All pins (Note) | –0.3 V to $V_{CC}f$ +0.5 V |
| | –0.3 V to $V_{CC}s$ +0.5 V |
| $V_{CC}f$/$V_{CC}s$ Supply (Note) | –0.3 V to +4.6 V |

**Note:** Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negativeovershoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are $V_{CC}f$ +0.5 V or $V_{CC}s$ +0.5 V. During voltage transitions, outputs may positive overshoot to $V_{CC}$ +2.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING RANGES

Commercial Devices

| | |
|---|---|
| Ambient Temperature ($T_A$) | –20°C to +85°C |
| $V_{CC}f$/$V_{CC}s$ Supply Voltages | +2.7 V to +3.6 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ DC CHARACTERISTICS

| Parameter Symbol | Parameter Description | Test Conditions | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | — | | | –1.0 | — | +1.0 | µA |
| $I_{LO}$ | Output Leakage Current | — | | | –1.0 | — | +1.0 | µA |
| $I_{CC1}f$ | Flash $V_{CC}$ Active Current (Read) | $V_{CC}f$ = $V_{CC}$ Max., $\overline{CE}f$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | Byte | $t_{CYCLE}$ = 10 MHz | — | — | 22 | mA |
| | | | Word | | — | — | 25 | |
| | | | Byte | $t_{CYCLE}$ = 5 MHz | — | — | 12 | |
| | | | Word | | — | — | 15 | |
| $I_{CC2}f$ | Flash $V_{CC}$ Active Current (Program/Erase) | $V_{CC}f$ = $V_{CC}$ Max., $\overline{CE}f$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | | | — | — | 35 | mA |
| $I_{CC1}s$ | SRAM $V_{CC}$ Active Current | $V_{CC}s$ = $V_{CC}$ Max., $\overline{CE1}s$ = $V_{IL}$, CE2s = $V_{IH}$ | | $t_{CYCLE}$ =10 MHz | — | — | 40 | mA |
| | | | | $t_{CYCLE}$ = 1 MHz | — | — | 12 | mA |
| $I_{CC2}s$ | SRAM $V_{CC}$ Active Current | $\overline{CE1}s$ = 0.2 V, CE2s = $V_{CC}s$ – 0.2 V, $\overline{WE}$ = $V_{CC}s$ – 0.2 V | | $t_{CYCLE}$ = 10 MHz | — | — | 35 | mA |
| | | | | $t_{CYCLE}$ = 1 MHz | — | — | 6 | mA |
| $I_{SB1}f$ | Flash $V_{CC}$ Standby Current | $V_{CC}f$ = $V_{CC}$ Max., $\overline{CE}f$ = $V_{CC}f$ ± 0.3 V, $\overline{RESET}$ = $V_{CC}f$ ± 0.3 V | | | — | — | 5 | µA |
| $I_{SB2}f$ | Flash $V_{CC}$ Standby Current ($\overline{RESET}$) | $V_{CC}f$ = $V_{CC}$ Max., $\overline{RESET}$ = $V_{SS}$ ± 0.3 V | | | — | — | 5 | µA |
| $I_{SB1}s$ | SRAM $V_{CC}$ Standby Current | $\overline{CE1}s$ = $V_{IH}$ or CE2s = $V_{IL}$ | | | — | — | 2 | mA |
| $I_{SB2}s$** | SRAM $V_{CC}$ Standby Current | $\overline{CE1}s$ = $V_{CC}$ – 0.2 V or CE2s = 0.2 V | $V_{CC}s$ = 3.0 V ±10% | $T_A$ = 25°C | — | 1 | 2.5 | µA |
| | | | | $T_A$ = –20 to +85°C | — | — | 55 | µA |
| | | | $V_{CC}s$ = 3.3 V ±0.3 V | $T_A$ = 25°C | — | 1.5 | 3 | µA |
| | | | | $T_A$ = –20 to +85°C | — | — | 60 | µA |
| | | | $V_{CC}s$ = 3.0 V | $T_A$ = 25°C | — | 1 | 2 | µA |
| | | | | $T_A$ = –20 to +40°C | — | — | 5 | µA |
| | | | | $T_A$ = –20 to +85°C | — | — | 50 | µA |
| $V_{IL}$ | Input Low Level | — | | | –0.3 | — | 0.6 | V |
| $V_{IH}$ | Input High Level | — | | | 2.2 | — | $V_{CC}$+0.3* | V |
| $V_{OL}$ | Output Low Voltage Level | $I_{OL}$ = 2.1 mA, $V_{CC}f$ = $V_{CC}s$ = $V_{CC}$ Min. | | | — | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage Level | $I_{OH}$ = –500 µA, $V_{CC}f$ = $V_{CC}s$ = $V_{CC}$ Min. | | | $V_{CC}$ – 0.5 | — | — | V |
| $V_{LKO}$ | Flash Low $V_{CC}$ Lock-Out Voltage | — | | | 2.3 | — | 2.5 | V |

* : $V_{CC}$ indicate lower of $V_{CC}f$ or $V_{CC}s$

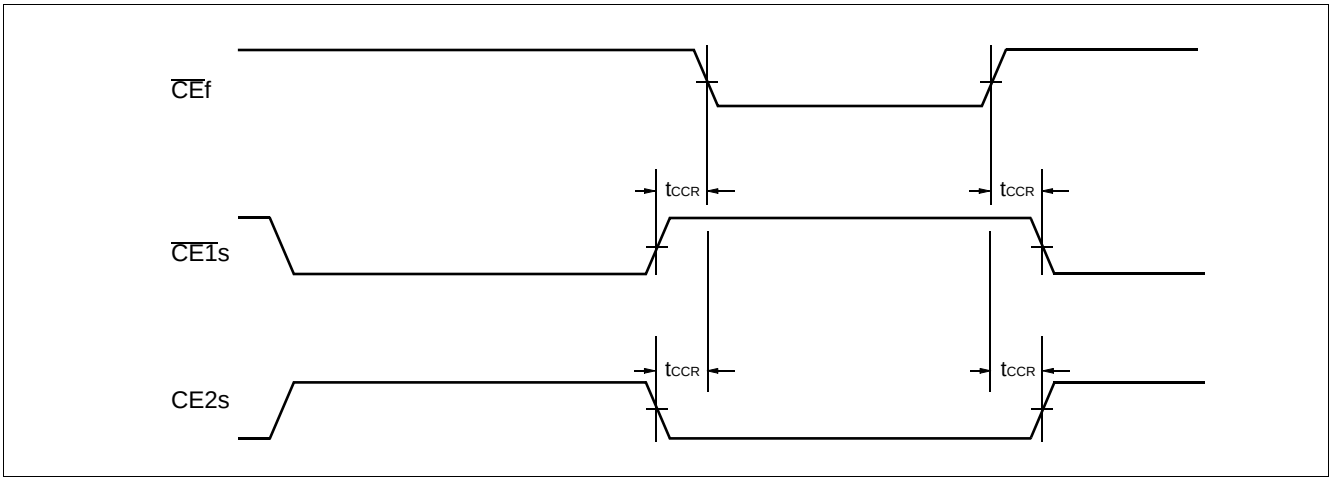
** :During standby mode with $\overline{CE1}s$ = $V_{CCS}$ – 0.2 V, CE2s should be CE2s < 0.2V or CE2s > $V_{CCS}$ – 0.2V

## ■ AC CHARACTERISTICS

- **$\overline{CE}$ Timing**

| Parameter Symbols | | Description | Test Setup | | -10 | Unit |
|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | | |
| — | $t_{CCR}$ | $\overline{CE}$ Recover Time | — | Min. | 0 | ns |

- **Timing Diagram for alternating SRAM to Flash**

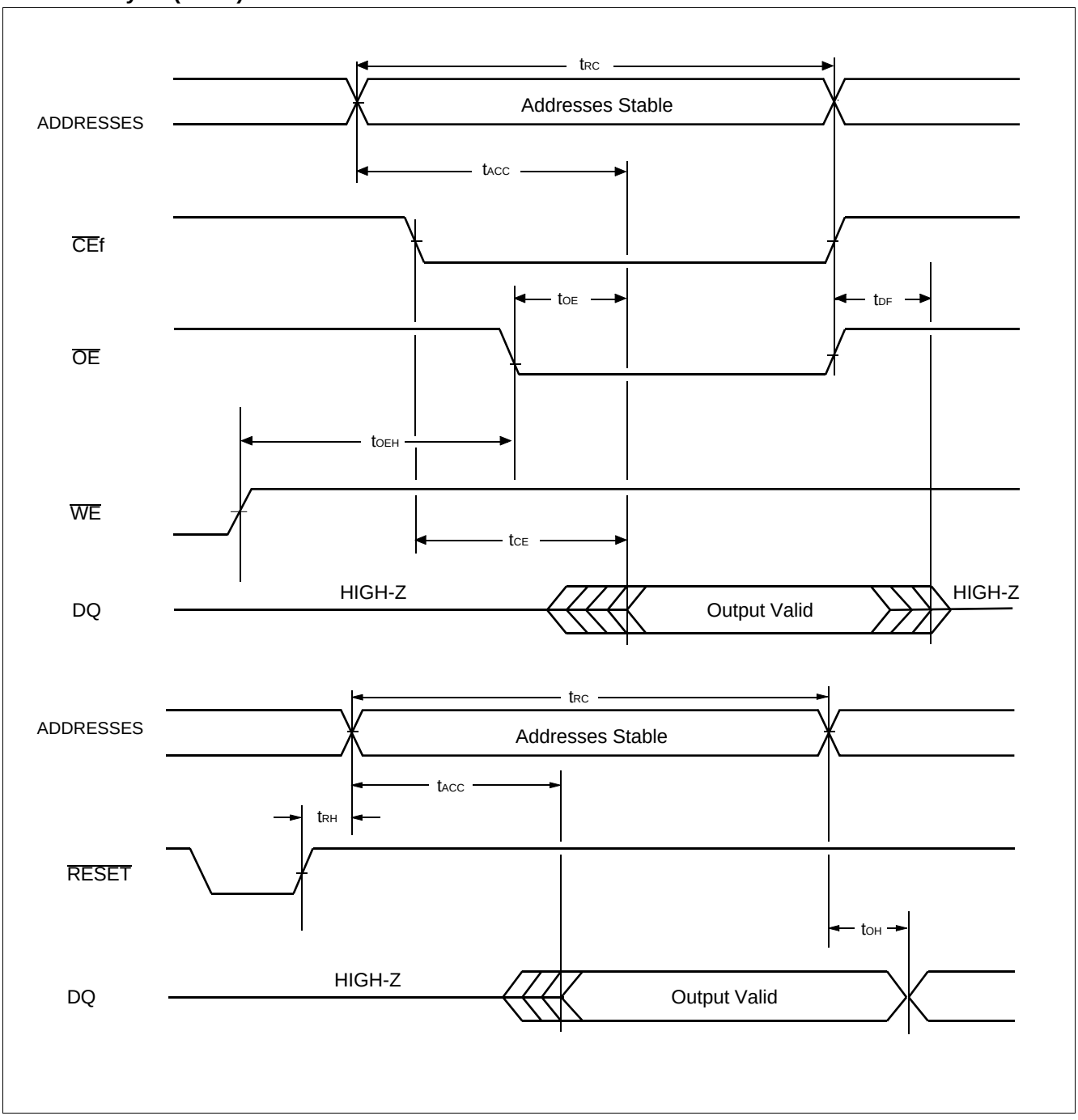



- **Read Only Operations Characteristics (Flash)**

| Parameter Symbols | | Description | Test Setup | -10 (Note) | | Unit |
|---|---|---|---|---|---|---|
| JEDEC | Standard | | | Min. | Max. | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | — | 100 | — | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | $\overline{CE}f = V_{IL}$<br>$\overline{OE} = V_{IL}$ | — | 100 | ns |
| $t_{ELQV}$ | $t_{CE}f$ | Chip Enable to Output Delay | $\overline{OE} = V_{IL}$ | — | 100 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | — | — | 40 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High-Z | — | — | 30 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High-Z | — | — | 30 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First | — | 0 | — | ns |
| — | $t_{READY}$ | $\overline{RESET}$ Pin Low to Read Mode | — | — | 20 | µs |
| — | $t_{ELFL}$<br>$t_{ELFH}$ | $\overline{CE}$ or $\overline{BYTE}$ Switching Low or High | — | — | 5 | ns |

**Note:** Test Conditions–Output Load: 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

- **Read Cycle (Flash)**



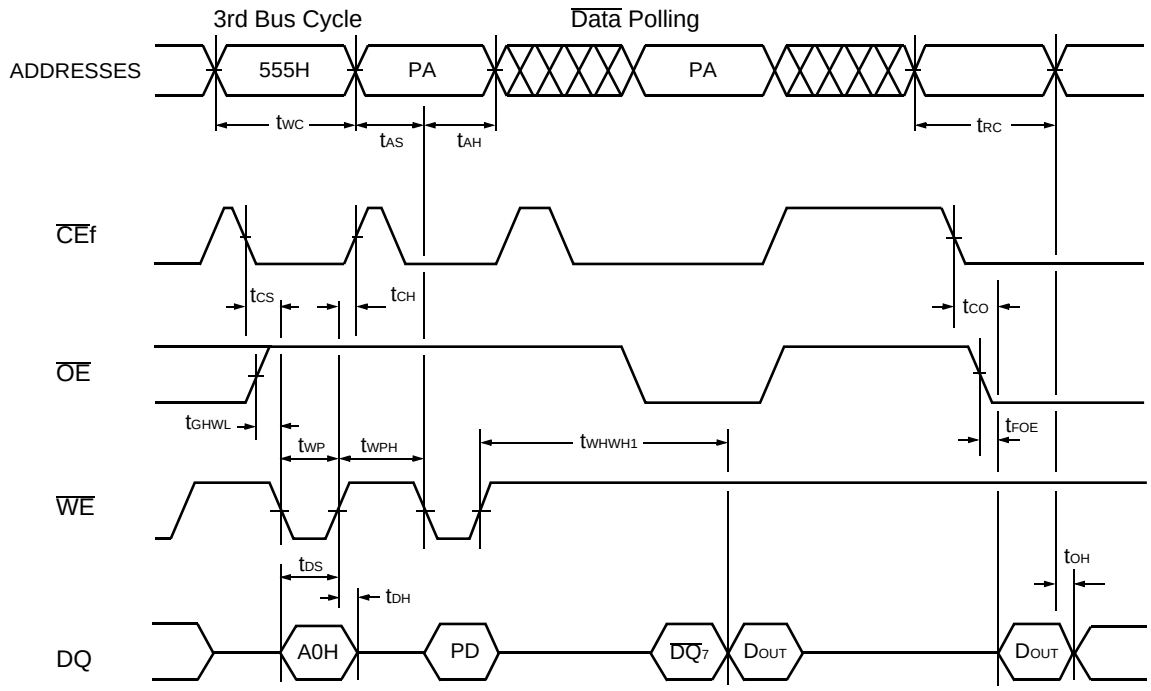
• **Erase/Program Operations (Flash)**

| Parameter Symbols | | Description | | -10 | | | Unit |
|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | Min. | Typ. | Max. | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | 100 | — | — | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time ($\overline{WE}$ to Addr.) | | 0 | — | — | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time ($\overline{CE}$f to Addr.) | | 0 | — | — | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time ($\overline{WE}$ to Addr.) | | 50 | — | — | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time ($\overline{CE}$f to Addr.) | | 50 | — | — | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | 50 | — | — | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | 0 | — | — | ns |
| — | $t_{OES}$ | Output Enable Setup Time | | 0 | — | — | ns |
| — | $t_{OEH}$ | Output Enable Hold Time | Read | 0 | — | — | ns |
| | | | Toggle and $\overline{Data}$ Polling | 10 | — | — | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f) | | 0 | — | — | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$) | | 0 | — | — | ns |
| $t_{WLEL}$ | $t_{WS}$ | $\overline{WE}$ Setup Time ($\overline{CE}$f to $\overline{WE}$) | | 0 | — | — | ns |
| $t_{ELWL}$ | $t_{CS}$ | $\overline{CE}$f Setup Time ($\overline{WE}$ to $\overline{CE}$f) | | 0 | — | — | ns |
| $t_{EHWH}$ | $t_{WH}$ | $\overline{WE}$ Hold Time ($\overline{CE}$f to $\overline{WE}$) | | 0 | — | — | ns |
| $t_{WHEH}$ | $t_{CH}$ | $\overline{CE}$f Hold Time ($\overline{WE}$ to $\overline{CE}$f) | | 0 | — | — | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | 50 | — | — | ns |
| $t_{ELEH}$ | $t_{CP}$ | $\overline{CE}$f Pulse Width | | 50 | — | — | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Pulse Width High | | 30 | — | — | ns |
| $t_{EHEL}$ | $t_{CPH}$ | $\overline{CE}$f Pulse Width High | | 30 | — | — | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Byte Programming Operation | | — | 8 | — | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 1) | | — | 1 | — | sec |
| | | | | — | — | 15 | sec |
| — | $t_{VCS}$ | $V_{CC}$f Setup Time | | 50 | — | — | µs |
| — | $t_{VLHT}$ | Voltage Transition Time (Note 2) | | 4 | — | — | µs |
| — | $t_{VIDR}$ | Rise Time to $V_{ID}$ (Note 2) | | 500 | — | — | ns |
| — | $t_{RB}$ | Recover Time from RY/$\overline{BY}$ | | 0 | — | — | ns |
| — | $t_{RP}$ | $\overline{RESET}$ Pulse Width | | 500 | — | — | ns |
| — | $t_{RH}$ | $\overline{RESET}$ Hold Time Before Read | | 200 | — | — | ns |
| — | $t_{EOE}$ | Delay Time from Embedded Output Enable | | — | — | 100 | ns |
| — | $t_{BUSY}$ | Program/Erase Valid to RY/$\overline{BY}$ Delay | | — | — | 90 | ns |
| — | $t_{FLQZ}$ | $\overline{BYTE}$ Switching Low to Output High-Z | | — | — | 30 | ns |
| — | $t_{FLQV}$ | $\overline{BYTE}$ Switching High to Output Active | | 30 | — | — | ns |

**Note** : 1. This does not include the preprogramming time.

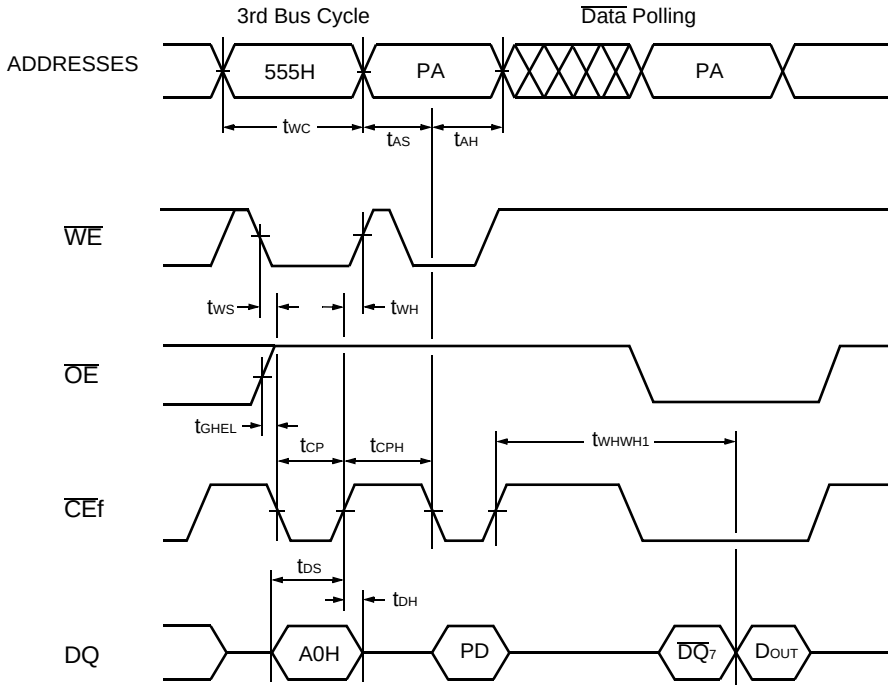
2. This timing is for Sector Protection Operation.

- **Write Cycle ($\overline{WE}$ control) (Flash)**



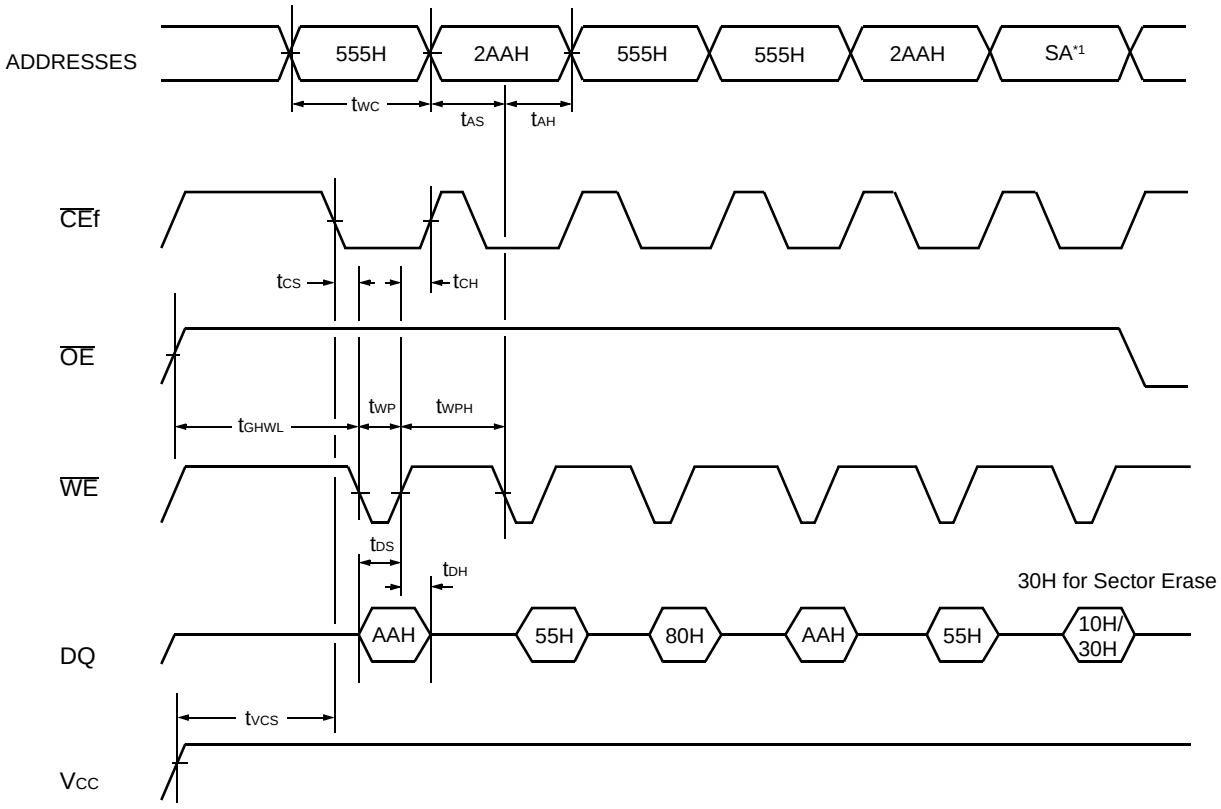

**Notes:** 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
4. $D_{OUT}$ is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence
6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

- **Write Cycle ($\overline{CE}$f control) (Flash)**



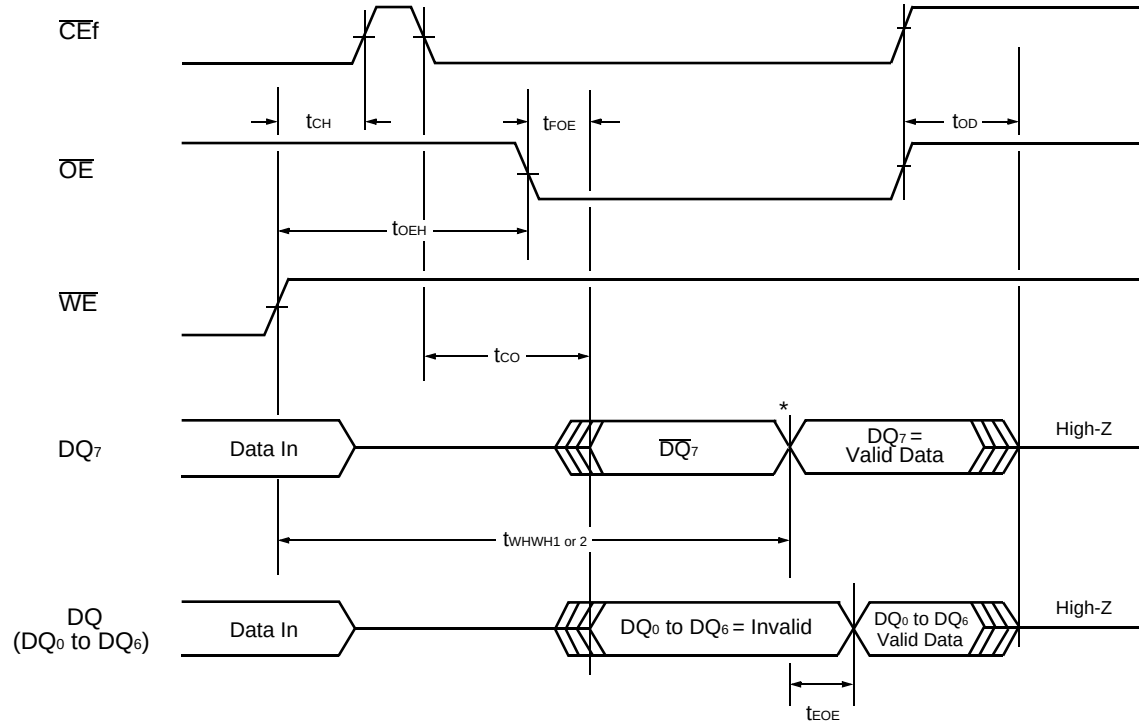

**Notes:** 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
4. $D_{OUT}$ is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence
6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

- **AC Waveforms Chip/Sector Erase Operations (Flash)**



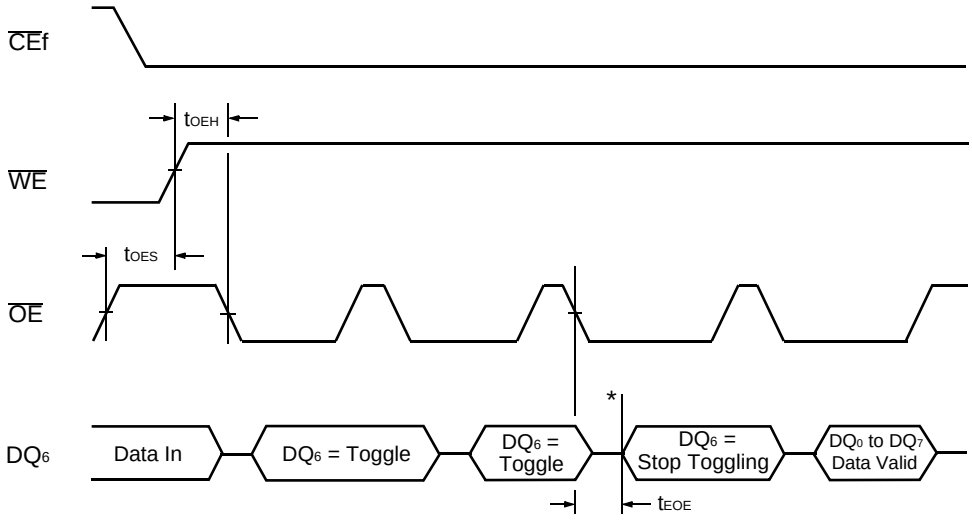

**Notes:** 1. SA is the sector address for Sector Erase. Addresses = 555H forChip Erase.
2. These waveforms are for the x16 mode. The addresses differ from x8 mode.

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



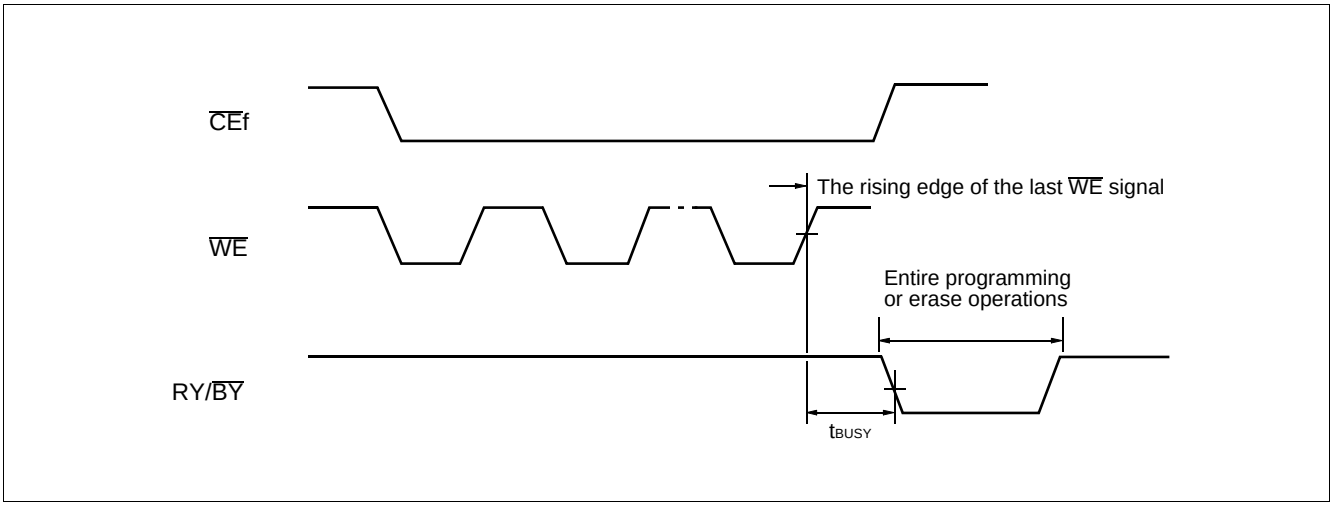

*$DQ_7$ = Valid Data (The device has completed the Embedded operation.)

- **AC Waveforms for Taggle Bit during Embedded Algorithm Operations (Flash)**

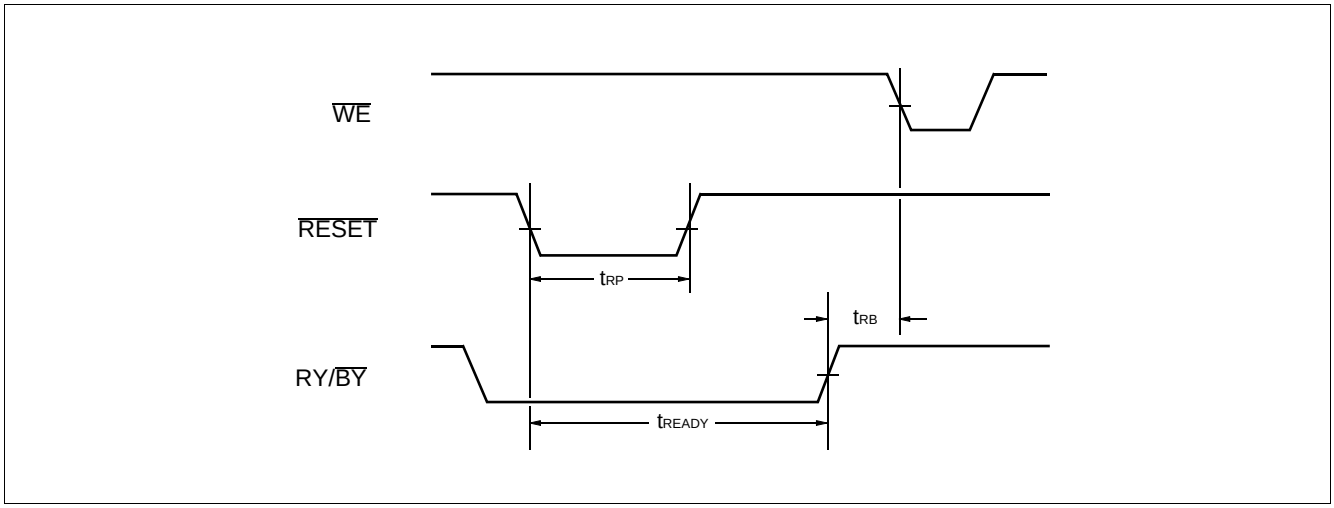



*$DQ_6$ = Stops toggling. (The device has completed the Embedded operation.)

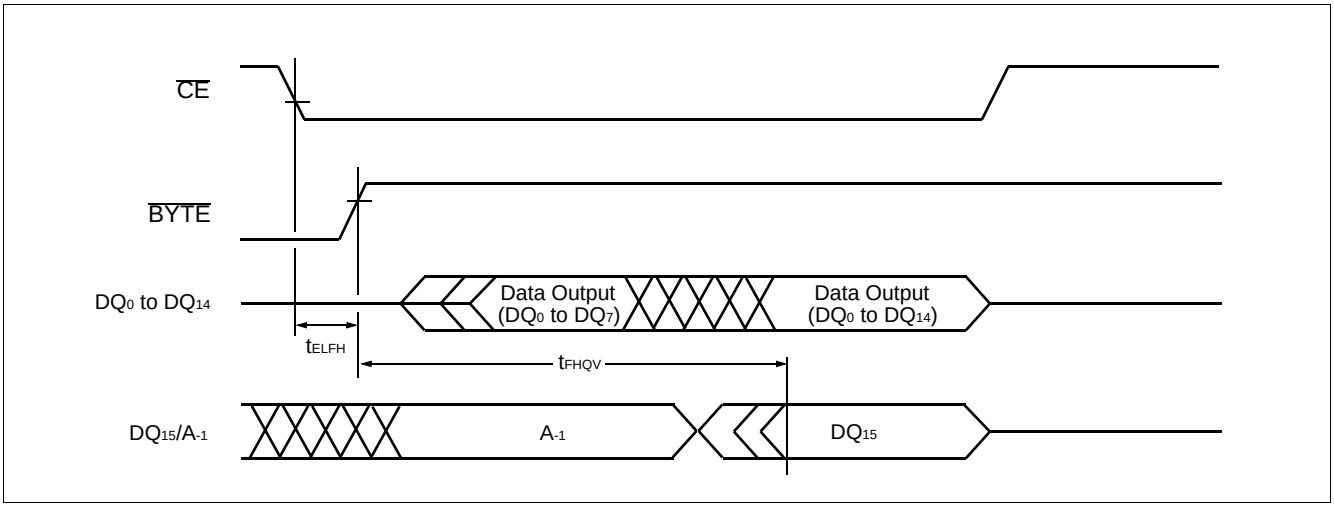
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



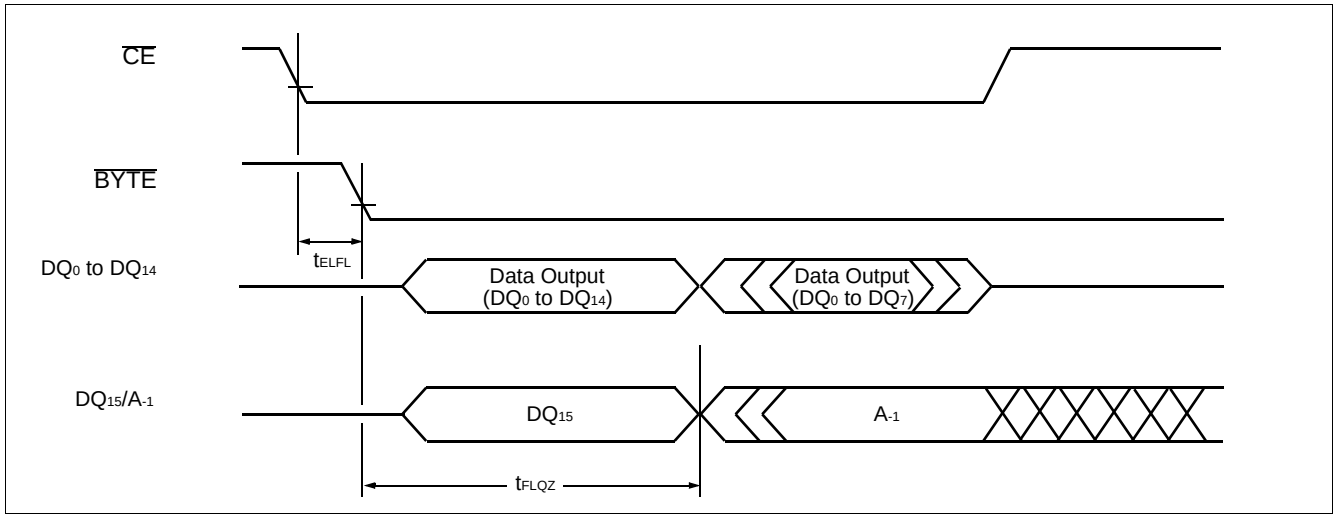

- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



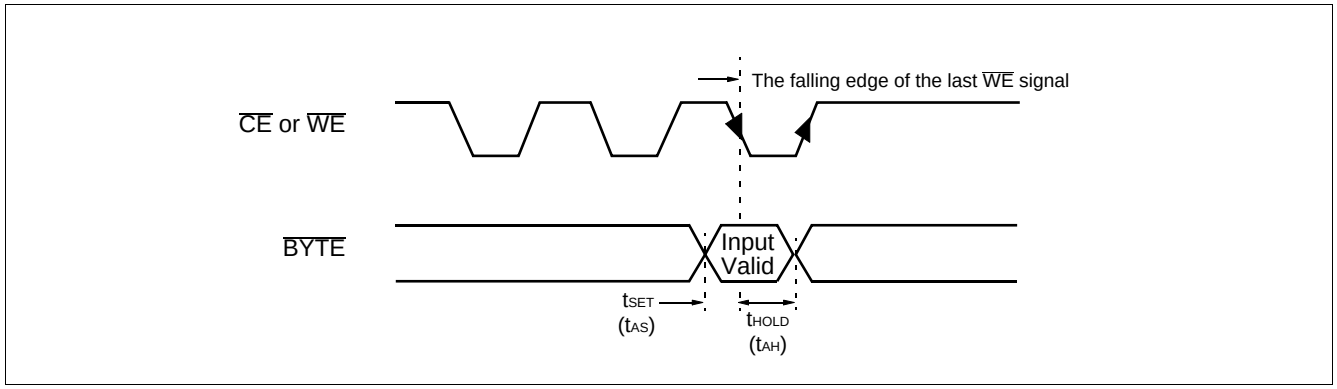

- **Timing Diagram for Word Mode Configuration (Flash)**



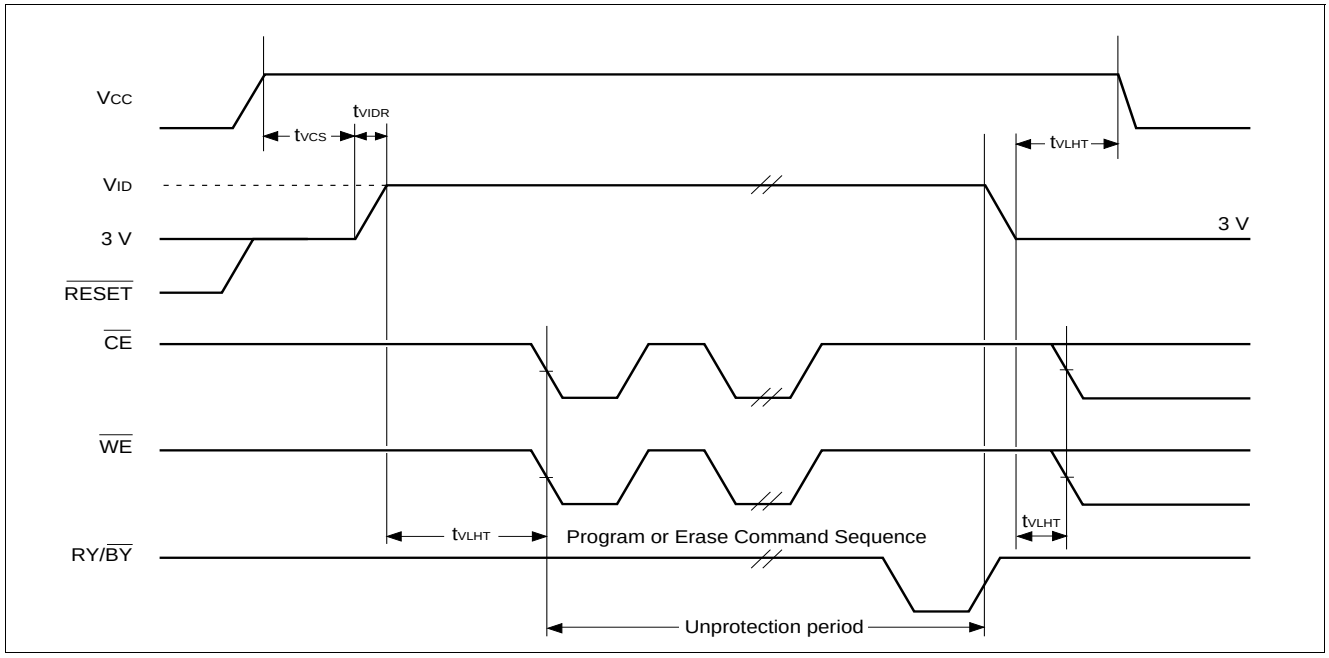
- **Timing Diagram for Byte Mode Configuration (Flash)**



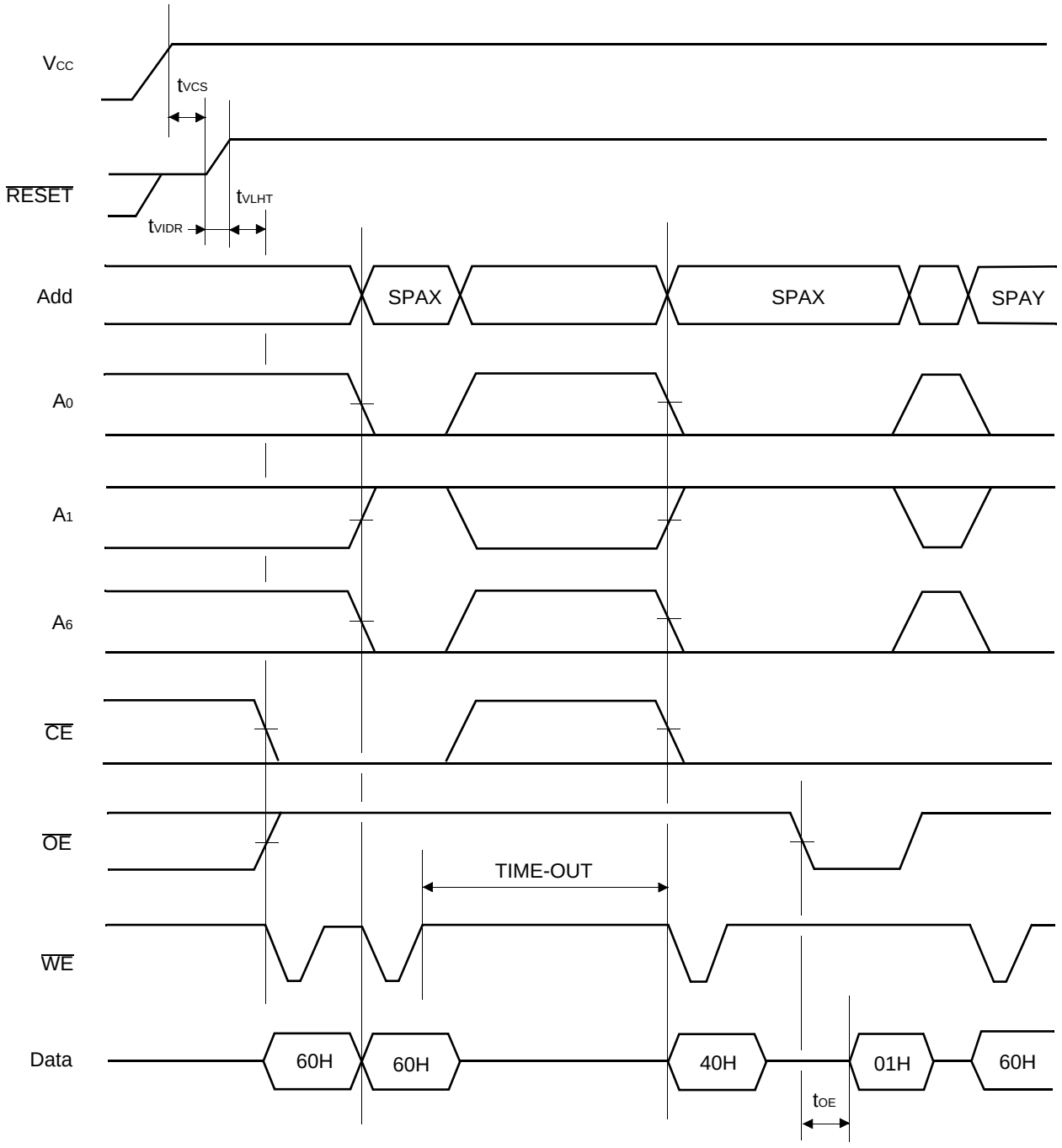

- **$\overline{BYTE}$ Timing Diagram for Write Operations (Flash)**




- **Temporary Sector Unprotection (Flash)**



- **Extended Sector Protection (Flash)**

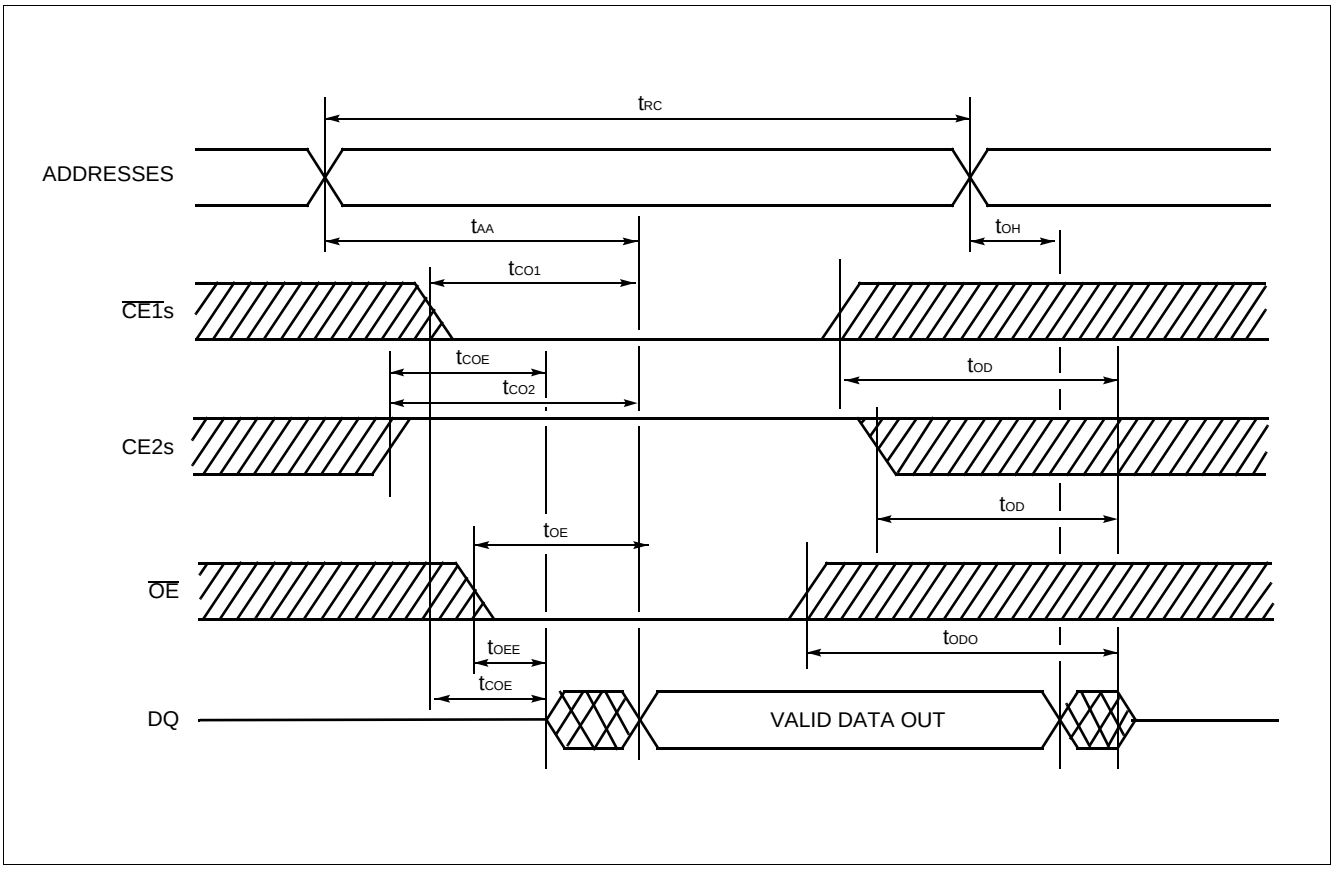



SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 150 µs (min)

- **Read Cycle (SRAM)**

| Parameter Symbol | Parameter Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 100 | — | ns |
| $t_{AA}$ | Address Access Time | — | 100 | ns |
| $t_{CO1}$ | Chip Enable ($\overline{CE1}$s) Access Time | — | 100 | ns |
| $t_{CO2}$ | Chip Enable (CE2s) Access Time | — | 100 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 50 | ns |
| $t_{COE}$ | Chip Enable ($\overline{CE1}$s Low and CE2s High) to Output Active | 5 | — | ns |
| $t_{OEE}$ | Output Enable Low to Output Active | 0 | — | ns |
| $t_{OD}$ | Chip Enable ($\overline{CE1}$s High or CE2s Low) to Output High-Z | — | 40 | ns |
| $t_{ODO}$ | Output Enable High to Output High-Z | — | 40 | ns |
| $t_{OH}$ | Output Data Hold Time | 10 | — | ns |

- **Read Cycle (Note 1) (SRAM)**

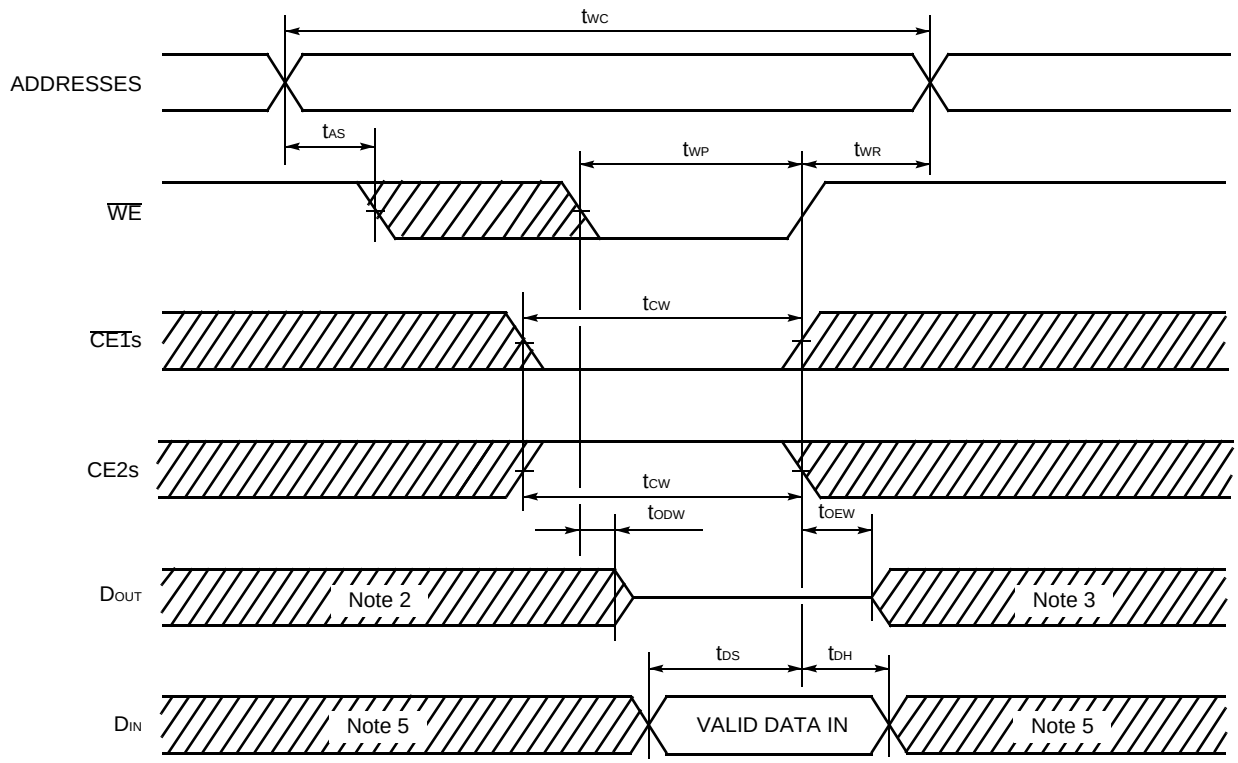



**Note:** 1. $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

| Parameter Symbol | Parameter Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | 100 | — | ns |
| $t_{WP}$ | Write Pulse Width | 60 | — | ns |
| $t_{CW}$ | Chip Enable to End of Write | 80 | — | ns |
| $t_{AS}$ | Address Setup Time | 0 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | ns |
| $t_{ODW}$ | $\overline{WE}$ Low to Output High-Z | — | 40 | ns |
| $t_{OEW}$ | $\overline{WE}$ High to Output Active | 0 | — | ns |
| $t_{DS}$ | Data Setup Time | 40 | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | ns |

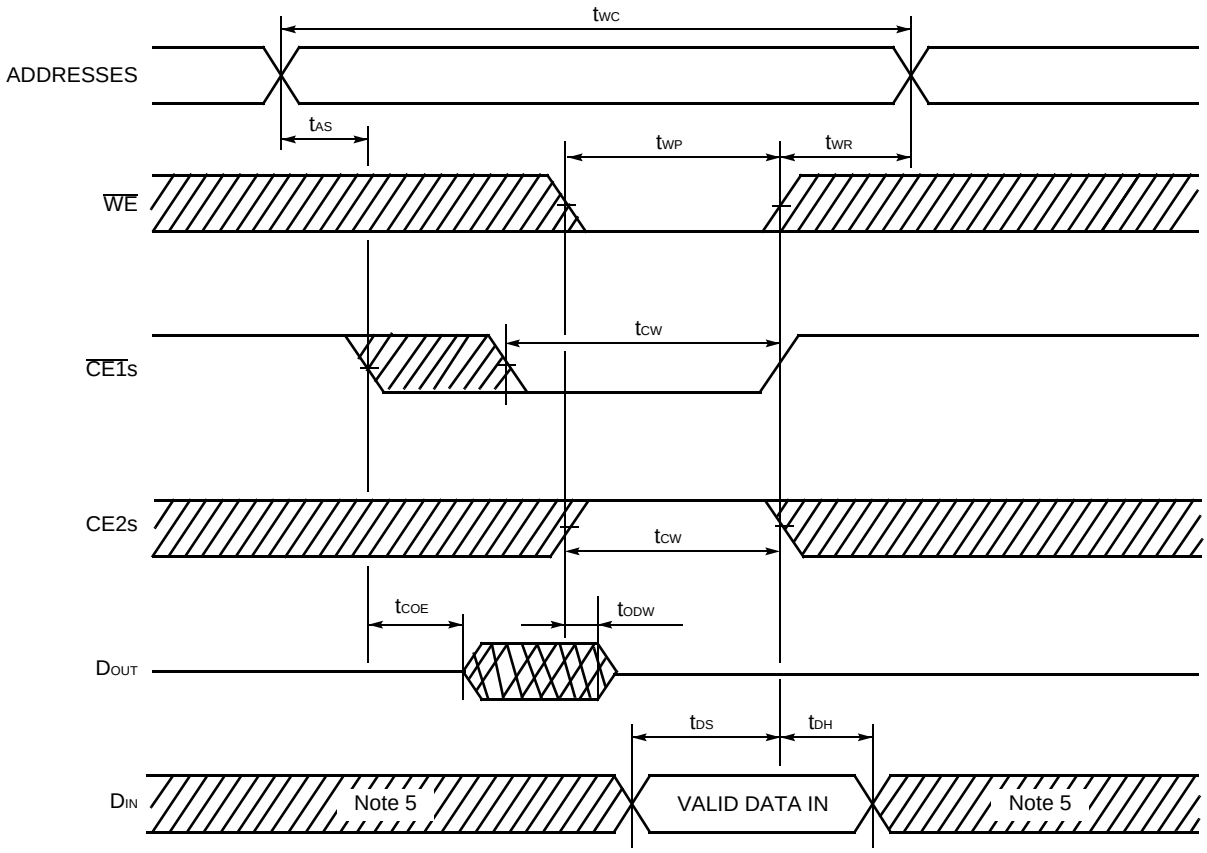
- **Write Cycle (Note 4) ($\overline{WE}$ control) (SRAM)**




**Notes:** 2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

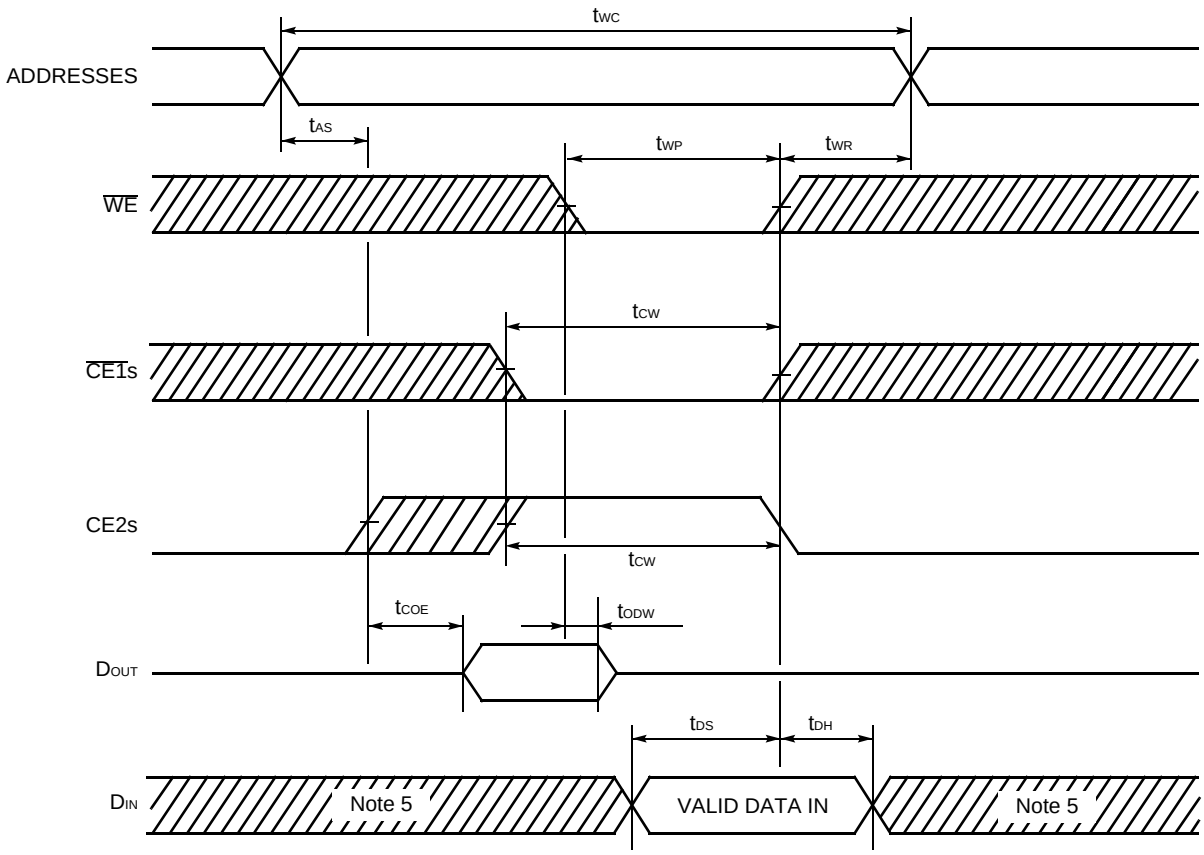
- **Write Cycle (Note 4) ($\overline{CE1}$s control) (SRAM)**




**Notes:** 2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 4) (CE2s Control) (SRAM)**




**Notes:** 2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

## ■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

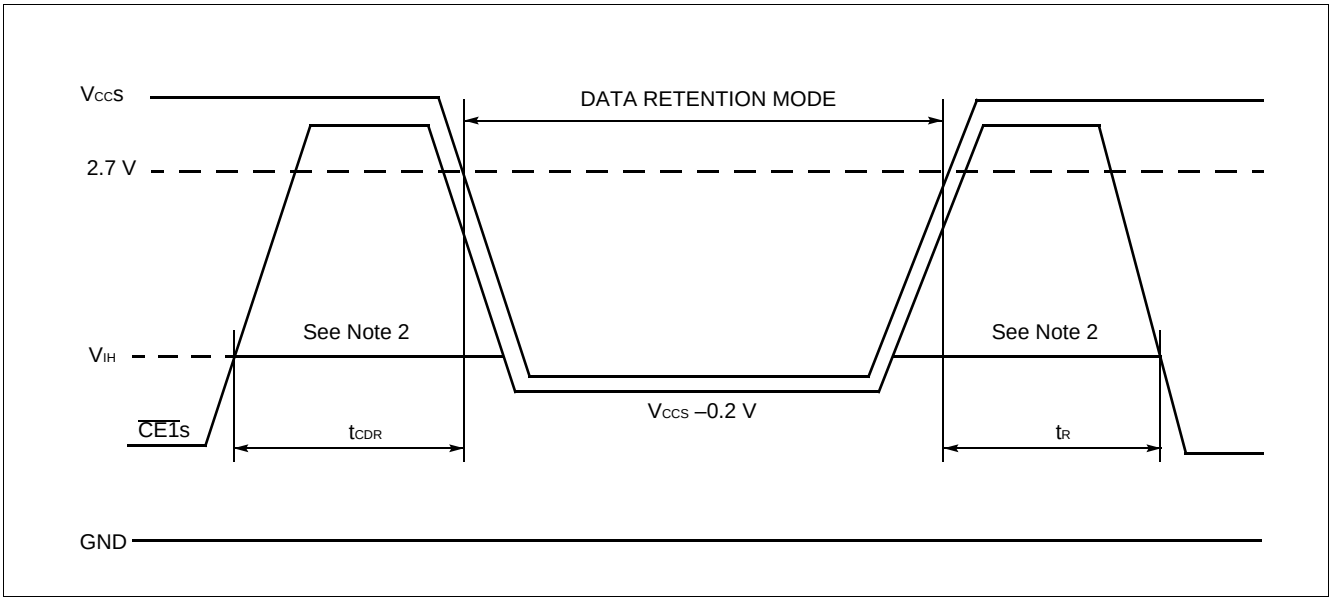
| Parameter | Limits | | | Unit | Comment |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Sector Erase Time | — | 1 | 15 | sec | Excludes programming time prior to erasure |
| Byte Programming Time | — | 8 | 3,600 | µs | Excludes system-level overhead |
| Chip Programming Time | — | 12 | T.B.D | sec | Excludes system-level overhead |
| Erase/Program Cycle | 100,000 | — | — | cycles | |

## ■ DATA RETENTION CHARACTERISTICS (SRAM)

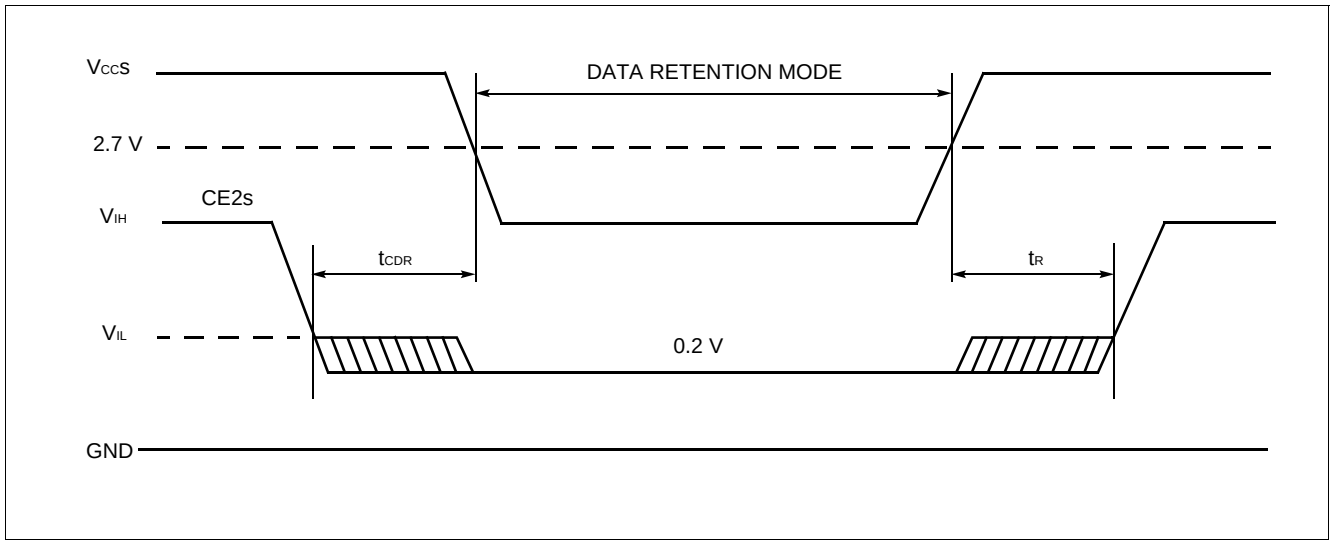
| Parameter Symbol | Parameter Description | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DH}$ | Data Retention Supply Voltage | | 2.0 | — | 3.6 | V |
| $I_{DDS2}$ | Standby Current | $V_{DH}$ = 3.0 V | — | — | 50* | µA |
| | | $V_{DH}$ = 3.6 V | — | — | 60 | µA |
| $t_{CDR}$ | Chip Deselect to Data Retention Mode Time | | 0 | — | — | ns |
| $t_R$ | Recovery Time | | 5 | — | — | ms |

* : 5 µA (Max.) at $T_A$ = –20°C to +40°C

- **$\overline{CE1}$s Controlled Data Retention Mode (Note 1)**



- **CE2s Controlled Data Retention Mode (Note 3)**




**Notes:** 1. In $\overline{CE1}$s controlled data retention mode, input level of CE2s should be fixed Vccs to Vccs-0.2V or Vss to 0.2V during data retention mode. Other input and input/output pins can be used between -0.3V to Vccs+0.3V.

2. When $\overline{CE1}$s is operating at the $V_{IH}$ min. level (2.2 V), the standby current is given by $I_{SB1}$s during the transition of $V_{CC}$s from 3.6 to 2.2 V.
3. In CE2s controlled data retention mode, input and input/output pins can be used between between -0.3V to Vccs+0.3V.

## ■ PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | T.B.D | T.B.D | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | T.B.D | T.B.D | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | T.B.D | T.B.D | pF |

**Note:** Test conditions $T_A$ = 25°C, f = 1.0 MHz

## ■ HANDRING OF PACKAGE

Please handle this package carefully since the sides of packages are right angle.

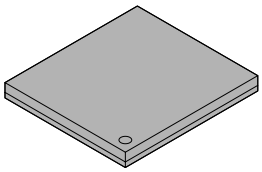
## ■ CAUTION

1.)The high voltage (VID) can not apply to address pins and control pins except $\overline{RESET}$. Therefore, it can not use autoselect and sector protect function by applying the high voltage (VID) to specific pins.

2.)For the sector protection, since the high voltage (VID) can be applied to the $\overline{RESET}$, it can be protected the sector useing "Extended sector protect" command.

## ■ PACKAGE

48-pin plastic FBGA

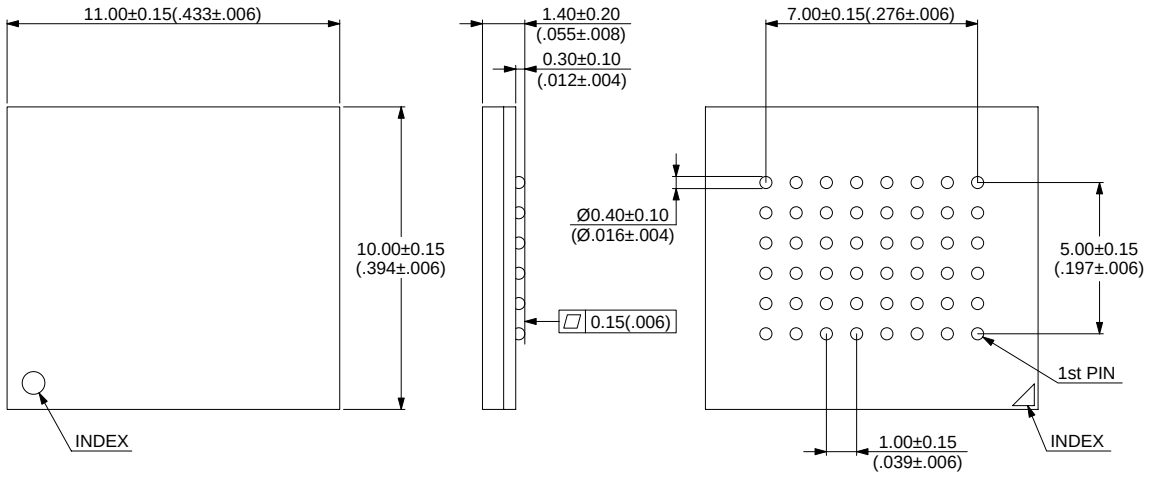


(BGA-48P-M06)

## ■ PACKAGE DIMENSIONS

48-pin plastic BGA
(BGA-48P-M06)

Note: The actual shape of coners may differ from the dimension.






Dimension in mm (inches).

# FUJITSU LIMITED

*For further information please contact:*

**Japan**
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-8588, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

*http://www.fujitsu.co.jp/*

**North and South America**
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
*Mon. - Fri.: 7 am - 5 pm (PST)*
Tel: (800) 866-8608
Fax: (408) 922-9179

*http://www.fujitsumicro.com/*

**Europe**
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

*http://www.fujitsu-ede.com/*

**Asia Pacific**
FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

*http://www.fmap.com.sg/*

F9805




The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.