

# CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

## DESCRIPTION

The Fujitsu MB8417 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

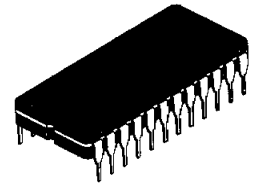
The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

The MB8417 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Chip Select  $\bar{E}^*$  permits the fast access time. The MB8417 is packaged in an industry standard 24-pin dual in-line package or 32-pin leadless chip carrier.

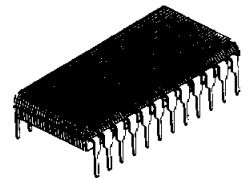
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## FEATURES

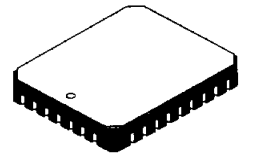
- Extended temperature range:  
MB8417-20:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
MB8417-20L:  $-40^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$
- Organized as 2048 words by 8-bits
- Fast Access Time:  
200 ns Max. ( $\bar{E}$  Controlled)  
100 ns Max. ( $\bar{E}^*$  Controlled)
- Low Standby Power:  
MB8417-20:  $55 \mu\text{W}$   
MB8417-20L:  $5.5 \mu\text{W}$
- Completely Static Operation, no clocks required
- Single +5 Volt Power Supply
- TTL Compatible Inputs/Outputs
- Low Data Retention Voltage: 2.0V Min.
- Pin compatible with TC5516 and  $\mu\text{PD447}$



**CERDIP PACKAGE**  
**DIP-24C-C03**

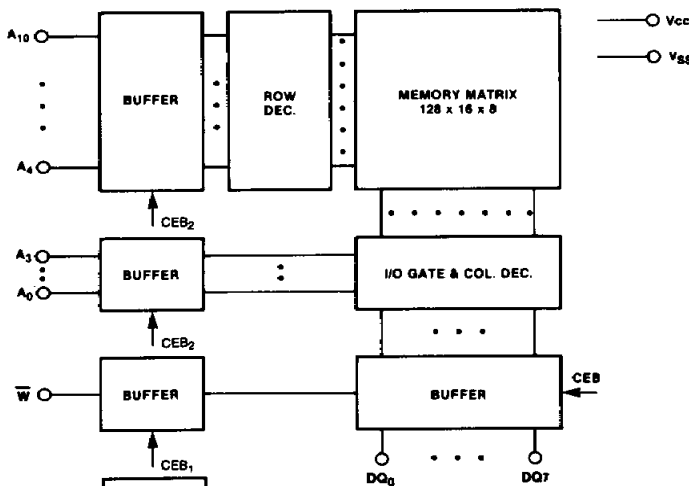


**PLASTIC PACKAGE**  
**DIP-24P-M02**



**LEADLESS CHIP CARRIER**  
**LCC-32C-A02**

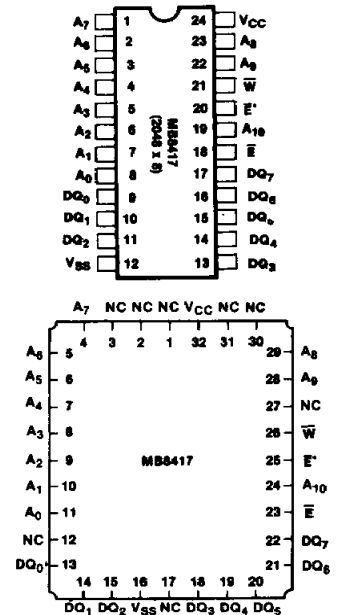
## MB8417 BLOCK DIAGRAM



## TRUTH TABLE

$\bar{E}$	$\bar{E}^*$	$\bar{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	$I_{SB}$	High-Z
L	H	X	Not Selected	$I_{CC}$	High-Z
L	L	H	Read	$I_{CC}$	$D_{OUT}$
L	L	L	Write	$I_{CC}$	$D_{IN}$

## PIN ASSIGNMENT



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit	
Storage Temperature	Ceramic	$T_{stg}$	-65	150	°C
	Plastic		-45	125	
Temperature Under Bias	$T_{bias}$	-40	85	°C	
Supply Voltage	$V_{CC}$	-0.5	8.0	V	
Input Voltage	$V_{IN}$	-0.5	$V_{CC} + 0.5$	V	
Input/Output Voltage	$V_{I/O}$	-0.5	$V_{CC} + 0.5$	V	

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

**RECOMMENDED OPERATING CONDITIONS,  $V_{SS} = GND$** 

Parameter	Symbol	MB8417			Unit	
		Min	Typ	Max		
Ambient Temperature	$T_A$	MB8417-20L	-40	—	+70	°C
		MB8417-20	-40	—	+85	
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	
Input High Voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V	

**CAPACITANCE**

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	$C_{IN}$	—	7	pF	$V_{IN} = 0V$
Input /Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O} = 0V$

**STATIC CHARACTERISTICS**

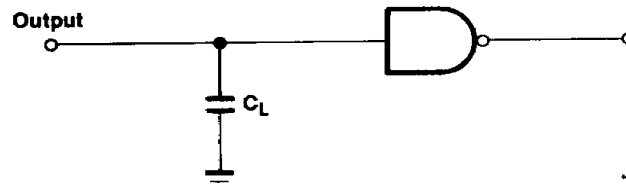
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Units
Standby Supply Current	$\bar{E} = V_{CC} - 0.2V$ to $V_{CC} + 0.2V$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	MB8417-20L	—	1	$\mu\text{A}$
		MB8417-20	—	10	
Standby Supply Current	$\bar{E} = V_{IH}$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	$I_{SB2}$	—	2	mA
Active Supply Current	$\bar{E} = V_{IL}$ $V_{IN} = V_{IL}$ or $V_{IH}$ ; $I_{OUT} = 0$	$I_{CC1}$	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	$I_{CC2}$	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to $V_{CC}$	$I_{LI}$	-1.0	1.0	$\mu\text{A}$
Output Leakage Current	$V_{I/O} = 0V$ to $V_{CC}$ $\bar{E} = V_{IH}$ or $\bar{E}^* = V_{IH}$	$I_{LO}$	-1.0	1.0	$\mu\text{A}$
Output High Voltage	$I_{OUT} = -1.0\text{ mA}$	$V_{OH}$	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0\text{ mA}$	$V_{OL}$	—	0.4	V



## AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	10 ns
Input Timing Reference Level:	0.8V to 2.2V
Output Timing Reference Level:	0.8V to 2.2V
Output Load:	† TTL Gate and $C_L = 100$ pF for all others.



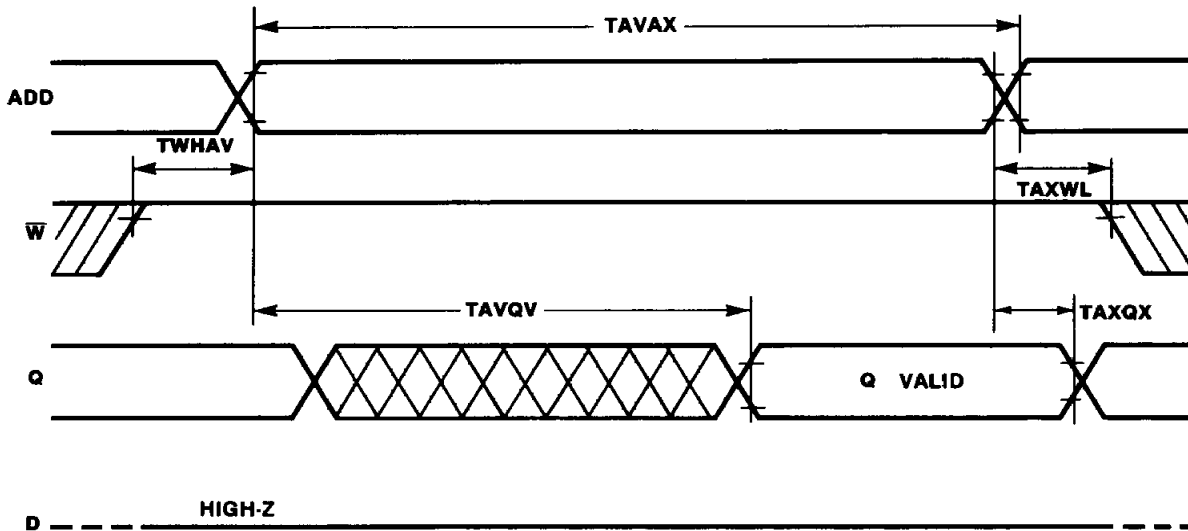
## DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAX	200	—	ns
Write Cycle Time	TAVAX	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Chip Select Access Time	TSLQV	—	100	ns
Output Hold from Address Change	TAXQX	15	—	ns
Output Low Z from $\bar{E}$ or $\bar{E}^*$	TELQX, TSLQX	15	—	ns
Output High Z from $\bar{E}$ or $\bar{E}^*$	TEHQZ, TSHQZ	—	60	ns
Output Low Z from $\bar{W}$	TWHQX	15	—	ns
Output High Z from $\bar{W}$	TWLQZ	—	60	ns
Address Set Up Time	TAVWL, TAVSL, TAVEL	0	—	ns
Read Set Up Time	TWHAV, TWHEL, TWHSL	0	—	ns
Read Hold Time	TEHWL, TAXWL, TSHWL	0	—	ns
Write Set Up Time	TWLSL, TWLEL	0	—	ns
Write Hold Time	TSHWH, TEHWH	0	—	ns
Address Valid to End of Write	TAVSH, TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Chip Selection to End of Write	TELEH*	100	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TEHAX, TWHAX, TSHAX	10	—	ns
Data Set Up Time	TDVWH, TDVEH, TDVSH	60	—	ns
Data Hold Time	TEHDX, TWHDX, TSHDX	0	—	ns

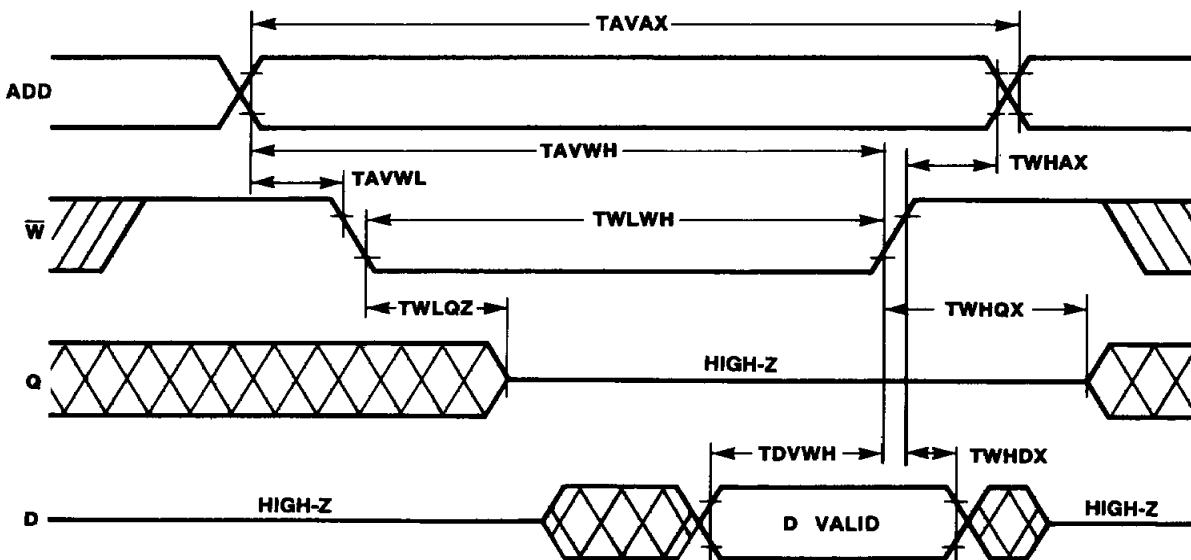
WAVEFORMS

MODE 1:  $\bar{W}$  Controlled: ( $\bar{E} = \text{Low}$ ,  $\bar{E}^* = \text{Low}$ )

Read Cycle



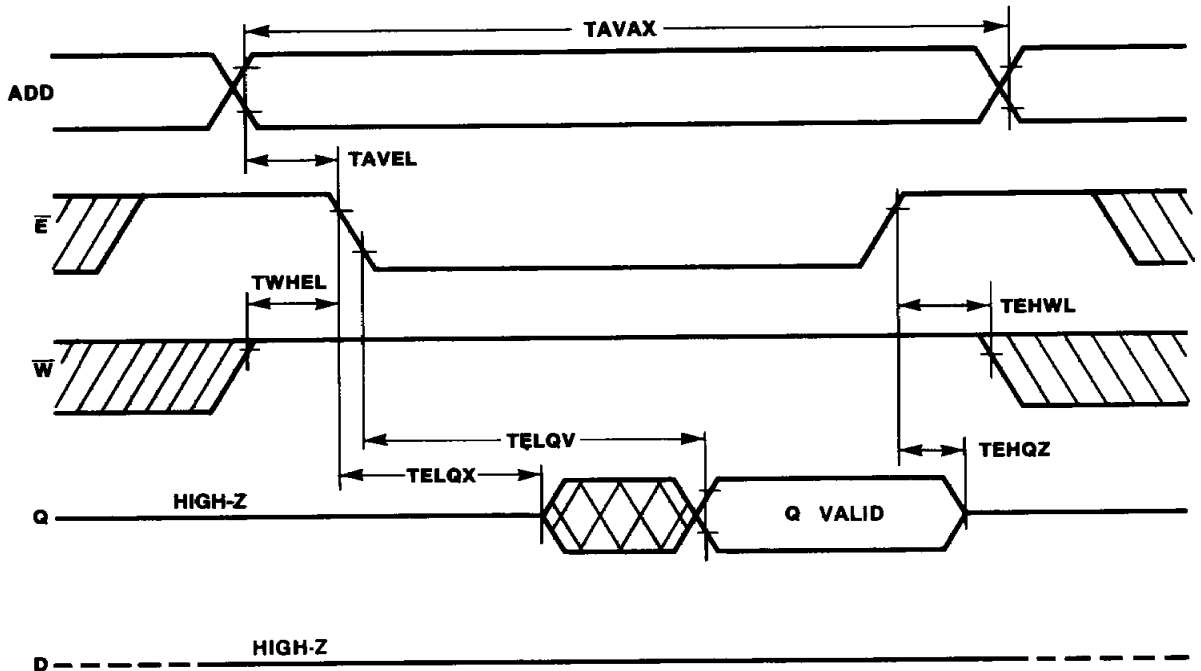
Write Cycle



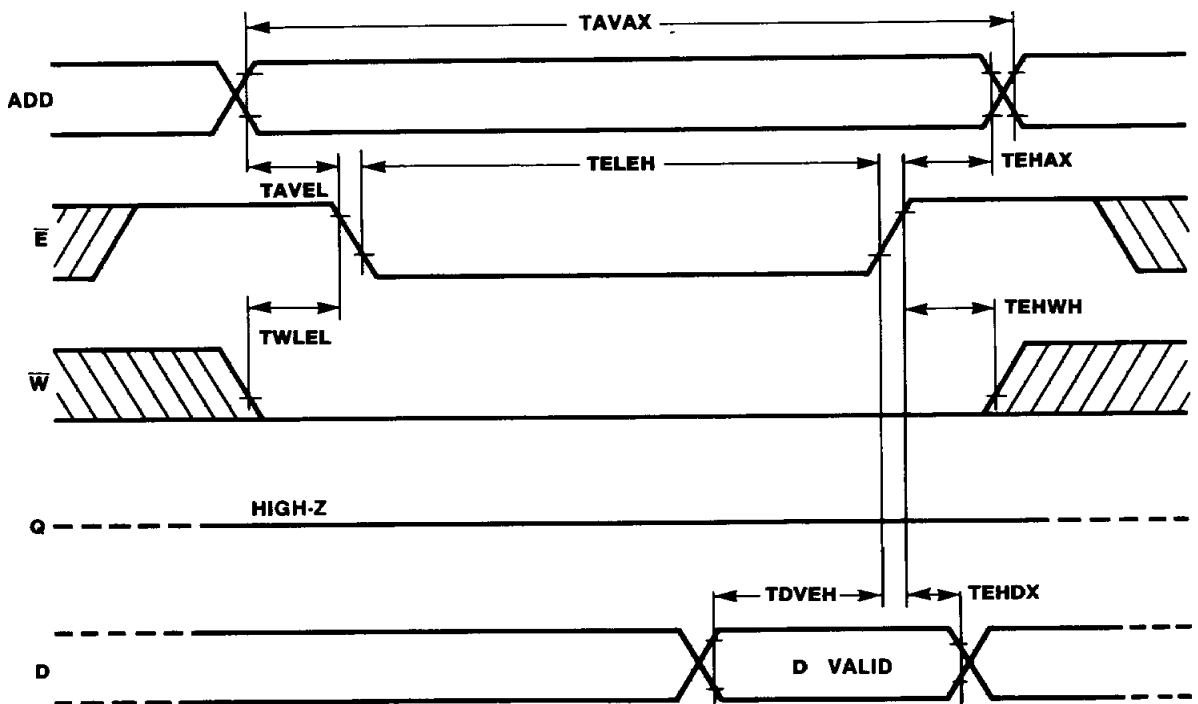
**WAVEFORMS** (Continued)

**MODE 2:  $\bar{E}$  Controlled, ( $\bar{E}^* = \text{Low}$ )**

**Read Cycle**



**Write Cycle**

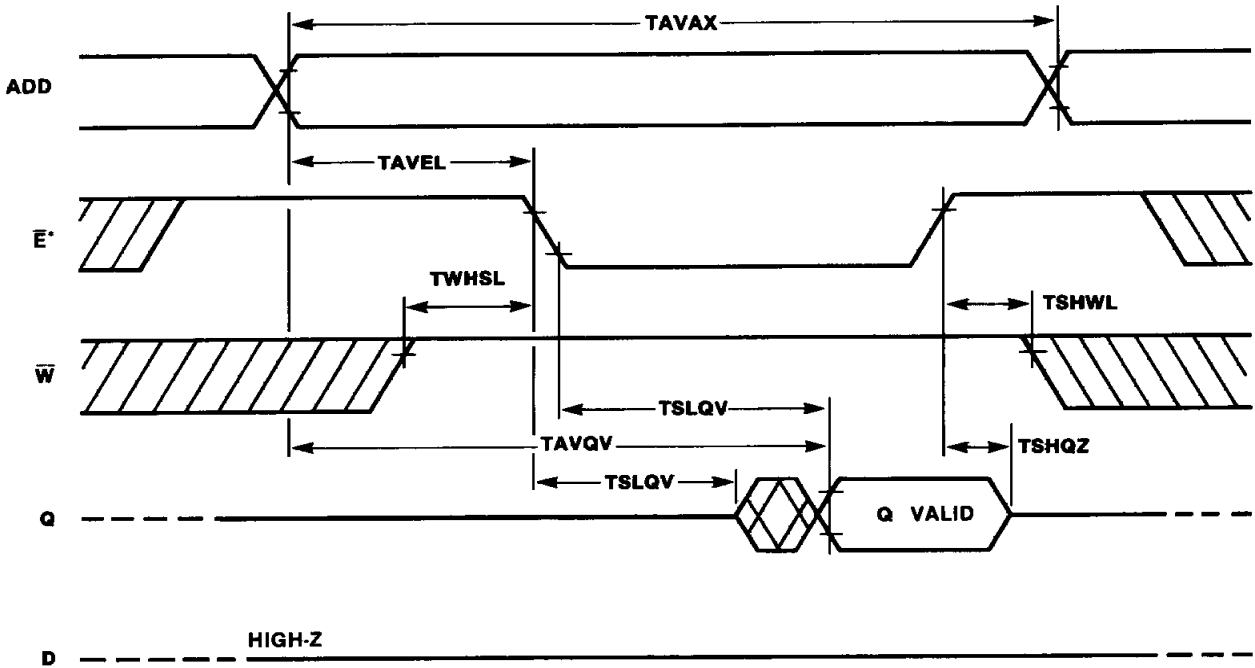


**MB8417-20 / MB8417-20 L**

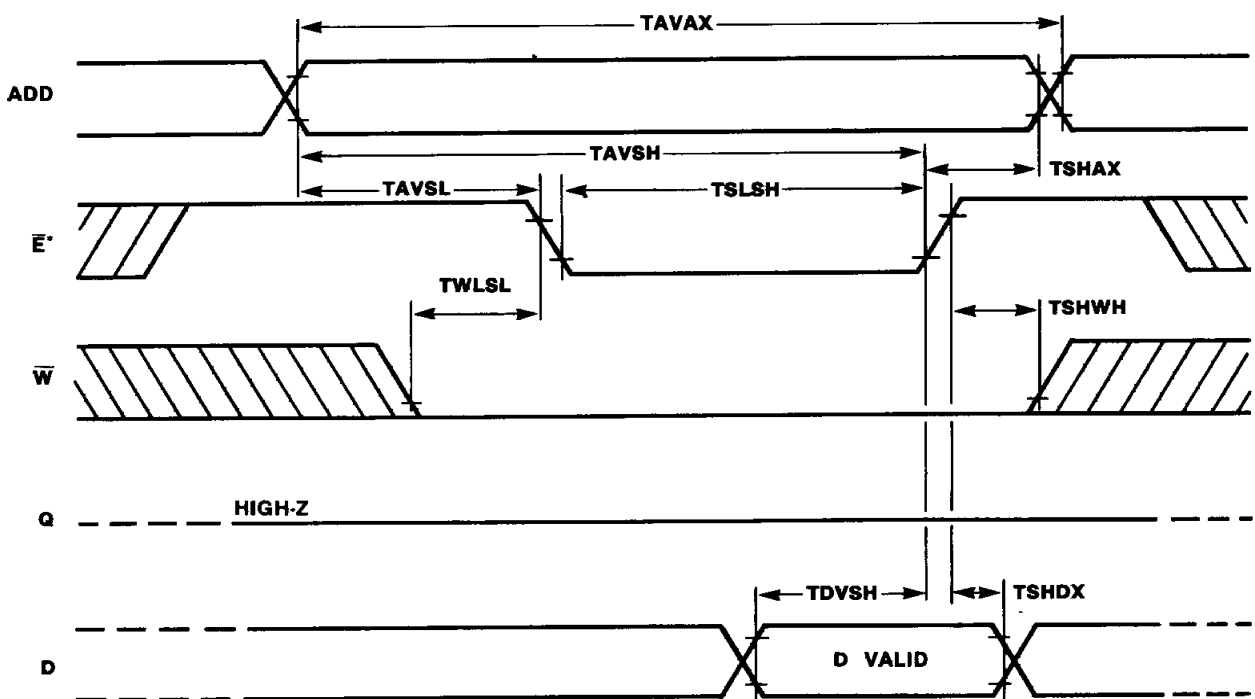
**WAVEFORMS** (Continued)

**MODE 3:  $\bar{E}^*$  Controlled, ( $\bar{E} = \text{Low}$ )**

**Read Cycle**



**Write Cycle**



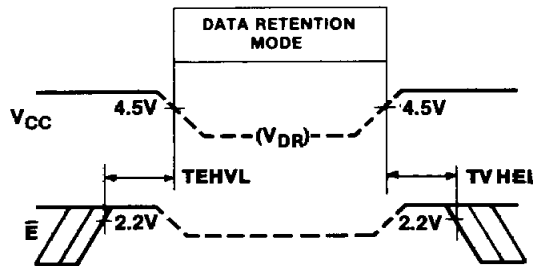
**DYNAMIC CHARACTERISTICS**

**Data Retention Characteristics, NOTES 1,2,3** (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	Min	Max	Unit
Data Retention Supply Voltage	1	VDR	2.0	5.5	V
Data Retention Supply Current	2	IDR	—	10	$\mu$ A
			—	1	$\mu$ A
Data Retention Set Up Time	3	TEHVL	0	—	ns
Recovery Time	3	TVHEL	60	—	ns

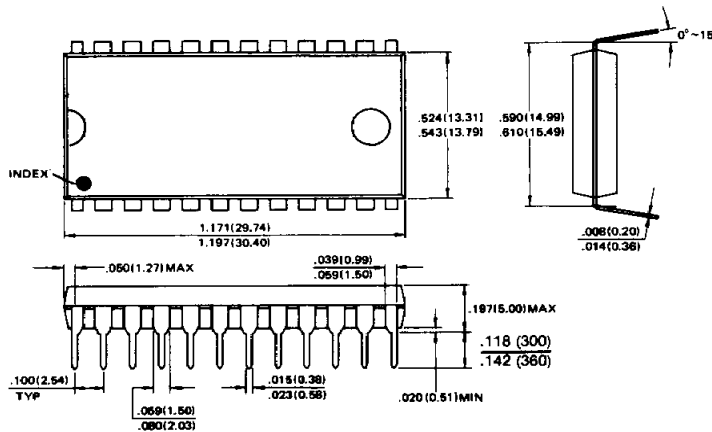
**NOTES:**

1.  $E = 2.2V$  to  $VDR + 0.3V$  when  $VDR = 2.5V$  to  $5.5V$ ,  $E = VDR \pm 0.3V$  when  $VDR = 2.0$  to  $2.5V$ .
2.  $V_{CC} = VDR = 2.0V$ ,  $E = VDR \pm 0.2V$ ,  $V_{IN} = -0.2V$  to  $VDR + 0.2V$ .
3.  $V_L = 4.5V$  on the falling transition,  $V_H = 4.5V$  on the rising transition.



**PACKAGE DIMENSIONS** Dimensions in inches (millimeters)

**24-LEAD PLASTIC DUAL IN-LINE PACKAGE  
 DIP-24P-M02**

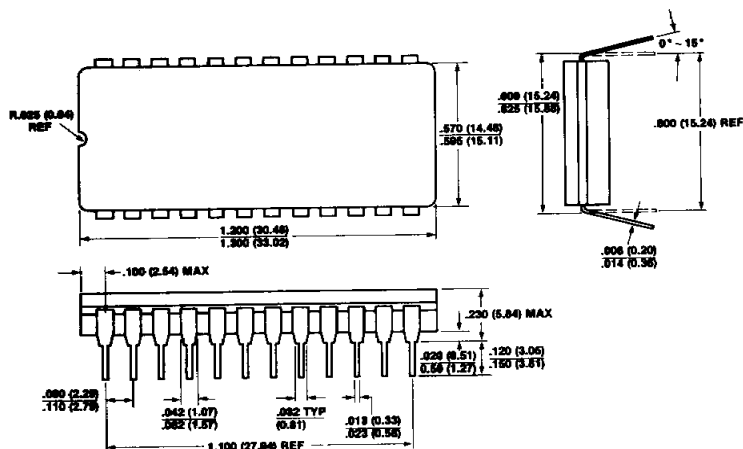


\*Symbols in extra bold type are industry standards. See IEEE STD 662 for details.

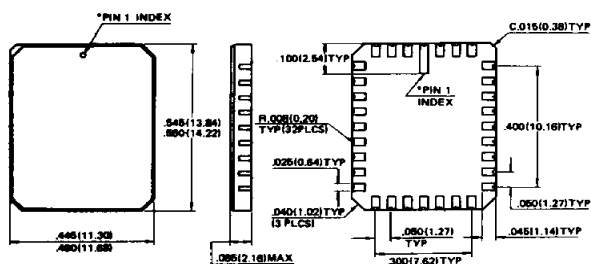


**PACKAGE DIMENSIONS** Dimensions in inches (millimeters) (Continued)

**24-LEAD CERAMIC DUAL IN-LINE PACKAGE  
DIP-24C-C03**



**LEADLESS CHIP CARRIER  
LCC-32C-A02**



\*Shape of Pin 1 Index: Subject to change without notice

