May 1990
Edition 1.0

FUJITSU

DATA SHEET

MB81C84A-25/-35
CMOS 256K-BIT HIGH-SPEED SRAM

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64K Words x 4 Bits High-Speed CMOS Static Random Access Memory

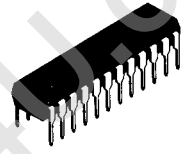
The Fujitsu MB81C84A is a 65,536 words x 4 bits static random access memory fabricated with CMOS silicon gate process technology. The MB81C84A uses NMOS cells and CMOS peripherals and is housed in 300 mil plastic DIP and SOJ packages.

The MB81C84A uses fully static circuitry and, therefore, requires no clocks or refreshes to operate. It is compatible with TTL logic and requires a single +5 V supply.

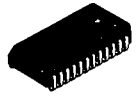
It is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required.

- Organization: 65,536 words x 4 bits
- Static operation: no clocks or refresh required
- Access time: 25 ns max. (MB81C84A-25)
  35 ns max. (MB81C84A-35)
- Single +5 V power supply ±10% tolerance with low current drain
  100 mA max. (Active operation)
  15 mA max. (Standby operation, TTL level)
  30 mA max. (Standby operation, CMOS level)
- Common data inputs and outputs
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- Three-state outputs with OR-tie capacity
- Electrostatic protection for all inputs and outputs
- Standard 24-pin Plastic Packages:
  Skinny DIP (300 mil) MB81C84A-xxPSK
  SOJ (300 mil) MB81C84A-xxPJ

PRELIMINARY

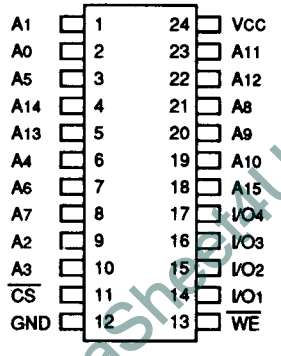


PLASTIC PACKAGE
DIP-24P-M03



PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT
TOP VIEW



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.0 to +7.0	V
Output Voltage on any pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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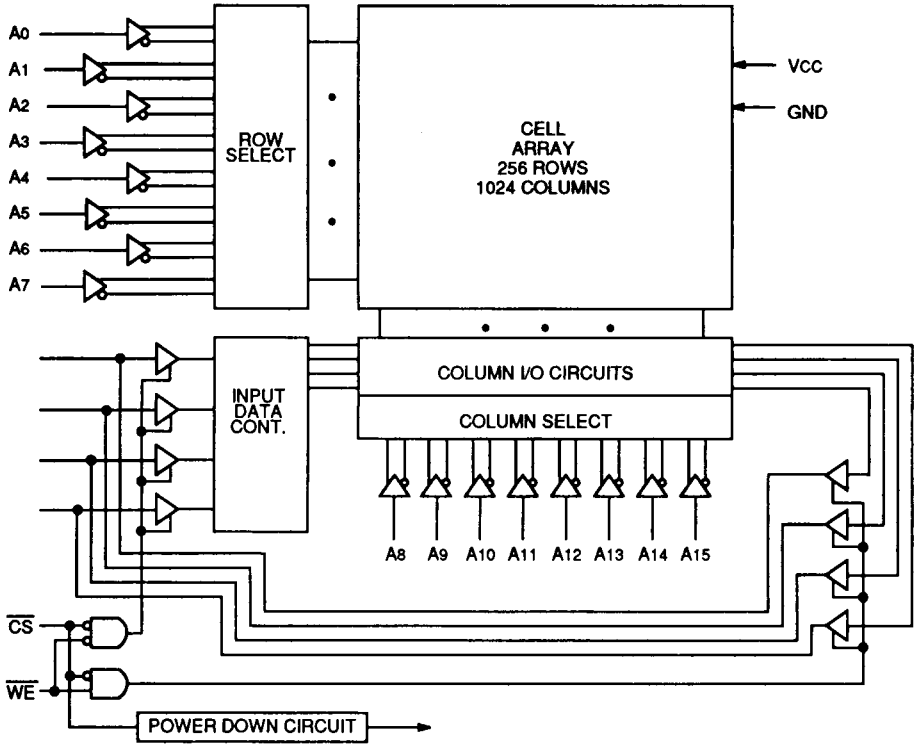
Fig. 1 – MB81C84A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	DIN	Active
L	H	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V\overline{CS}$ = 0 V)	$C\overline{CS}$		8	pF
Output Capacitance (VOUT = 0 V)	COUT		8	pF

PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A0 to A15	Address Input	$\overline{WE}$	Write Enable
I/O1 to I/O4	Data Inputs/Data Outputs	VCC	Power Supply (5V±10%)
$\overline{CS}$	Chip Select	GND	Ground

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceed 2m/sec.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	VIN = 0V to VCC	ILI	−10		10	µA
Output Leakage Current	$\overline{CS}$ = VIH, VOUT = 0V to 4.5V	ILO	−50		50	µA
Power Supply Current	$\overline{CS}$ = VIL, VIN = VIH or VIL, IOUT = 0mA, Cycle = Min.	ICC			100	mA
Standby Supply Current	$\overline{CS}$≥VCC−0.2V VIN≥VCC−0.2V or VIN≤0.2V	ISB1			15	mA
	$\overline{CS}$ = VIH, VIN = VIH or VIL	ISB2			30	mA
Peak Power on Current *1	VCC = 0V to VCC Min., $\overline{CS}$ = Lower of VCC or VIH Min.	IPO			40	mA
Input High Voltage		VIH	2.2		6.0	V
Input Low Voltage		VIL	−0.5 *2		0.8	V
Output High Voltage	IOH = −4mA	VOH	2.4			V
Output Low Voltage	IOL = 8mA	VOL			0.4	V

*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 −2.0 V Min. for pulse width less than 10 ns.

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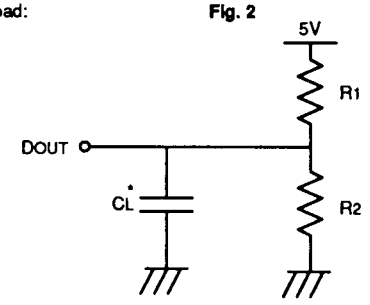
AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 2 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: VIL = 0.8, VIH = 2.2 V
  Output: VOL = 0.8, VOH = 2.2 V
- Output Load: **Fig. 2**



*Including Scope and Jig capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except tLZ, tHZ, tOW and tWZ
Load II	480Ω	255Ω	5 pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS

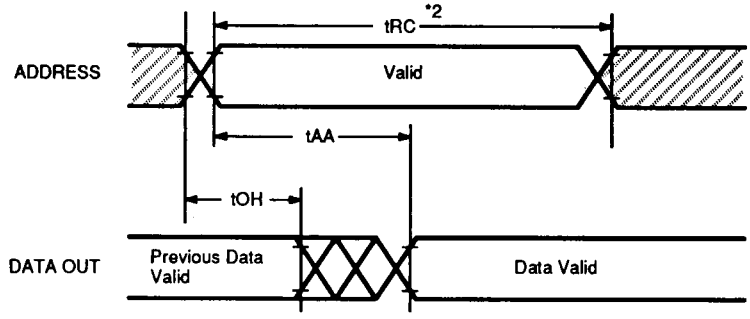
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C84A-25		MB81C84A-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2 *3	tRC	25		35		ns
Address Access Time	tAA		25		35	ns
Chip Select Access Time *4	tACS		25		35	ns
Output Hold from Address Change	tOH	3		3		ns
Chip Selection to Output in Low-Z	tLZ	3		3		ns
Chip Deselect to Output in High-Z	tHZ	0	15	0	20	ns
Chip Selection to Power Up Time	tPU	0		0		ns
Chip Selection to Power Down Time	tPD		25		35	ns

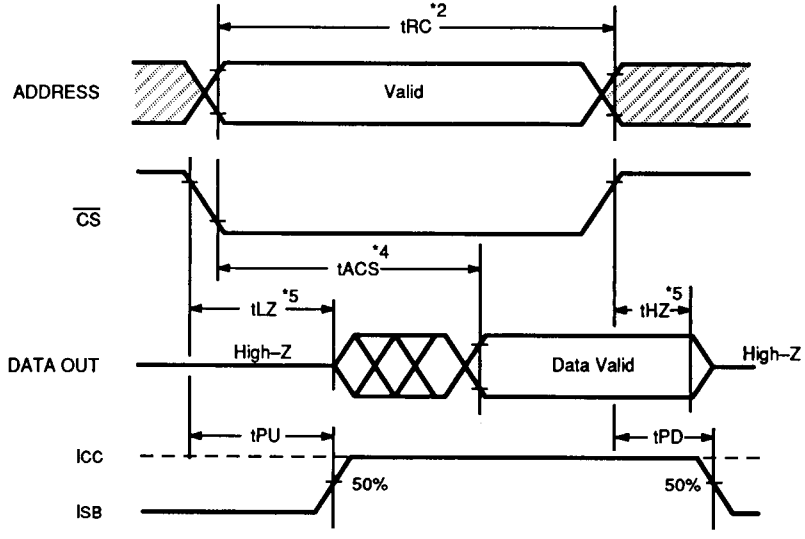
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



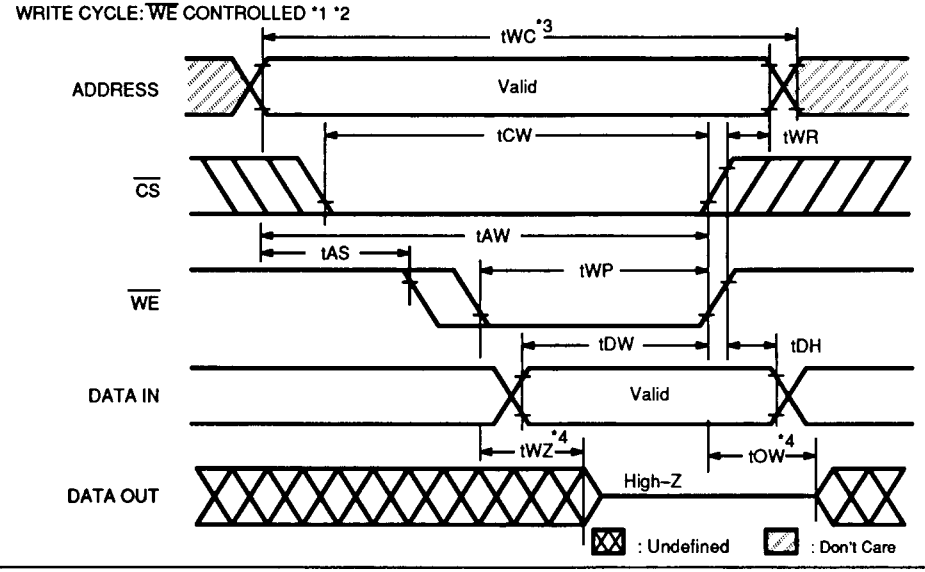
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C84A-25		MB81C84A-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time	tWC	25		35		ns
Address Valid to End of Write	tAW	20		30		ns
Chip Selection to End of Write	tCW	20		30		ns
Data Valid to End of Write	tDW	8		12		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	18		28		ns
Write Recovery Time	tWR	1		1		ns
Address Setup Time	tAS	0		0		ns
Output Active from End of Write	tOW	3		3		ns
Write Enable to Output in High-Z	tWZ	0	9	0	15	ns

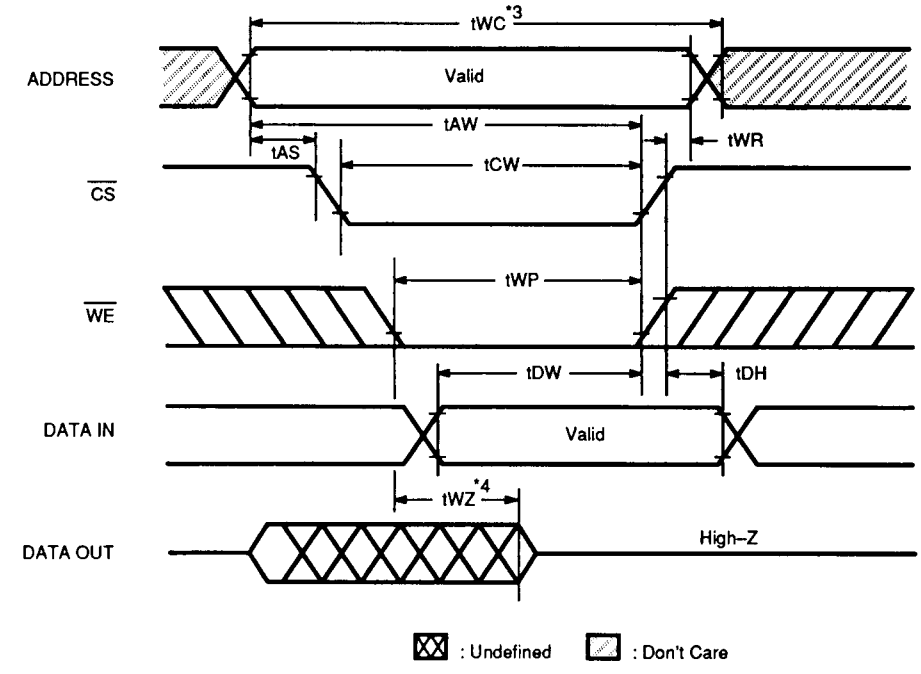
WRITE CYCLE TIMING DIAGRAM



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

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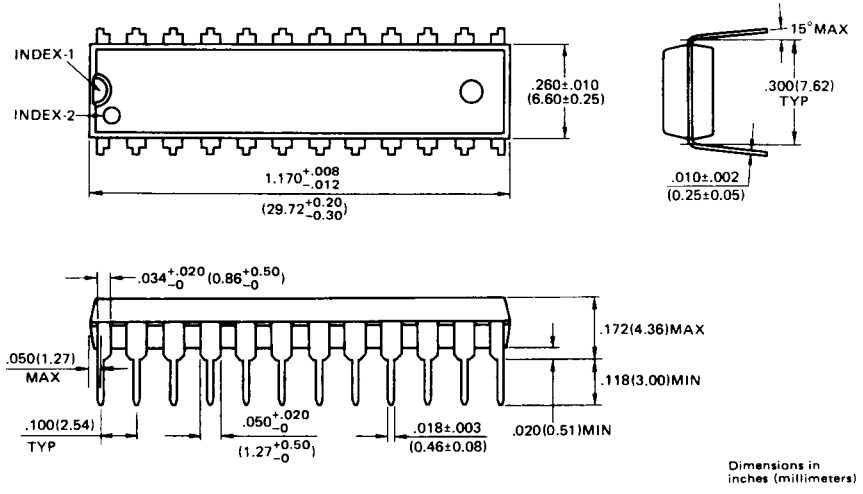
PACKAGE DIMENSIONS

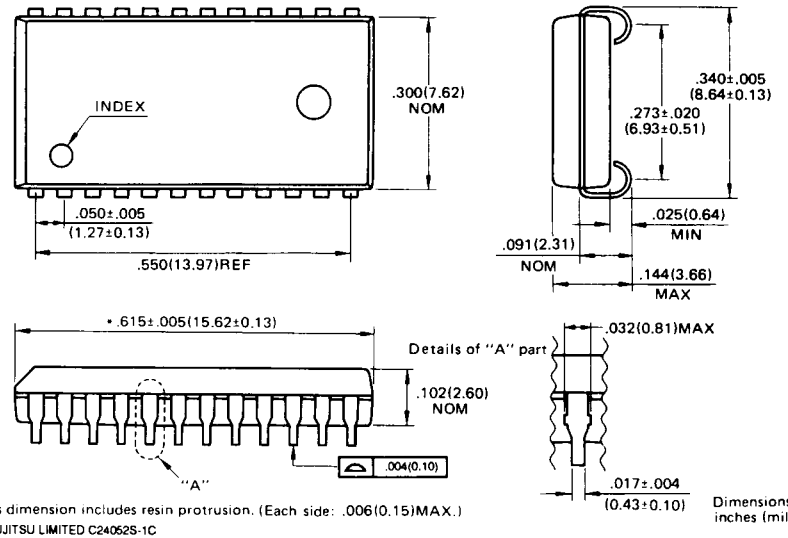
24-LEAD PLASTIC SKINNY DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

Dimensions in inches (millimeters)