



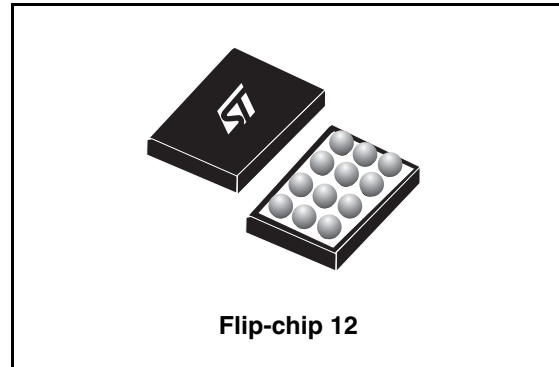
STG4260

Low voltage 0.5 Ω dual SPDT switch with break-before-make feature and 15 kV ESD protection

Preliminary Data

Features

- Wide operating voltage range:
 V_{CC} (OPR) = 1.65 to 4.8 V
- Low power dissipation:
 I_{CC} = 0.2 μ A (max.) at T_A = 85 °C
- Low "ON" resistance:
 - R_{ON} = 0.75 Ω (T_A = 25 °C) at V_{CC} = 2.25 V
 - R_{ON} = 0.50 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
 - R_{ON} = 0.40 Ω (T_A = 25 °C) at V_{CC} = 4.3 V
- Separate supply voltage for switch and control pin
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested on common pin (D pin):
 - 15 kV IEC-61000-4-2 ESD, contact discharge
 - 8 kV HBM JESD22 A114-B Class II
- ESD performance tested on S1 and S2 pin:
 - 8 kV IEC-61000-4-2 ESD, contact discharge
- ESD performance test on all other pins:
 - 4 kV HBM (JESD22 A114-B Class II)
 - 400 V machine model (JESD22 A115-A)
 - 1500 V charged-device model (JESD22 C101)



Description

The STG4260 is a high -speed CMOS low voltage dual analog SPDT (single pole dual throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65 V to 4.8 V, making this device ideal for portable applications. It offers low ON-resistance (0.40 Ω typ.) at V_{CC} = 4.3 V. The SEL inputs are provided to control the switches.

The switch S1 is ON (connected to common port D) when the SEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common Port D) when the SEL input is held low and OFF (high impedance state exist between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Applications

- Mobile phones

Table 1. Device summary

Order code	Package	Packing
STG4260BJR	Flip-chip 12	Tape and reel

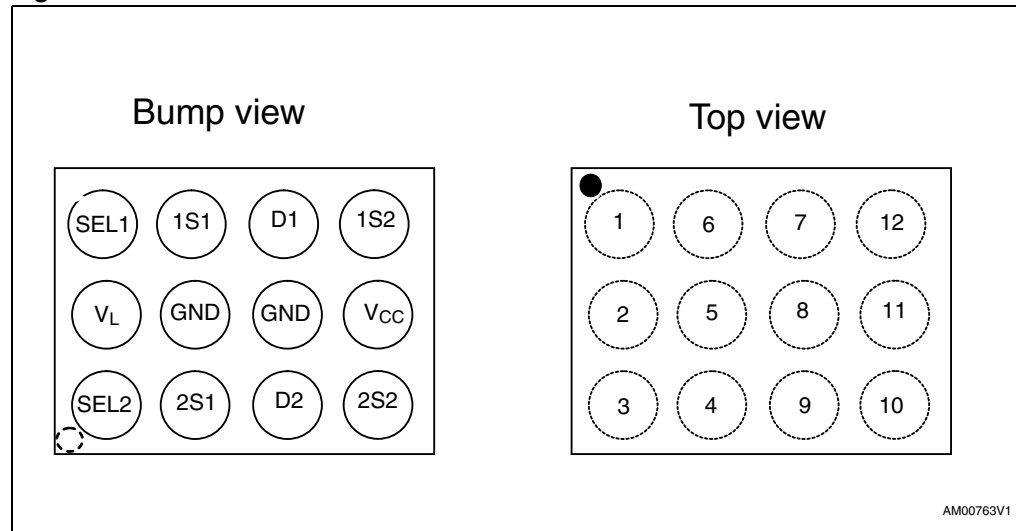
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1 Pin settings

1.1 Pin connections

Figure 1. Pin connection



1.2 Pin description

Table 2. Pin assignment

Pin number	Symbol	Name and function
1	SEL2	Selection control for switch 2
2	V_L	Logic supply voltage
3	SEL1	Selection control for switch 1
4	1S1	Independent channel for switch 1
5	GND	Ground (0 V)
6	2S1	Independent channel for switch 2
7	D2	Common channel for switch 2
8	GND	Ground (0 V)
9	D1	Common channel for switch 1
10	1S2	Independent channel for switch 1
11	V_{CC}	Positive supply voltage
12	2S2	Independent channel for switch 2

2 Logic diagram

Figure 2. Functional diagram

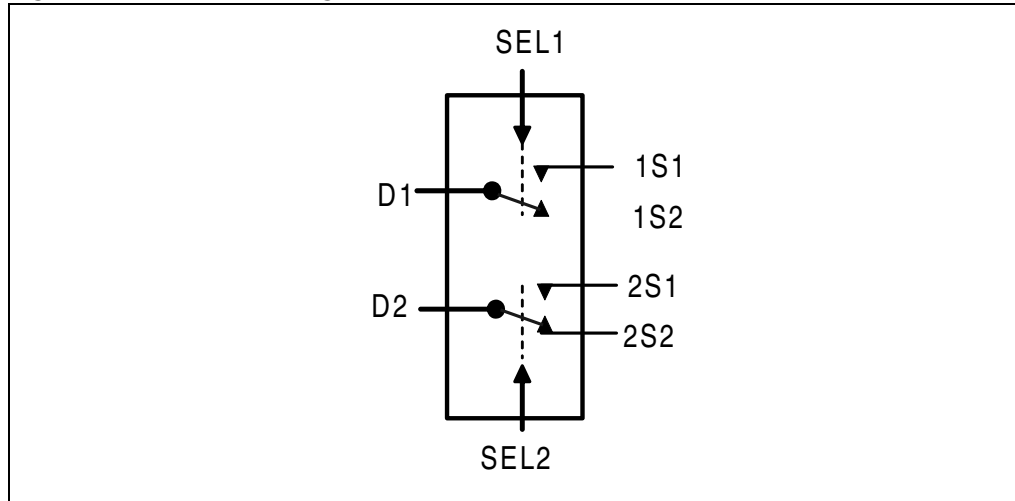


Figure 3. Circuit equivalent logic

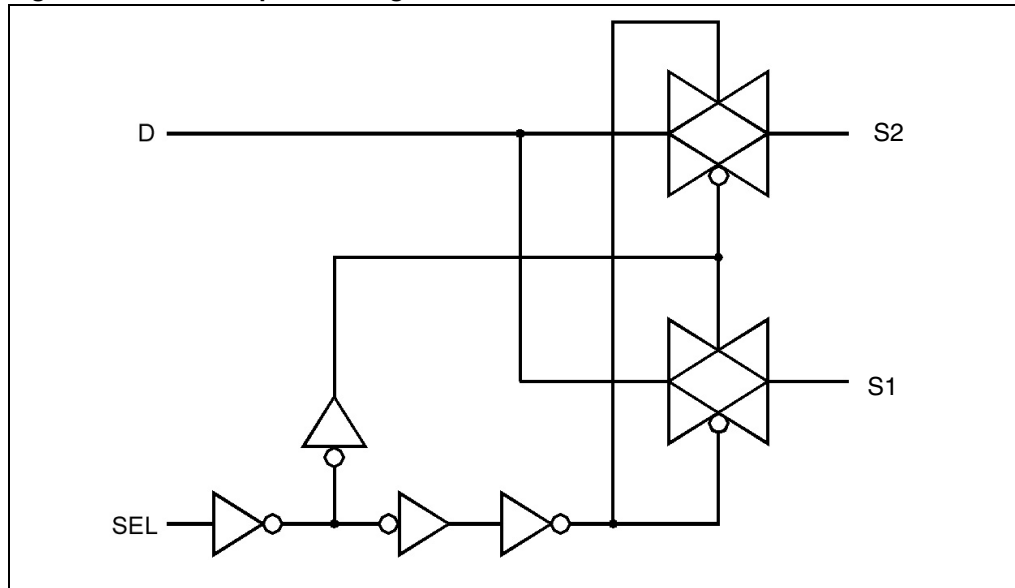


Table 3. Truth table

SEL	Switch S1	Switch S2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High impedance

3 Maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_L	Logic supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to $V_L + 5.5$	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0$ V)	- 50	mA
I_{IK}	DC input diode current ($V_{SEL} < 0$ V)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 300	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at $T_A = 70^\circ\text{C}$ ⁽¹⁾	500	mW
T_{stg}	Storage temperature	-65 to 150	$^\circ\text{C}$
T_L	Lead temperature (10 sec)	260	$^\circ\text{C}$

1. Derate above 70 $^\circ\text{C}$ by 18.5 mW/C

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.65 to 4.8	V
V_L	Logic supply voltage ⁽¹⁾	1.65 to V_{CC}	V
V_I	Input voltage	0 to V_{CC}	V
V_{IC}	Control input voltage	0 to V_L	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-40 to 85	$^\circ\text{C}$
dt/dv	Input rise and fall time control input	$V_L = 1.65$ to 2.7 V	0 to 20
		$V_L = 3.0$ to 4.8 V	0 to 10

1. V_L pin should not be left floating.

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	V _L (V)	Test condition	Value					Unit
					T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
V _{IH}	High level input voltage	1.65 – 4.3	1.65 – 1.95		1.25			1.25		V
			2.3 – 2.7		1.75			1.75		
			3.0 – 3.6		2.34			2.34		
			4.3		2.80			2.80		
V _{IL}	Low level input voltage	1.65 – 4.3	1.65 – 1.95				0.6		0.6	V
			2.3 – 2.7				0.8		0.8	
			3.0 – 3.6				1.05		1.05	
			4.3				1.5		1.5	
R _{ON}	ON resistance	1.8	1.65 – 4.3	V _S = 0 V to V _{CC} I _S = 100 mA		1.5	2.5		3.7	Ω
		2.25				0.75	1.0		1.3	
		3				0.50	0.65		0.8	
		3.7				0.45	0.55		0.7	
		4.3				0.40	0.50		0.65	
ΔR _{ON}	ON resistance match between channels ⁽¹⁾	1.8	1.65 – 4.3	V _S = 0 V to V _{CC} I _S = 100 mA		40				mΩ
		2.25				20				
		3				10				
		3.7				10				
		4.3				10				
R _{FLAT}	ON resistance flatness ⁽²⁾	1.8	1.65 – 4.3	V _S = 0 V to V _{CC} I _S = 100 mA		1000	1700		2000	mΩ
		2.25				300	430		550	
		3				170	220		270	
		3.7				160	210		270	
		4.3				160	210		270	
I _{OFF}	Sn OFF state leakage current	1.65 – 4.3	1.65 – 4.3	V _S = 0 to V _{CC} V _D = 0 to V _{CC}	-30		30	-300	300	nA
I _{ON}	Sn ON state leakage current	1.65 – 4.3	1.65 – 4.3	V _S = 0 to V _{CC} V _D = open	-30		30	-300	300	nA
I _D	D ON state leakage current	1.65 – 4.3	1.65 – 4.3	V _S = open V _D = 0 to V _{CC}	-30		30	-300	300	nA

Table 6. DC specifications (continued)

Symbol	Parameter	V _{CC} (V)	V _L (V)	Test condition	Value					Unit
					T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
I _{CC}	Quiescent supply current	1.65 – 4.3	1.65 – 4.3	V _{SEL} =V _{CC} or GND	-0.05		0.05	-0.2	0.2	μA
I _{SEL}	SEL leakage current	1.65 – 4.3	1.65 – 4.3	V _{SEL} =4.3V or GND	-0.2		0.2	-2	2	μA

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$

2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤ 5 ns)

Symbol	Parameter	Test conditions			Value					Unit
		V _{CC} (V)	V _L (V)		T _A = 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation delay	1.65-1.95	1.65 – 4.3			0.18				ns
		2.3 – 2.7				0.14				
		3.0 – 3.3				0.12				
		3.6 – 4.3				0.12				
t _{ON}	TURN-ON time	1.65 – 1.95	1.65 – 4.3	V _S = V _{CC} R _L = 50 Ω C _L = 30 pF		70	123		160	ns
		2.3 – 2.7				48	62		80	
		3 – 3.6				33	43		56	
		4.3				29	38		49	
t _{OFF}	TURN-OFF time	1.65 – 1.95	1.65 – 4.3	V _S = V _{CC} R _L = 50 Ω C _L = 30 pF		36	45		60	ns
		2.3 – 2.7				35	47		62	
		3 – 3.6				30	40		51	
		4.3				29	38		50	
t _D	Break-before-make time delay	1.65 – 1.95	1.65 – 4.3	C _L = 35 pF R _L = 50 Ω V _S = V _{CC} /2	10	42				ns
		2.3 – 2.7			10	22				
		3 – 3.6			5	15				
		4.3			5	12				

Table 7. AC electrical characteristics ($C_L = 35 \text{ pF}$, $R_L = 50 \Omega$, $t_r = t_f \leq 5 \text{ ns}$) (continued)

Symbol	Parameter	Test conditions			Value					Unit
		V_{CC} (V)	V_L (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		
					Min	Typ	Max	Min	Max	
Q	Charge injection	1.65 – 1.95	1.65-4.3	$C_L = 1\text{nF}$ $V_{GEN} = 0\text{V}$		83				pC
		2.3 – 2.7				98				
		3.0 – 3.3				114				
		3.6 – 4.3				140				
OIRR	Off Isolation ⁽¹⁾	1.65 – 4.3	4.3	$V_S = 1V_{RMS}$ $f = 100 \text{ kHz}$		77				dB
				$V_S = 1V_{RMS}$ $f = 1 \text{ MHz}$		67				
				$V_S = 1V_{RMS}$ $f = 5 \text{ MHz}$		50				
Xtalk	Crosstalk	1.65 – 4.3	4.3	$V_S = 1V_{RMS}$ $f = 100 \text{ kHz}$		80				dB
				$V_S = 1V_{RMS}$ $f = 1 \text{ MHz}$		67				
				$V_S = 1V_{RMS}$ $f = 5 \text{ MHz}$		50				
THD	Total harmonic distortion	2.3 – 4.3	4.3	$R_L = 600 \Omega$ $C_L = 50 \text{ pF}$ $V_S = V_{CC} V_{PP}$ $f = 600 \text{ Hz to } 20 \text{ kHz}$		0.01				%
BW	-3dB Bandwidth (switch ON)	1.65 – 4.3	4.3	$R_L = 50 \Omega$		50				MHz

1. OFF-isolation = $20 \log_{10} (V_D/V_S)$, V_D = output, V_S = input to off switch

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition			Value					Unit
		V _{CC} (V)	V _L (V)		T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
C _{SEL}	Control pin input capacitance	1.8 – 4.3	1.8 – 4.3	V _L = V _{CC}		30				pf
C _{SN}	Sn port capacitance	1.8 – 4.3	1.8 – 4.3	V _L = V _{CC}		94				pf
C _D	D port capacitance when the switch is enabled	1.8 – 4.3	1.8 – 4.3	V _L = V _{CC}		227				pf

5 Test circuits

Figure 4. ON resistance

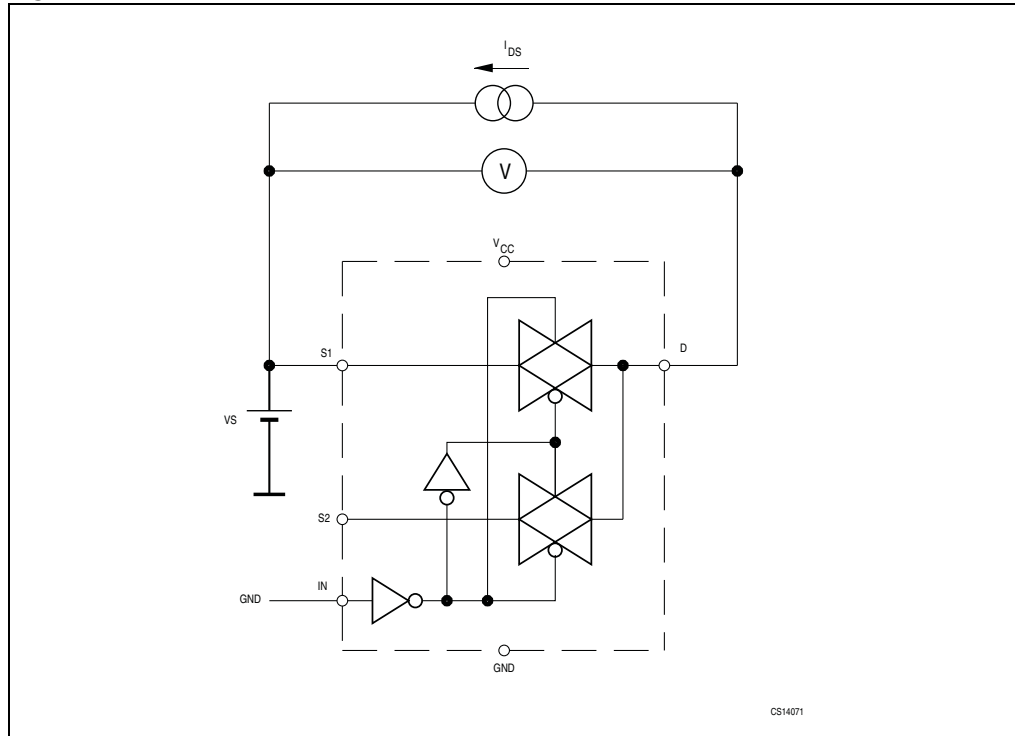


Figure 5. Bandwidth

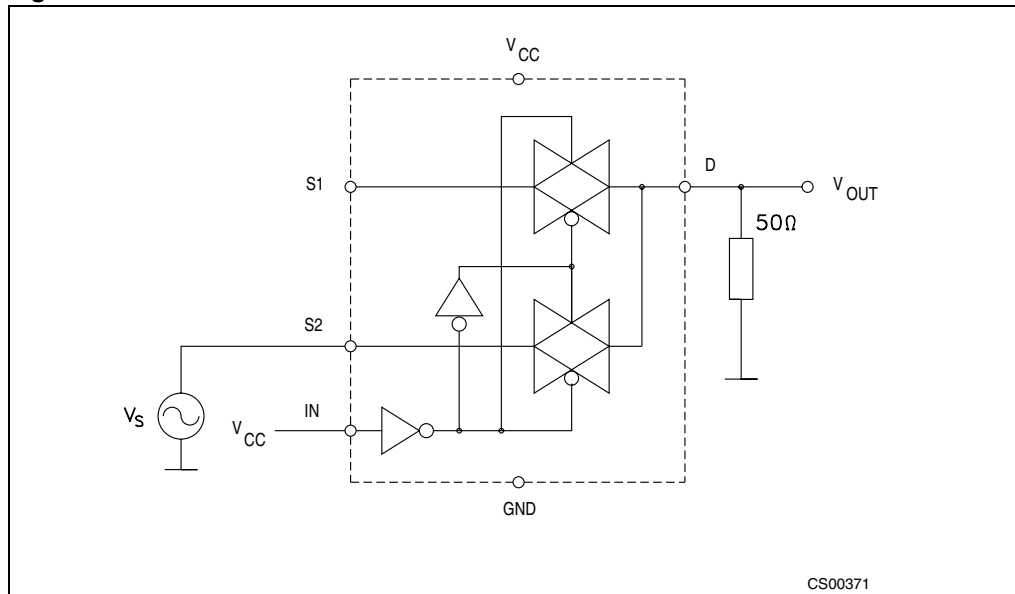


Figure 6. OFF leakage

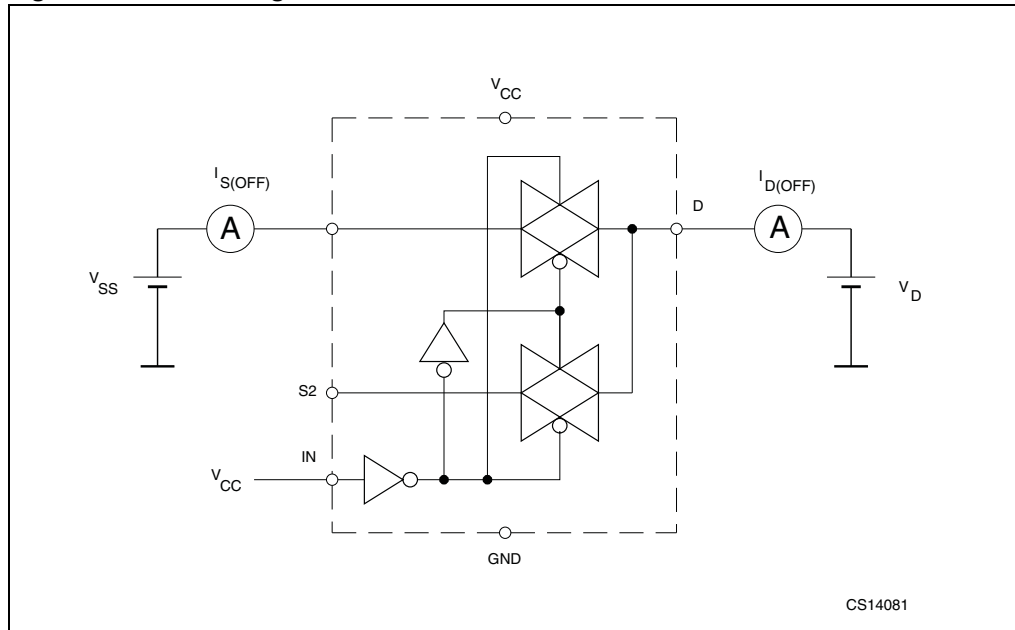


Figure 7. Channel-to-channel crosstalk

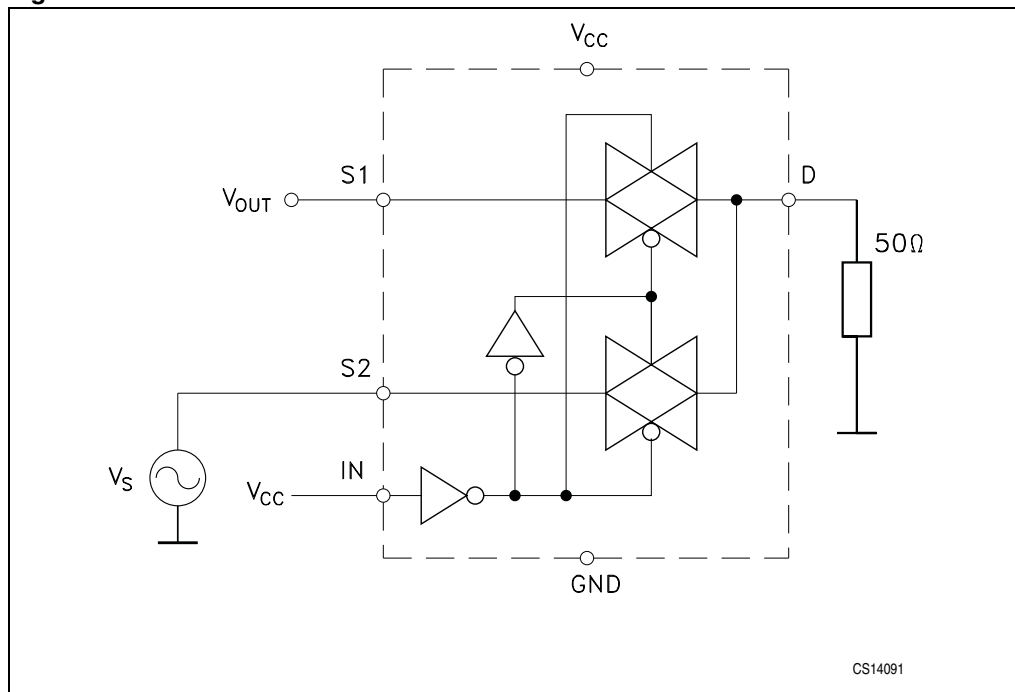


Figure 8. OFF isolation

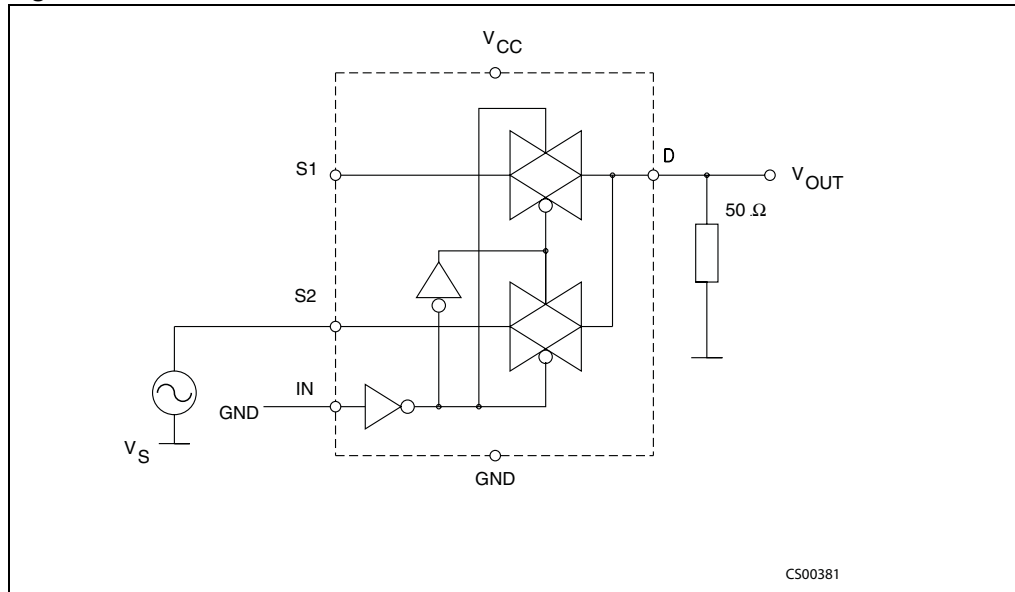
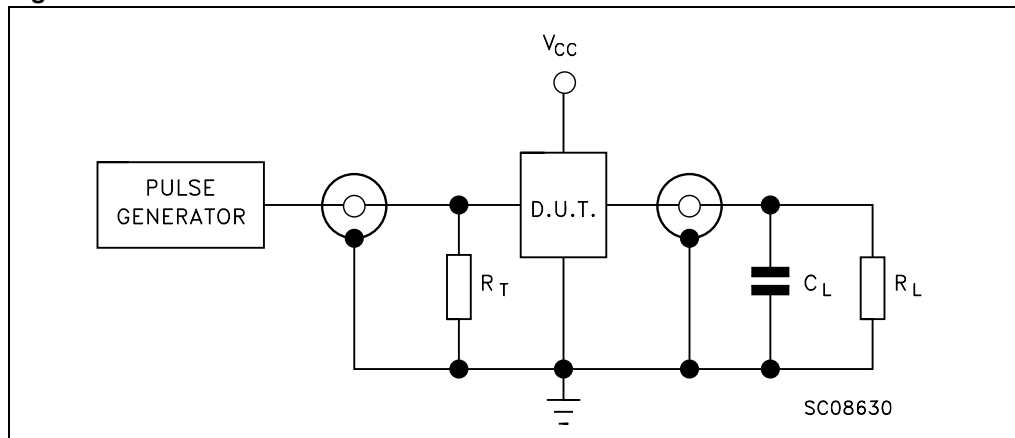


Figure 9. Test circuit



1. $C_L = 5/35$ pF or equivalent: (includes jig capacitance)
2. $R_L = 50 \Omega$ or equivalent
3. $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 10. Break-before-make time delay

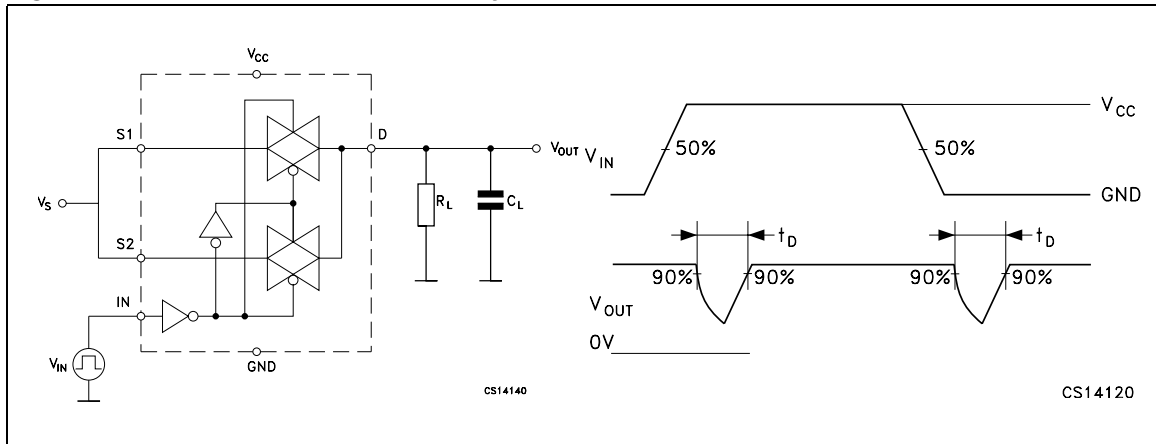


Figure 11. Switching time and charge injection
 ($V_{GEN} = 0\text{ V}$, $R_{GEN} = 0\ \Omega$, $R_L = 1\text{ M}\Omega$, $C_L = 100\text{ pF}$)

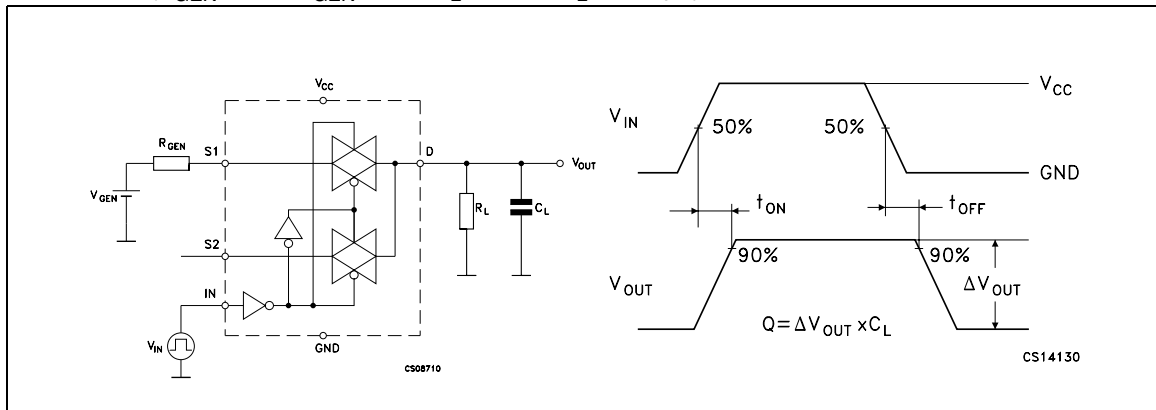
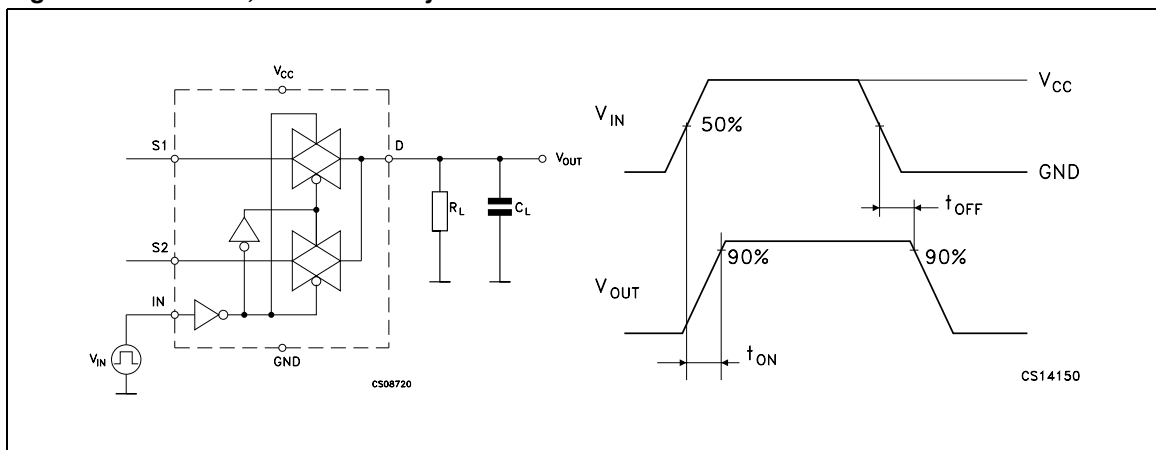


Figure 12. Turn ON, turn OFF delay time



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 13. Flip-chip 12 mechanical outline

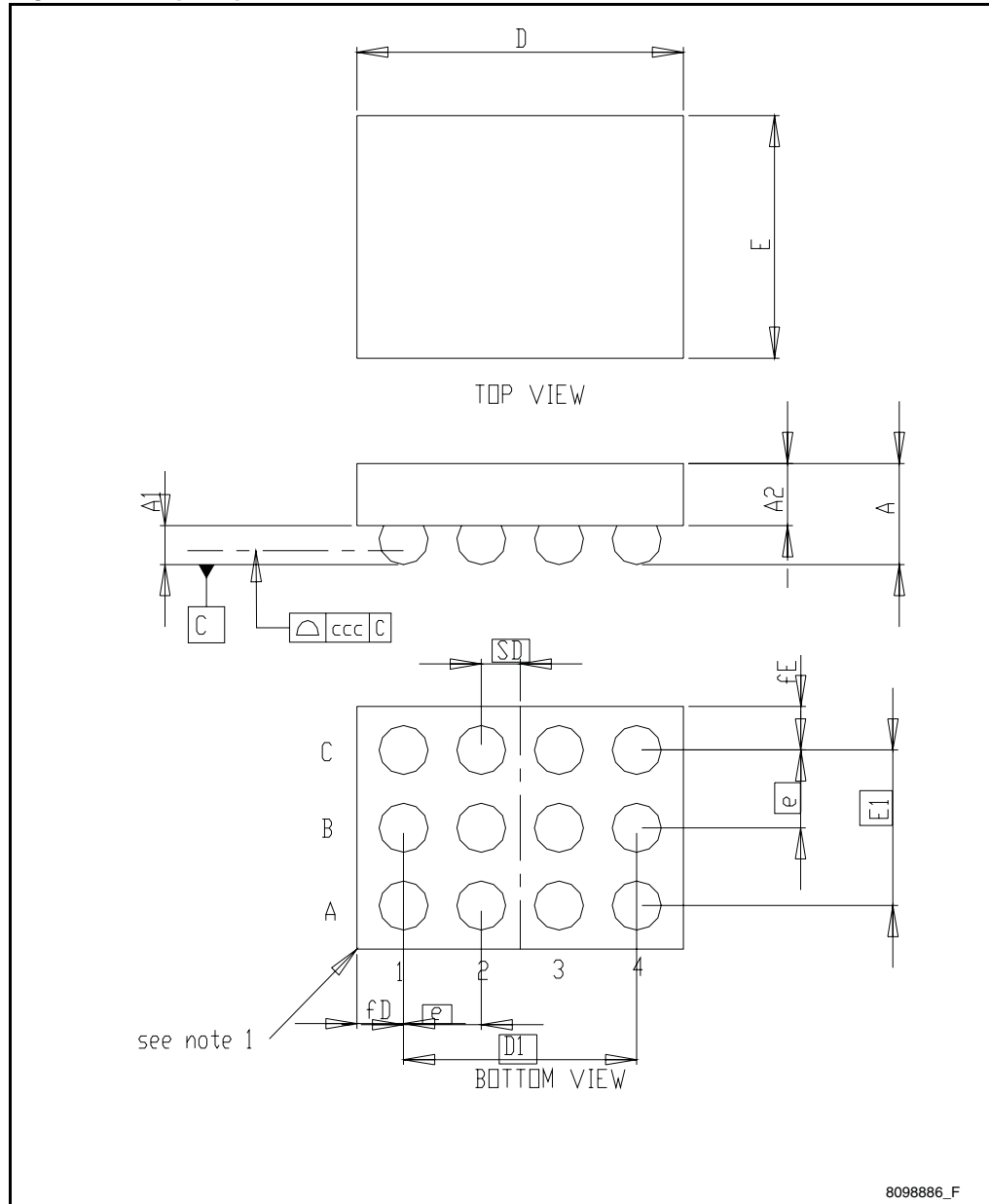


Table 9. Flip-chip 12 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.535	0.58	0.625
A1	0.18	0.205	0.23
A2	0.355	0.375	0.395
b	0.215	0.255	0.295
D	1.85	1.9	1.95
D1		1.5	
e	0.45	0.5	0.55
E	1.35	1.4	1.45
E1		1	
SD		0.25	
f	0.19	0.2	0.21
ccc		0.08	

Figure 14. Footprint recommendation

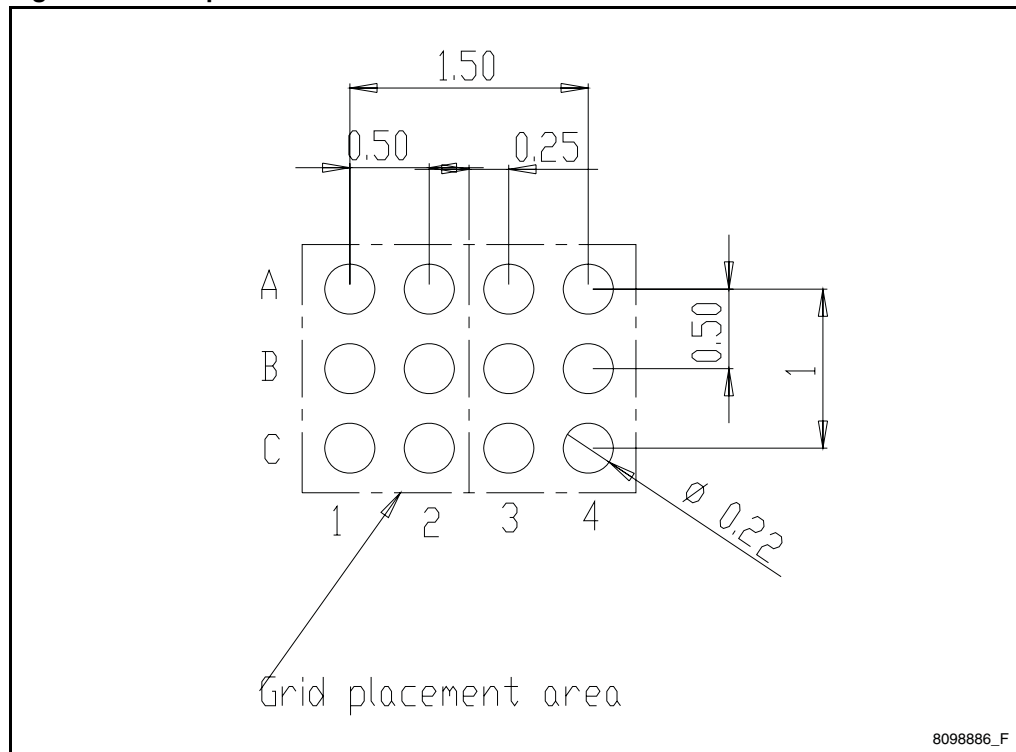


Figure 15. Flip-chip 12 tape information

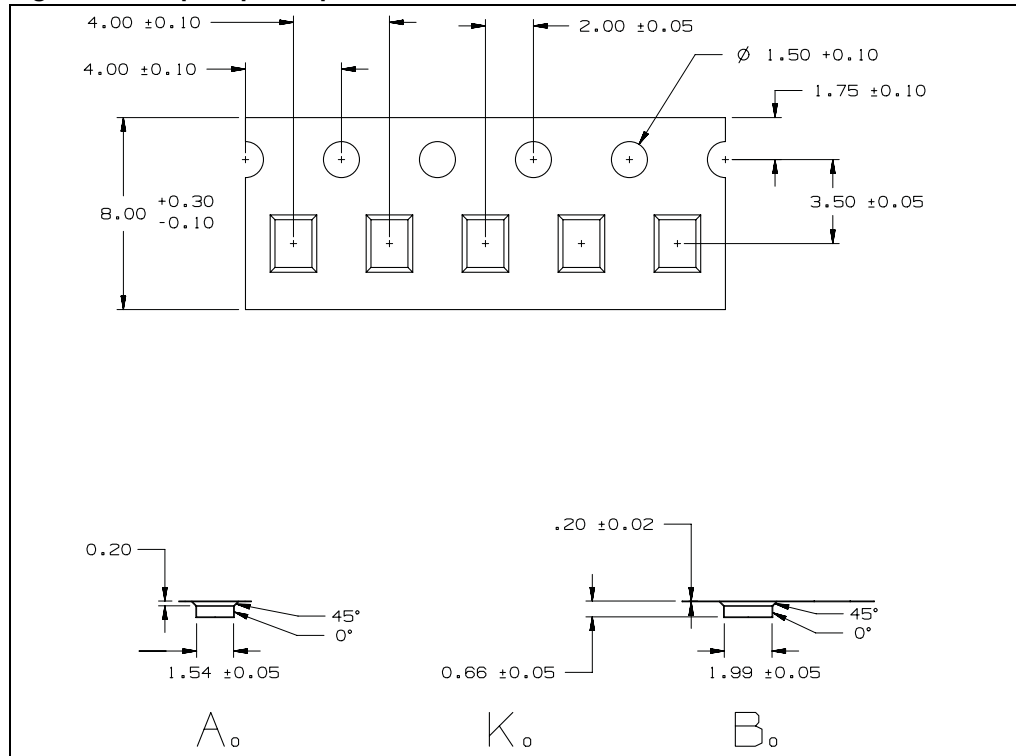
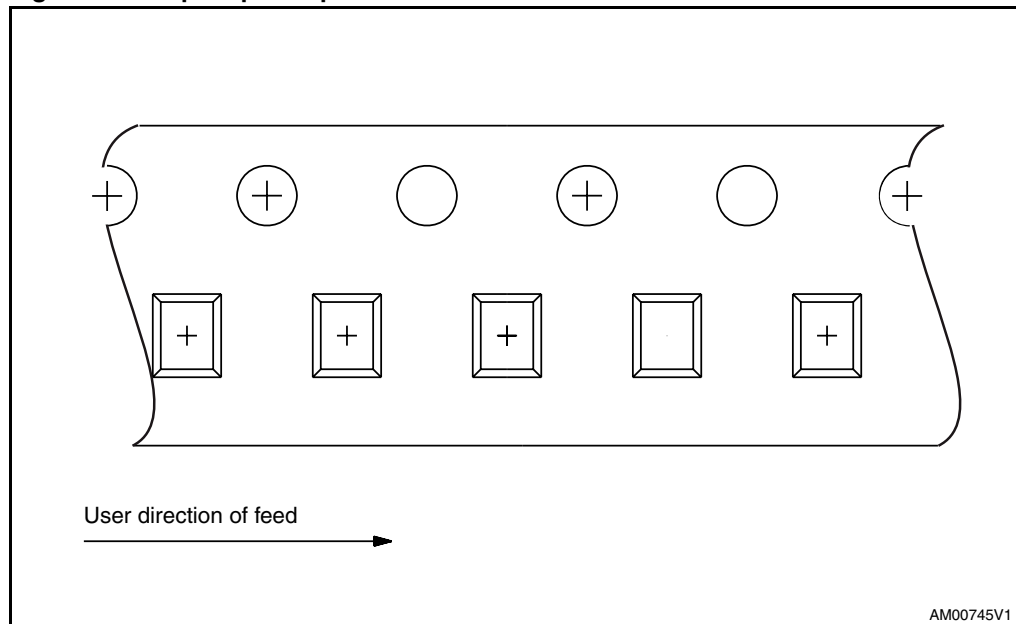


Figure 16. Flip-chip 12 tape orientation



7 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-Nov-2008	1	Initial release.

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