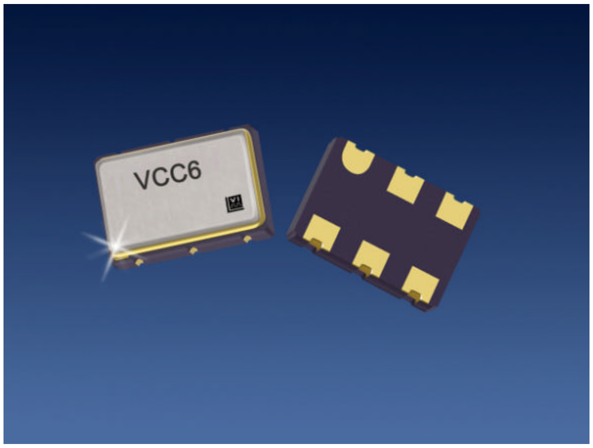
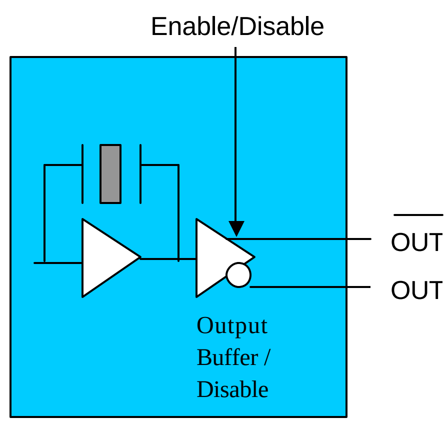
VCC6-Q/R Series

2.5 and 3.3 volt LVPECL Crystal Oscillator



The VCC6 Crystal Oscillator



Features

- 2.5 or 3.3V LVPECL
- 3rd Overtone Crystal for best jitter performance
- Output frequencies to 270 MHz
- Low Jitter < 1 pS rms, 12kHz to 20MHz
- Enable/Disable for test and board debug
- -10/70 or –40/85 °C operating temperature
- Hermetically sealed ceramic SMD package
- Product is compliant to RoHS directive

Applications

- SONET/SDH/DWDM
- Fiber Channel
- Ethernet, Gigabit Ethernet
- Storage Area Network
- Digital Video
- Broadband Access

Description

Vectron's VCC6 Crystal Oscillator (XO) is quartz stabilized square wave generator with a LV-PECL output, operating off a 3.3 volt supply.

The VCC6 is uses 3rd overtone crystals for frequencies under 200MHz, resulting in low jitter performance, typically 0.5pS rms in the 12 kHz to 20MHz band.

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Performance Characteristics

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	f_O	10		270	MHz
Supply Voltage [1], 3.3V Q option 2.5V R option	V_{DD}	3.15 2.25		3.45 2.75	V
Supply Current	I_{DD}			98	mA
Output Logic Levels, 0/70°C Output Logic High[2] Output Logic Low[2]	V_{OH} V_{OL}	V_{DD}-1.025 V_{DD}-1.810		V_{DD}-0.880 V_{DD}-1.620	V V
Output Logic Levels, -40/85°C Output Logic High[2] Output Logic Low[2]	V_{OH} V_{OL}	V_{DD}-1.085 V_{DD}-1.830		V_{DD}-0.880 V_{DD}-1.555	V V
Transition Times Rise Time[2] Fall Time[2]	t_R t_F			600 600	ps ps
Symmetry or Duty Cycle[3]	SYM	45	50	55	%
Operating temperature (*ordering option*)	T_{OP}	-10/70 or –40/85			°C
Stability (*ordering option)*[4]	deltaF/F	+/-25, +/-50 or +/-100			ppm
Jitter, 12kHz to 20MHz[5] Cycle to Cycle, rms Cycle to Cycle, peak-peak Period Jitter, rms Period Jitter, peak-peak			0.5 4.8 38 2.7 23	1	pS
Output Enabled[6]	V_{IH}	0.7*V_{DD}			V
Output Disabled[6]	V_{IL}			0.3*V_{DD}	V
Output Enable/Disable time	$t_{E/D}$			200	nS
Enable/Disable Leakage Current	I_{IL}			±200	uA
Output Enable Pull-Up Resistor[6] Output Enabled Output Disabled			33 1		Kohm Mohm

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible and terminated to ground.
2. Figure 1 defines these parameters. Figure 2 illustrates the operating conditions under which these parameters are tested and specified.
3. Symmetry is measured defined as On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging (40 degreesC/10 years) and shock and vibration (not under operation).
5. Measurements made on a VCC6-QAB-125M000 using a LeCroy 8600, 25K samples.
6. Output will be enabled if Enable/Disable is left open. The pull resistor changes to a higher value, operating in a "power saving mode" when Enable/Disable is set to a logic 0.

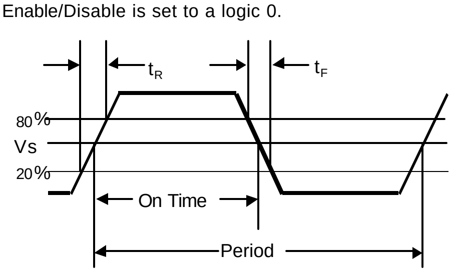

Figure 1. Output Waveform

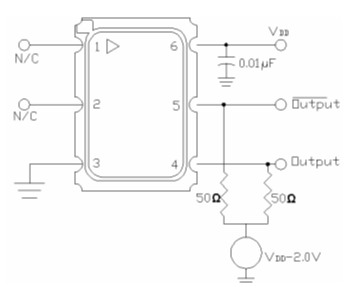

Figure 2. Typical Output Test Conditions (25±5°C)

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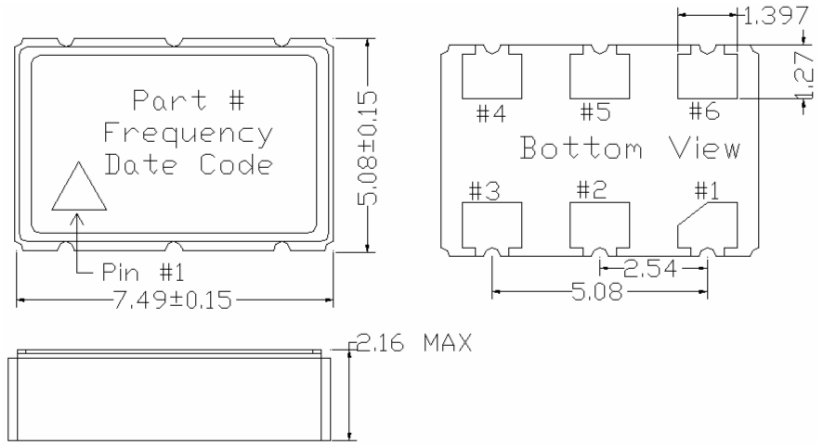
Outline Diagram and Pin Out

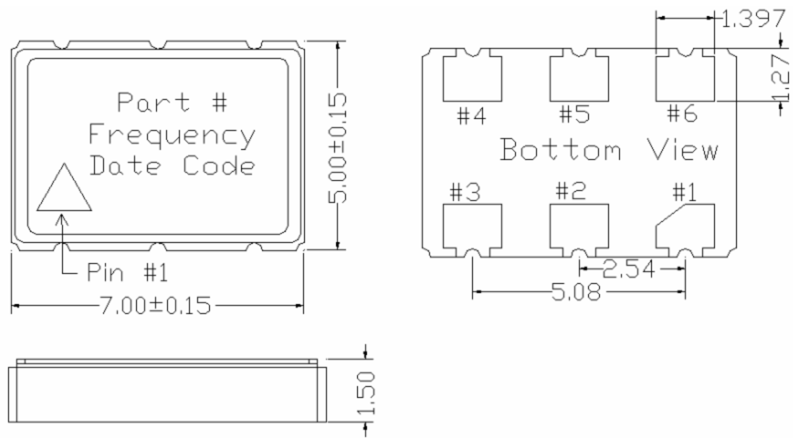
Table 2. VCC6-QAx Pinout		
Pin #	**Symbol**	**Function**
1	NC	No Connection
2	E/D	Enable/Disable function
3	GND	Ground
4	f_O	Output Frequency
5	Cf_o	Complementary Output Frequency
6	V_{DD}	Supply Voltage



Gold over Nickel plating

Figure 3 VCC6-QAx Package Drawing

Table 3. VCC6-QCx Pinout		
Pin #	**Symbol**	**Function**
1	E/D	Enable/Disable function
2	NC	No Connection
3	GND	Ground
4	f_O	Output Frequency
5	Cf_o	Complementary Output Frequency
6	V_{DD}	Supply Voltage



Gold over Nickel plating

Figure 4. VCC6-QCx Package Drawing

Terminating PECL Outputs

The VCC6 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 5. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 6, and a pull-up/pull-down scheme as shown in Figure 7. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

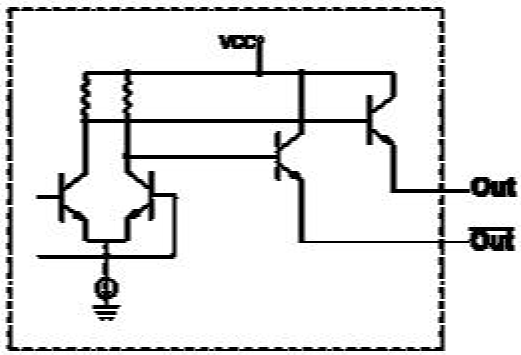
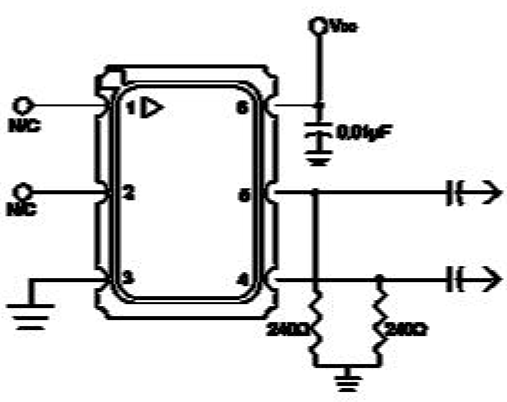


Figure 5. Standard PECL Output Configuration



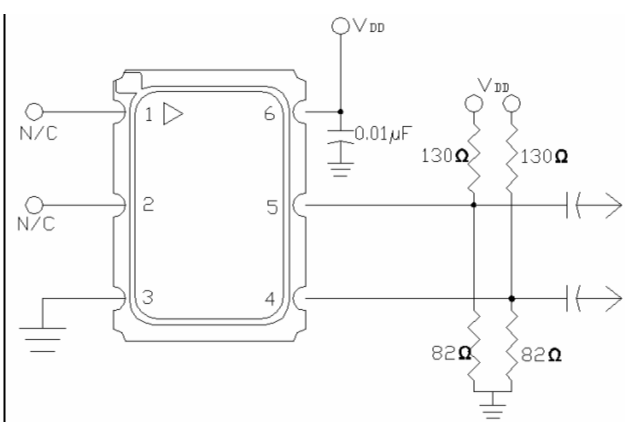


Figure 6. Single Resistor Termination
Resistor value are typically:
120 to 240ohms for 3.3V
82 to 120 ohms for 2.5V

Figure 7. Pull-up Pull-down Termination
Resistor values are typically:
130 and 82 ohms for 3.3V
240 and 62 ohms for 2.5V

Enable/Disable Functional Description

Under normal operation the Enable/Disable is left open or set to a logic high state. When the E/D is set to a logic low, the oscillator stops and the both the output and complementary outputs are in a high impedance state. This helps facilitate board testing and troubleshooting.

Power Saving Pull-Up Resistor
The E/D pull-up resistor changes in response to the input logic level; the pull-up resistor is a large value when E/D is set to a logic low, which reduces the current consumed. When E/D is open, or set to a logic high, the pull-up resistance becomes a smaller value which helps decrease the effects of external noise.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	-0.5 to +7.0	Vdc
Enable/Disable	V_{IN}	-0.5 to V_{DD}+0.5	Vdc
Storage Temperature	Tstorage	-55/125	°C

Reliability

The VCC6 qualification tests included:

Table 5. Environnemental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Solderability	MIL-STD-883 Method 2003
Gross and Fine Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the the VCC6, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

Table 6. ESD Ratings

Model	Minimum	Conditions
Human Body Model	1500	MIL-STD-883 Method 3015
Charged Device Model	1000	

IR Reflow and Suggested Pad Size Layout

The VCC6 has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements and maximum parameters are listed in Table 6, lower temperatures are also acceptable. The VCC6 is hermetically sealed so an aqueous wash is not an issue. **Frequencies >200MHz will need to be reflowed at 220C max.**

Table 7. Reflow Profile (IPC/JEDEC J-STD-020B)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 200 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C (max)	t_P	10 sec Max
Time At 240°C (max)	tp2	60 sec MAX
Ramp Down	R_{DN}	6 °C/sec Max

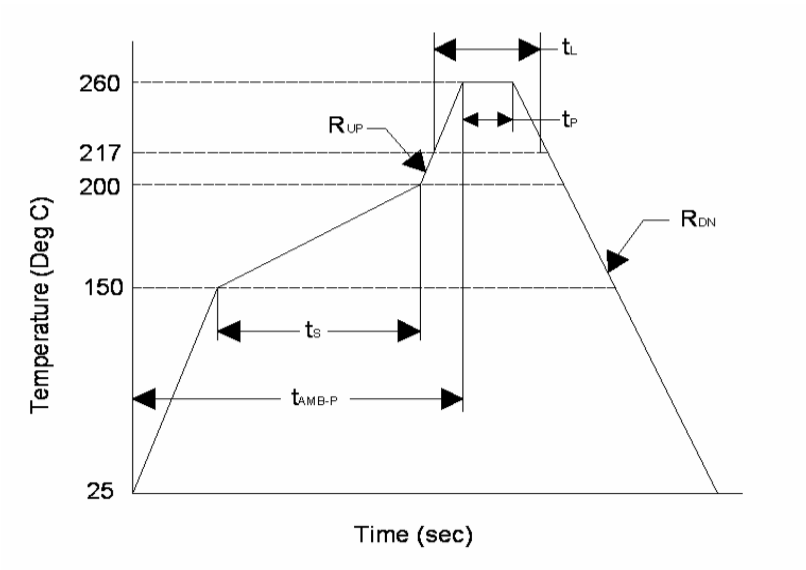


Figure 8. IR Reflow Diagram

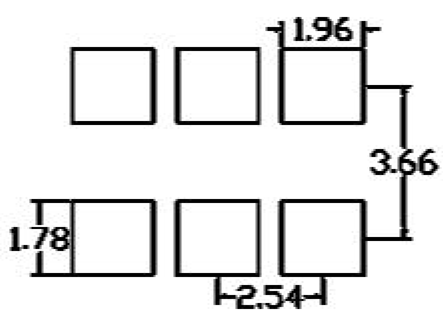


Figure 9. Pad Size Diagram

Tape and Reel

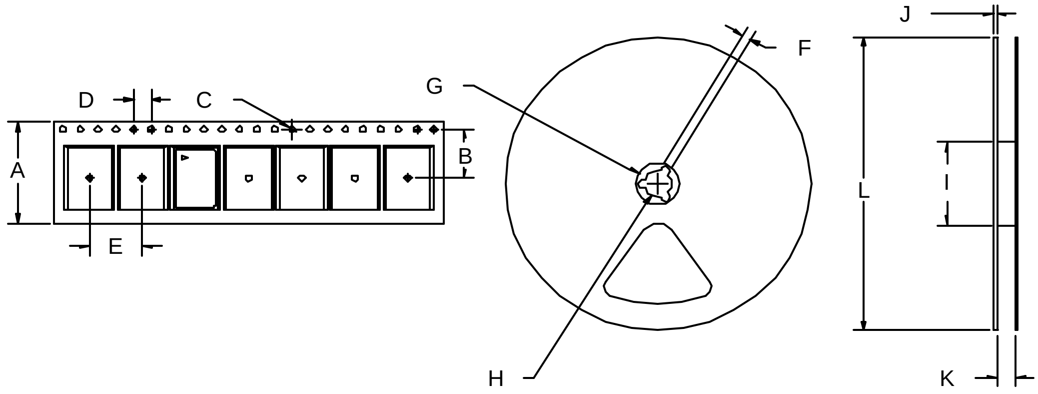


Figure 10. Tape and Reel Diagram

Table 8. Tape and Reel Dimensions (mm)													
Tape Dimensions						Reel Dimensions							# Per
Product	A	B	C	D	E	F	G	H	I	J	K	L	Reel
VCC6	12	5.5	1.5	4	8	1.78	20.6	13	55	6	12.4	178	250

Table 9. Standard Frequencies (MHz)

19.440	27.000	27.027	35.000	37.000	38.880
40.000	40.680	48.000	50.000	52.300	62.500
64.000	64.375	74.1758	74.250	76.800	77.760
80.000	83.125	87.000	90.000	91.875	93.000
98.304	100.000	105.000	106.000	106.250	110.000
125.000	130.000	130.5882	133.000	134.560729	135.000
136.000	143.000	145.221	150.000	153.500	155.520
156.000	156.250	159.375	160.000	160.160	161.1328
163.235	164.3555	165.000	166.000	166.6286	166.6667
166.67	167.00	167.3316	168.200912	171.000	173.3707
175.000	180.000	187.500	190.000	195.3125	200.000
212.500					

Other frequencies may be available upon request. Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

Ordering Information

VCC6 – Qxx – xxxMxx

Product Family

Crystal Oscillator

Supply Voltage, Output

Q=3.3, LVPECL

R=2.5V, LVPECL

Enable/Disable

A: E/D is on Pin 2, Pin 1 is a NC

C: E/D is on Pin 1, Pin 2 is a NC

Frequency MHz

example: 125M00= 125.00

Stability Options/Temperature

A: +/-100ppm -10 to 70 C

B: +/-50ppm -10 to 70 C

C: +/-100ppm -40 to 85 C

D: +/-50ppm -40 to 85 C

E: +/-25ppm -10 to 70 C

F: +/-25ppm -40 to 85 C

NOTE: *Not all combinations of options are available. A ±20ppm option, VCC6-107, is also available.*

For Additional Information, Please Contact:

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VCC6-Q/R (REVISION DATE: April 18, 2005)