CT2565
Bus Controller, Remote Terminal and BUS Monitor
FOR MIL-STD-1553B

Features

- **Second Source Compatible to the BUS-65600**
- **RTU implements all dual redundant mode codes**
- **Selective mode code illegalization available**
- **16 bit microprocessor compatibility**
- **BC checks status word for correct address and set flags**
- **RTU illegal mode codes externally selectable**
- **16 bit µProcessor compatibility**
- **DMA handshaking for subsystem message transfers**
- **MIL-PRF-38534 compliant circuits available**
- **DESC SMD #5962–88585 Pending**
- **Packaging – Hermetic Metal**
  - **78 Pin, 2.1" x 1.87" x .25" Plug-In type package**
  - **82 Lead, 2.2" x 1.61" x .18" Flat package**

AEROFLEX
CIRCUIT TECHNOLOGY
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General Description

The CT2565 is a dual redundant MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT), and Bus Monitor, (BM) Bus packaged in a 1.9" x 2.1" hermetic hybrid. It provides all the functions required to interface a MIL-STD-1553 dual redundant serial data bus transceiver, (Aeroflex's ACT4487 for example) and a subsystem parallel three-state data bus. Utilizing a custom monolithic IC, the CT2565 provides selectable operation as a Bus Controller, Remote Terminal or a Bus Monitor (BM).

The CT2565 is compatible with most µprocessors. It provides a 16 bit three-state parallel data bus and uses direct memory access (DMA type) handshaking for subsystem transfers. All message transfer timing as well as DMA and control lines are provided internally. Subsystem overhead associated with message transfers is therefore minimized. Interface control lines are common for both BC and RT operation.

The CT2565 features the capability for implementing all dual redundant MIL-STD-1553 mode codes. In addition, any mode code may (optional) be illegalized through the use of an external (200ns access time) PROM. Complete error detection capability is provided, for both BC and RTU operation. Error detection includes: response time-out, inter message gaps, sync, parity, Manchester, word count and bit count. The CT2565 complies with all the requirements of MIL-STD-1553.

The hybrid is screened in accordance with the requirements of MIL-STD-883 and operates over the full military temperature range of -55°C to +125°C.

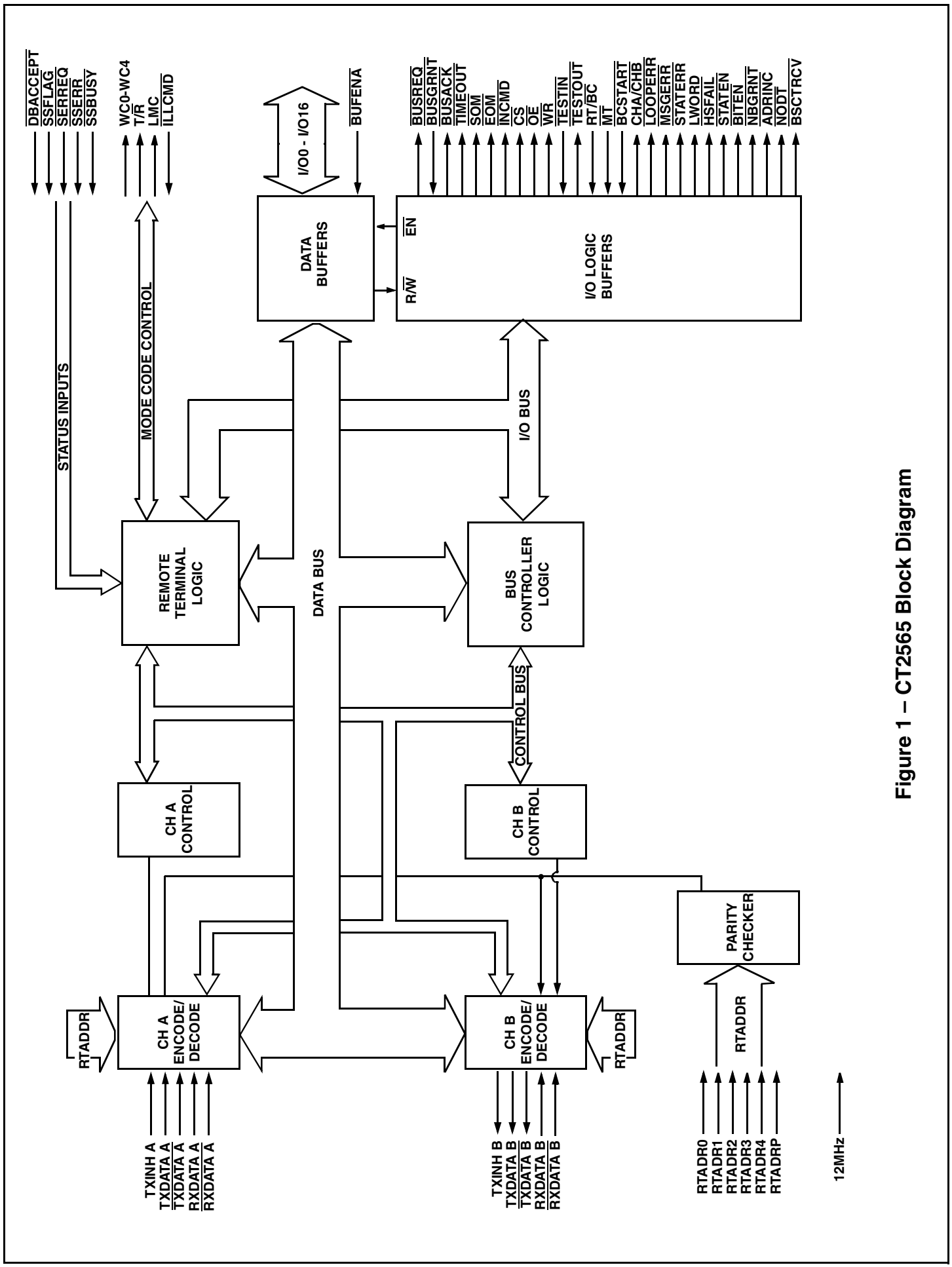


Figure 1 – CT2565 Block Diagram

Values at nominal Power Supply Voltages unless otherwise specified

PARAMETER	VALUE	UNITS
Logic		
V_{IH}	2.0 min	V
V_{IL}	0.8 max	V
V_{OH}	3.7 min	V
V_{OL}	0.4 max	V
I_{IH}	±100 max	µA
I_{IL}	-0.4 max	mA
I_{OL} *	±1.2 max	mA
I_{OH} *	±0.4 max	mA
C_{IN} (f = 1MHz)	20 max	pF
C_{OUT} (f = 1MHz)	20 max	pF
Power Supply		
+5VDC		
Tolerances	±10 max	%
Supply Current	50 typ (70 max)	mA
Internal Decoupling	1.5 typ	µF
Temperature Range		
Operating (Case)	–55 to +125	°C
Storage	–65 to +150	°C
Physical Characteristics		
Size		
78 pin DDIP	1.9 x 2.10 x 0.25 (48.30 x 53.34 x 6.35)	in (mm)
82 pin flatpack	1.6 x 2.19 x 0.15 (40.64 x 55.63 x 3.81)	in (mm)
Weight	1.7 (48)	oz (g)

* I_{OL} and I_{OH} parameters are indicated for all logic outputs except Data Bus (DB0 – DB15) which are ±5mA for both parameters.

Table 1 – CT2565 Specifications

GENERAL

The CT2565 uses a custom CMOS ASIC for protocol logic and I/O buffering to provide low power dissipation in its small package.

The CT2565 performs a continuous on-line Built-In-Test (BIT); in this test the last transmitted word of each message transfer is wrapped around through the active receiver channel and verified against the captured encoded word. A user-defined loop test under subsystem control can also be implemented. Numerous error flags are provided to the subsystem including message error, status error, response time out and loop test error.

An external 12 MHz, TTL clock connected to Pin 39 is required.

Where appropriate, references to signal names and their associated pin numbers for the 78 pin DDIP package are made throughout this document. For flatpack model pin numbers, refer to Table 10.

BC/RTU/MT Initialization

The CT2565 provides BC, RTU, and MT operating modes. The operating mode if dynamically selectable through two static control inputs as listed in Table 2. It is recommended that a master RESET signal be issued (80ns min) prior to mode selection to clear the internal registers.

MIL-STD-1553 Word Types

Figure 2 illustrates the three MIL-STD-1553 word types: Command, Data, and Status.

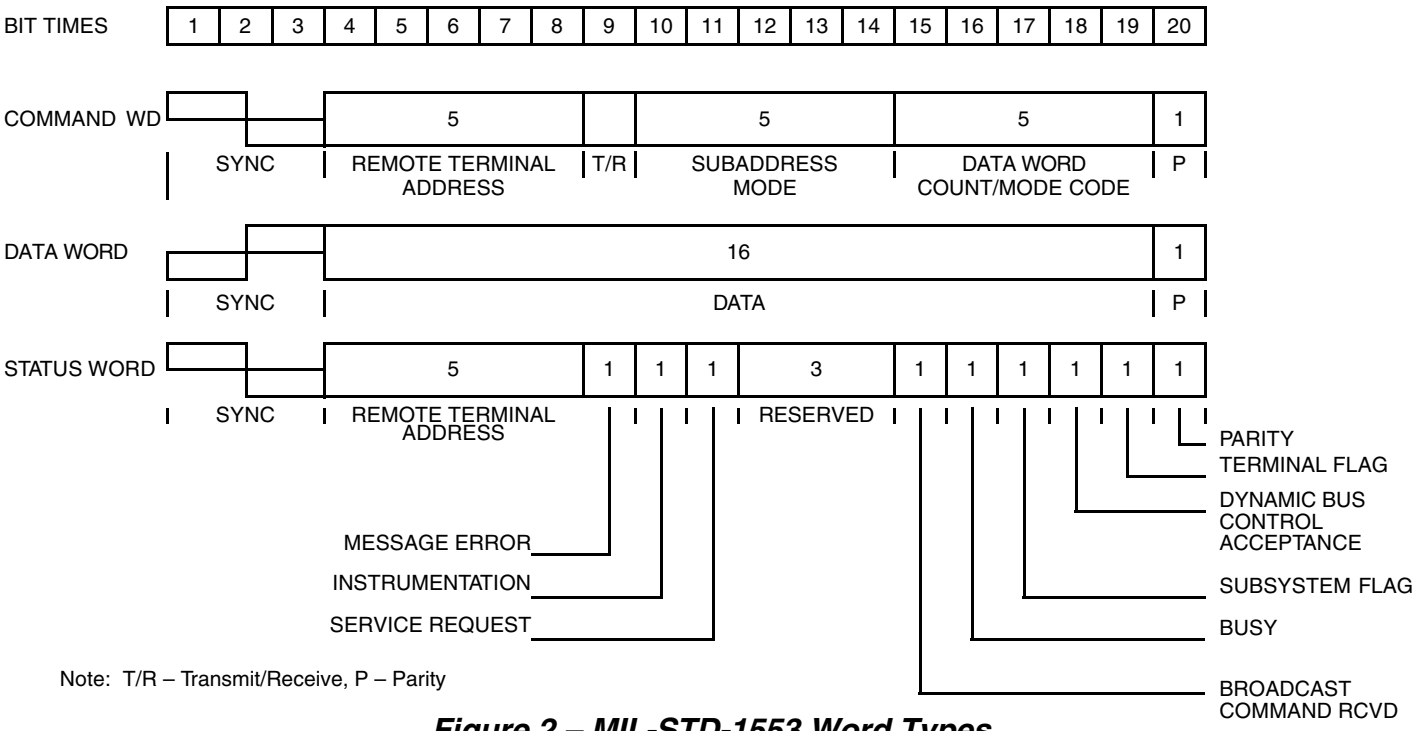


Figure 2 – MIL-STD-1553 Word Types

MODE	RT/$\overline{BC}$ (PIN 1)	$\overline{MT}$ (PIN 2)
BC	0	1
RT	1	1
MT	0	0

Table 2 – Operating Modes

DMA - Type Handshake

All BC and RT word transfers are preceded by a request-grant-acknowledge format DMA handshake procedure. Timing information is provided in BC, RTU and MT sections.

In MT mode, the 1553 transmission is transferred along with an identification Word using a single DMA handshake containing two memory-write operations. The DMA format requires that the subsystem provide a bus grant ($\overline{BUSGRNT}$ pin 45) low within a timeout period. Note that $\overline{BUSGRNT}$ should be set to logic "1" before another bus request ($\overline{BUSREQ}$) is issued.

Memory Read/Write

With the single exception of an RT command word transfer, all subsystem transfers take the form of a static memory read or write. A low pulse on both the chip select ($\overline{CS}$) and output enable ($\overline{OE}$) or a low pulse on $\overline{CS}$ and write enable ($\overline{WE}$) (pins 17, 18 and 44 respectively) indicates data is valid on the parallel data bus for the duration of the pulse. The rising edge of $\overline{CS}$ triggers an address increment ($\overline{ADRINC}$ pin) low output pulse used to increment the subsystem memory address for successive transfers.

BC OPERATION

In the BC mode, the CT2565 initiates all MIL-STD-1553 data and control message transfers. Figure 3 details specific message transfer flow and Table 3 lists subsystem memory allocation. The subsystem, or host processor, must provide a CT2565 protocol Control Word (See Figure 4) and MIL-STD-1553 command and data words. The CT2565 will transfer the RTU status response and provide message transfer validation during an active transfer. All parallel word transfers occur in the form of a DMA (request-grant-acknowledge) handshake with memory read or operation as shown in Figures 5 and 6.

Command Transfer

In the BC mode pulse $\overline{BCSTART}$ (pin 41) low. Following the pulse, the CT2565 will initiate a DMA handshake and memory read for; the control, word, command word(s) and up to 32 data words. No handshake timeout is enforced in the BC mode (CT2565) remains idle during $\overline{BUSREQ}$ to $\overline{BUSGRNT}$), however 1553 protocol must be maintained.

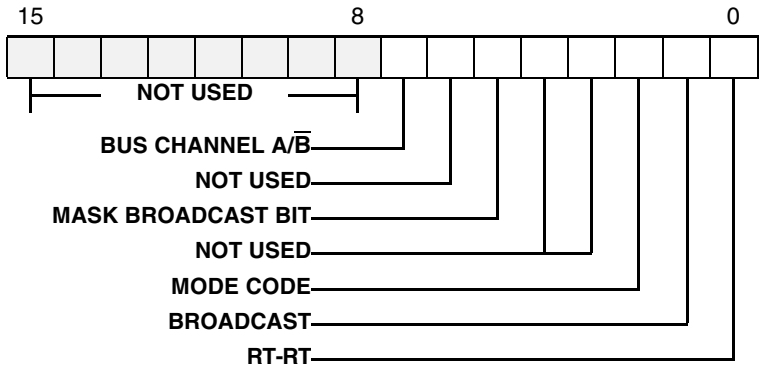
Note that commands are named from the BC's point-of-view (for example, a TRANSMIT CMD indicates the addressed RTU must transmit data).

RECEIVE	TRANSMIT
Control Word	Control Word
Receive Command	Transmit Command
Data 1	Looped Command Word
•	RTU Status
•	Data 1
Last Data	•
Looped Data Word	•
RTU Status	Last Data

Table 3 – BC Memory Allocation

Loop Test

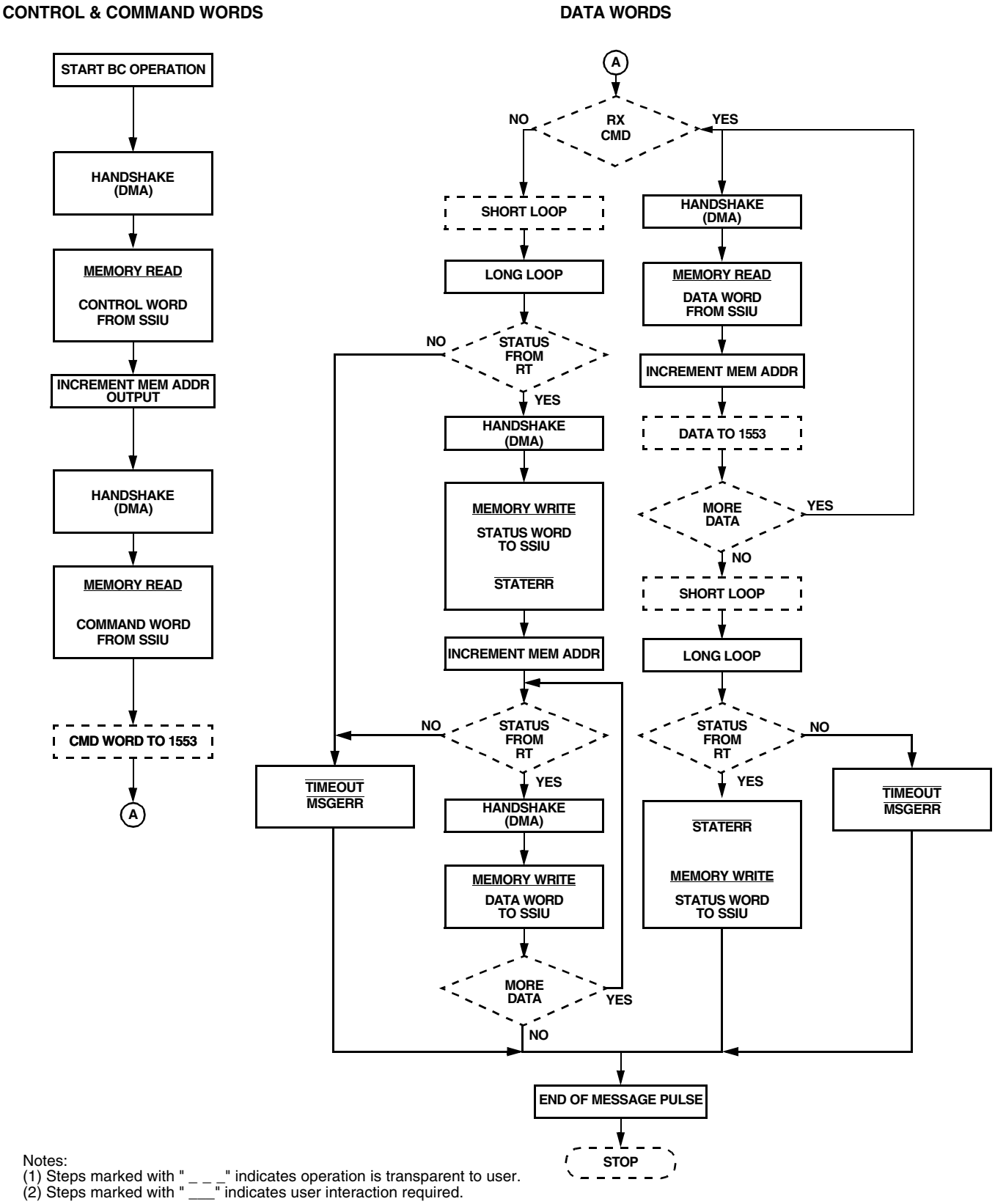
Upon receipt from the subsystem, the last word to be transmitted within a given message transfer (command or Data word) is stored in a CT2565 internal register. As this word is transmitted to the 1553 bus, it is looped back through the active receiver channel for auto-BC, Short Loop verification. A LOOPERR (.5us typ) low pulse indicates a mismatch between the stored and looped word. The CT2565 also initiates a handshake with a memory write to the subsystem for user-defined, "long loop" (subsystem, CT2565, subsystem) verification. Note that both short and long loop testing are initiated for all transfers (on the last word transmitted to 1553). Subsystems response to use Long Loop Test is to compare the loaded word to what was looped back into memory.



BIT	DEFINITION
BUS CHANNEL A/B	When logic "1" transmits over 1553 Bus A. When logic "0" transmits over 1553 Bus B (See note)
MASK BROADCAST BIT	Always set to "0"
MODE CODE	Command Word count field signifies mode code type
BROADCAST	Multiple RTU's addressed, no status word expected
RT-RT	When set, RTU(b) transmits, RTU(a) receives. Both RTU Status Words are validated and sent to subsystem.

Note: Messages-transmission (routing) status pin (pin 16, Chan A/$\overline{B}$) becomes active after loading the control word and command word respectively. The signal is cleared by $\overline{RESET}$ or $\overline{EOM}$ low.

Figure 4 – BC Control Word



Notes:
(1) Steps marked with " _ _ _" indicates operation is transparent to user.
(2) Steps marked with " ___" indicates user interaction required.

Figure 3 – BC Message Transfer Flow

TRANSFER/CONDITION	DESCRIPTION	ERROR SIGNAL	PIN
CONTROL/COMMAND WORD 1 Handshake Failure	Memory read by BC subsystem. No response to Bus Request within timeout period.	 BC waits for Grant (no 1553 timing error)	 -
LOOPED WORD Short Loop Failure Long Loop Failure	Looped back through receiver. Received Word ≠ last xmitted word. DMA/Write looped word to subsystem.	 $\overline{\text{LOOPERR}}$ User Defined	 46 -
RT-RT	Status-RT1, data, status-RT2 response to follow receive, transmit, commands.	(See definitions in STATUS/DATA WORD below)	-
STATUS WORD No Status Received within 15.5μS	$\overline{\text{NODT}}$ timeout	$\overline{\text{TIMEOUT}}$ $\overline{\text{EOM}}$	4 57
RT Address Mismatch	Command RTU Address ≠ Status Word RTU Address	$\overline{\text{STATERR}}$	68
Error Flag(s) Set	Status Word Response from RT: Error Condition	$\overline{\text{STATERR}}$	68
Broadcast Received bit Set	Response to Transmit Status Word mode command may allow this, all others ERROR.	Broadcast Mask not set (See BC Control Word) $\overline{\text{STATERR}}$	68
DATA WORD Handshake Failure Transmit Command Receive Command	 No subsystem response to Bus Request. Data lost: Word Count fails. 1553 transmission gap.	 BC waits for Grant. $\overline{\text{MSGERR}}$ Status Word response: $\overline{\text{STATERR}}$	 30 68
Data Received from RTU Less than word count Greater than word count	 Transmit Command (RTU response) More data received than requested.	 $\overline{\text{MSGERR}}$ and $\overline{\text{EOM}}$ $\overline{\text{MSGERR}}$ and $\overline{\text{EOM}}$	 4 30
Data after Status Set (all extra words)	Transmit Command: data words received after status to subsystem.	DMA/memory write (for each)	-
FORMAT ERROR	-	$\overline{\text{MSGERR}}$	30

Notes:
(1) $\overline{\text{LOOPERR}}$ is a .5μS pulse which occurs near DMA handshake for loop back word.
(2) $\overline{\text{TIMEOUT}}$ is a 40/160nS pulse which occurs 19.5μS ±0.5μS after the mid-bit parity of the last word onto the bus.
(3) $\overline{\text{STATERR}}$ is a 120/166nS pulse which occurs during the status word DMA handshake.
(4) $\overline{\text{MSGRR}}$ is a 40/160nS pulse which occurs approximately 100nS before INCMD goes high. It is triggered by NODT going inactive (i.e., low word count).

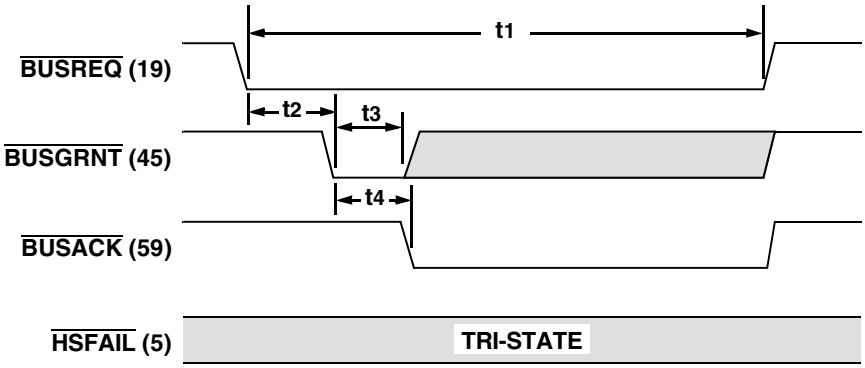
Table 4 – BC Error Handling

RTU Response
The addressed RTU(s) must respond (to non-broadcast commands) within a timeout period as shown in Figures 7, 8, and 9. Figures 10 and 11 illustrate the BC Mode Code Timing. Status and data words received from the 1553 port are transferred to the subsystem via a handshake and memory write operation for each (See Message Length Checking).

BC Status/Error Handling
Message transfer errors are indicated using the $\overline{\text{TIMEOUT}}$, $\overline{\text{MSGERR}}$, $\overline{\text{LOOPERR}}$ and $\overline{\text{STATERR}}$ BC status outputs (pins 4, 30, 46 and 68 respectively). Additional error detection methods include user evaluation of status, data and (long) loop words and/or use of the 1553B dual redundant mode codes. Note that certain error conditions not reflected in the current Status Word (SW) can occur; Broadcast CMD RT-status and post RT status response may be accessed via the Transmit Status Word mode command.

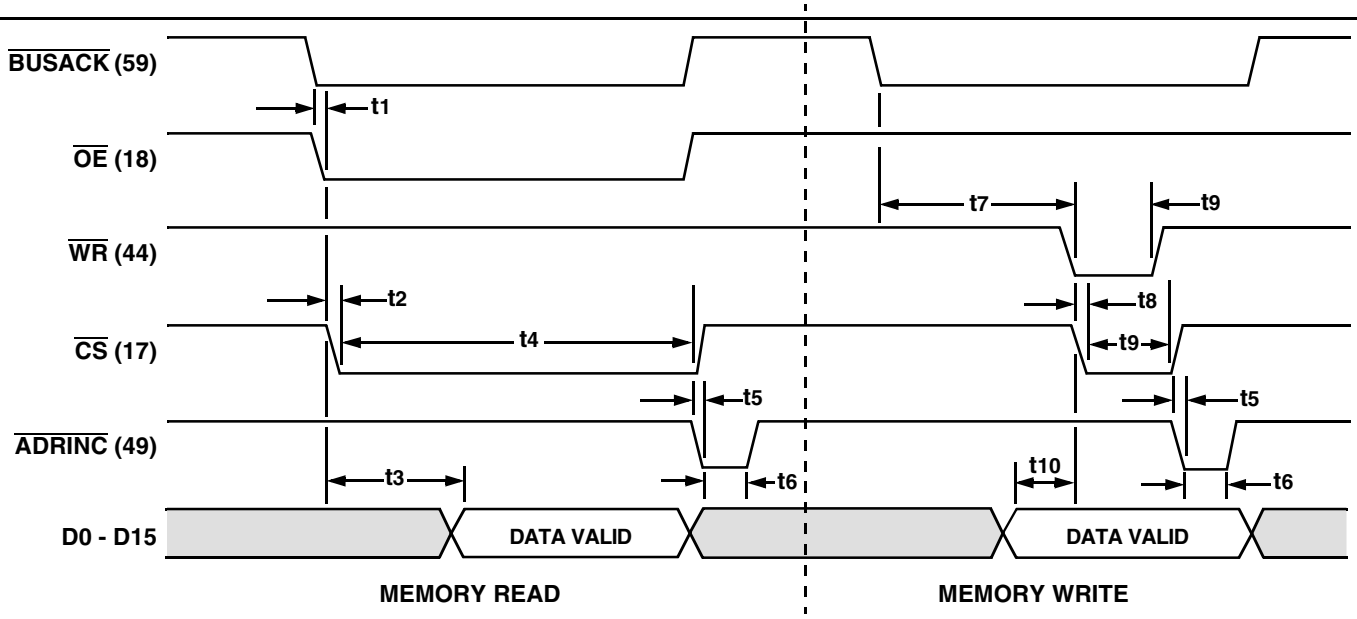
Transmit Bit Word. Additional status informa tion is generated by an RTU (CT2565 for each transfer in the form of a BIT word). This word may be accessed by the BC using the TRANSMIT B-I-T WORD mode command. See RTU Error Handling and Mode Code sections).

Message Length Checking. The BC stores the command word, word-count field in an internal register. By decrementing this register following each data word transfer (See BC Memory Read/Write Timing), the BC can detect an incorrect message length.
For a description of the possible BC error, indicators occurring during each stage of message transfer read from left to right in Table 4. For a description of the possible causes of errors within a transfer, read from right to left.



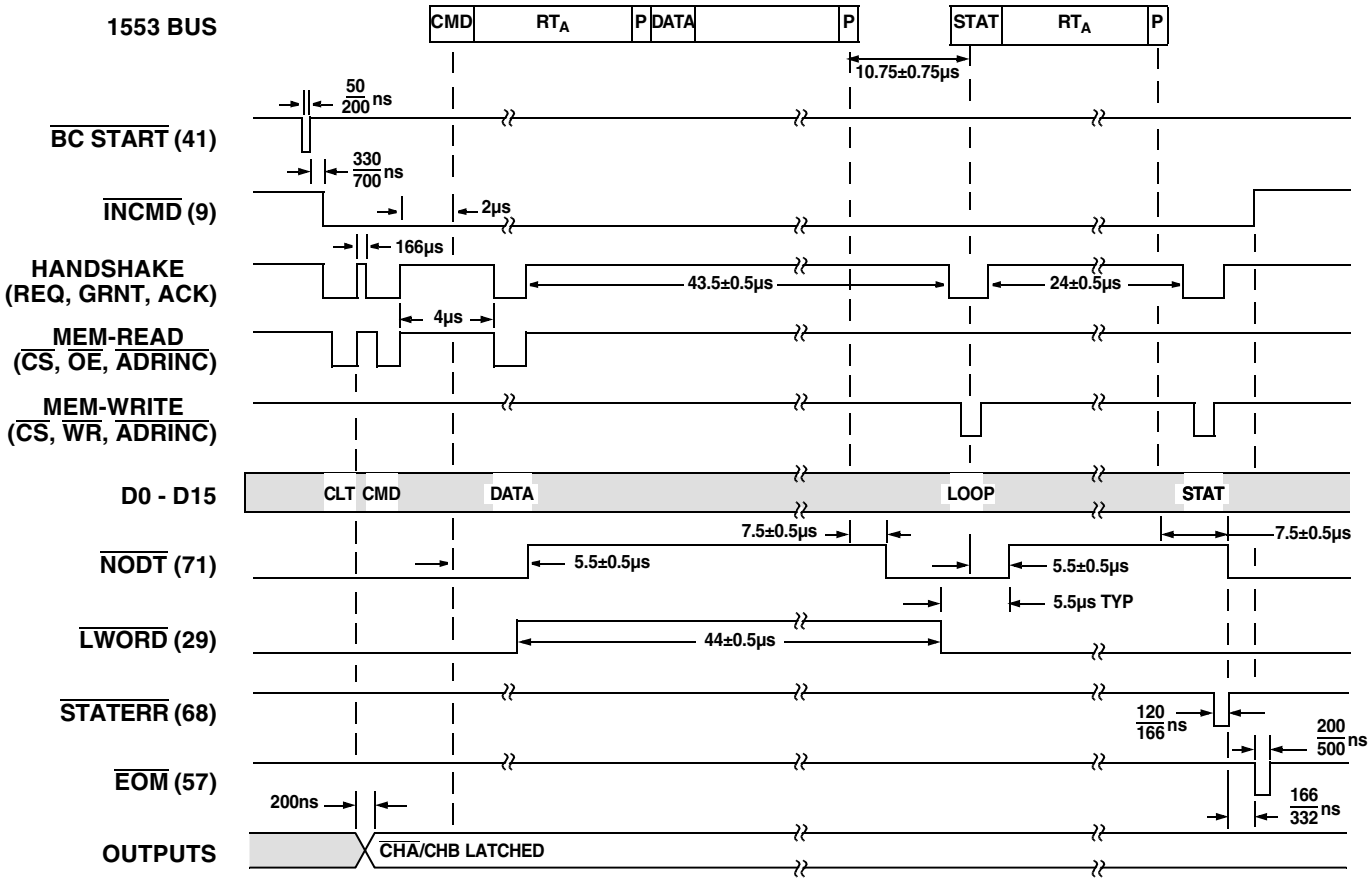
SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t1	$\overline{\text{BUSREQ}}$ pulse width	867	1667	ns
t2	$\overline{\text{BUSREQ}}$ to $\overline{\text{BUSGRNT}}$ delay	0	800	ns
t3	$\overline{\text{BUSGRNT}}$ pulse width	166	-	ns
t4	$\overline{\text{BUSGRNT}}$ to $\overline{\text{BUSACK}}$ delay	50	200	ns

Figure 5 – BC Handshake Timing



CYCLE	SYMBOL	DESCRIPTION	MIN	MAX	UNITS
Read	t1	$\overline{\text{BUSACK}}$ to $\overline{\text{OE}}$ delay	-	25	ns
	t2	$\overline{\text{OE}}$ to $\overline{\text{CS}}$ delay	-	25	ns
	t3	Data setup time	-	250	ns
	t4	$\overline{\text{CS}}$ ($\overline{\text{OE}}$) pulse width	650	680	ns
	t5	$\overline{\text{CS}}$ to $\overline{\text{ADRINC}}$ delay	-	25	ns
	t6	$\overline{\text{ADRINC}}$ pulse width	80	166	ns
Write	t7	$\overline{\text{BUSACK}}$ to $\overline{\text{WR}}$ delay	-	378	ns
	t8	$\overline{\text{WR}}$ to $\overline{\text{CS}}$ delay	-	25	ns
	t9	$\overline{\text{CS}}$ and $\overline{\text{WR}}$ pulse width	150	175	ns
	t10	Data valid setup	100	-	ns

Figure 6 – BC Read/Write Timing



Notes for Figures 7-9
T/R and HSFAIL are static at logic "1" in BC mode. All timing is typical unless otherwise noted.

Figure 7 – BC Receive One Word Command Timing

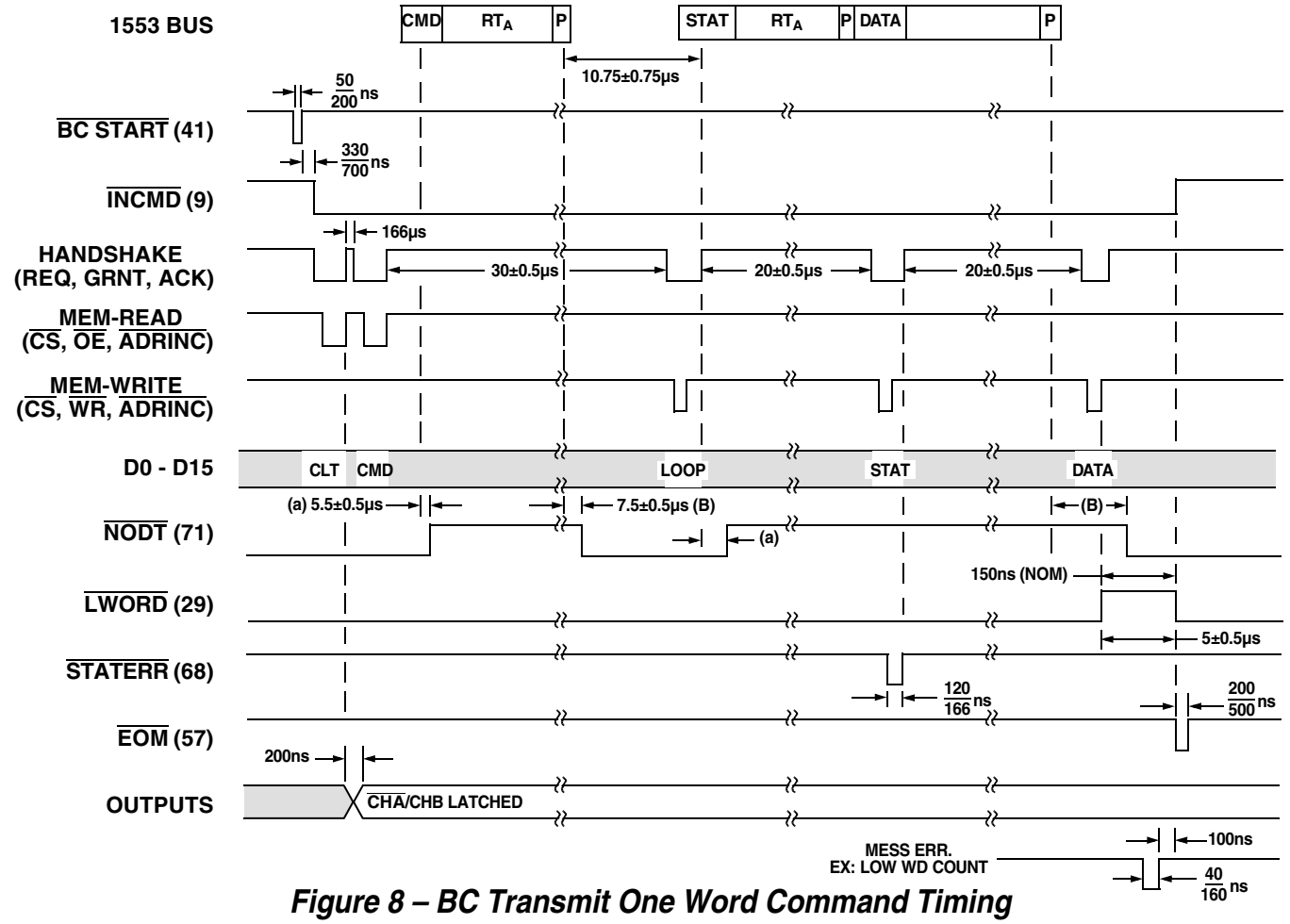


Figure 8 – BC Transmit One Word Command Timing

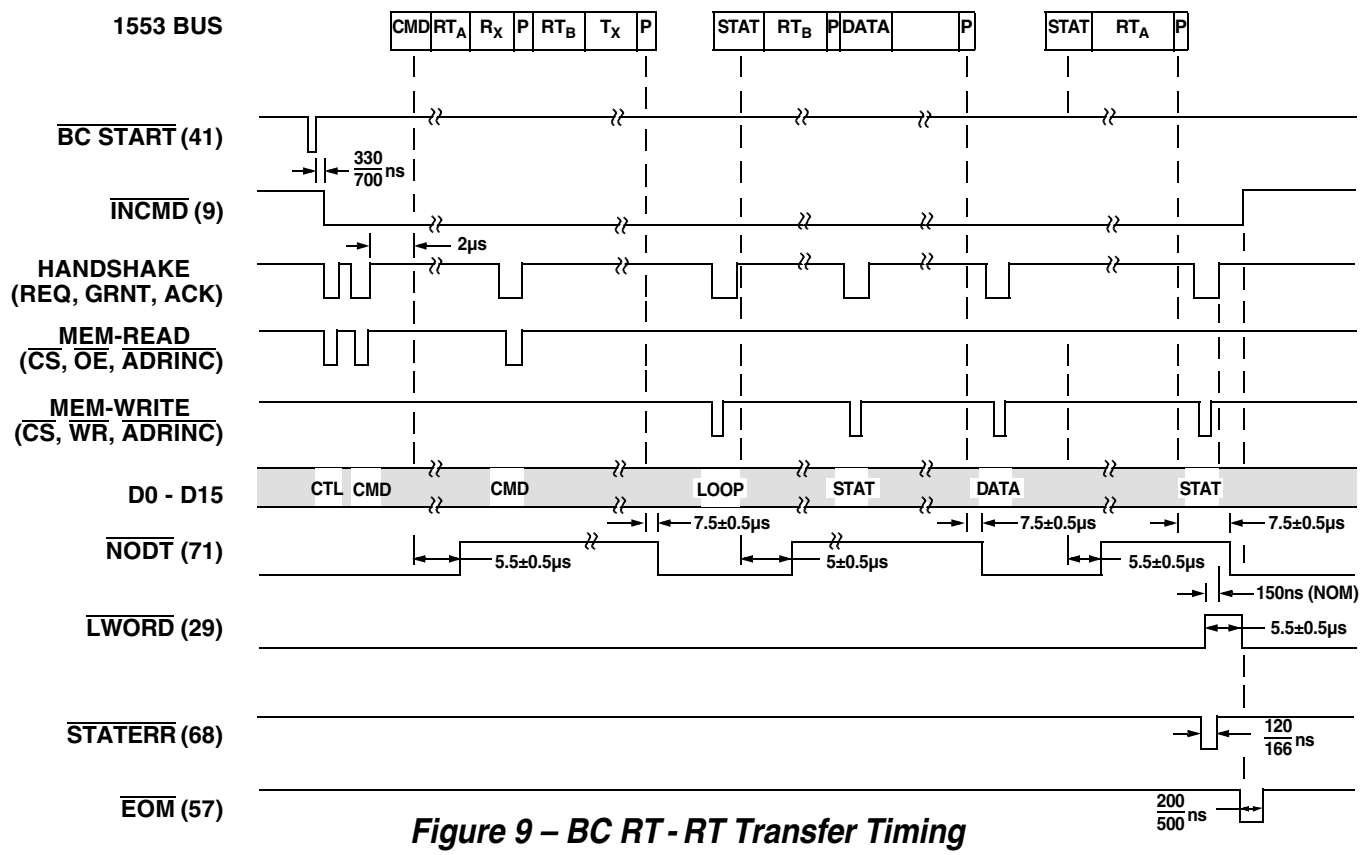


Figure 9 – BC RT - RT Transfer Timing

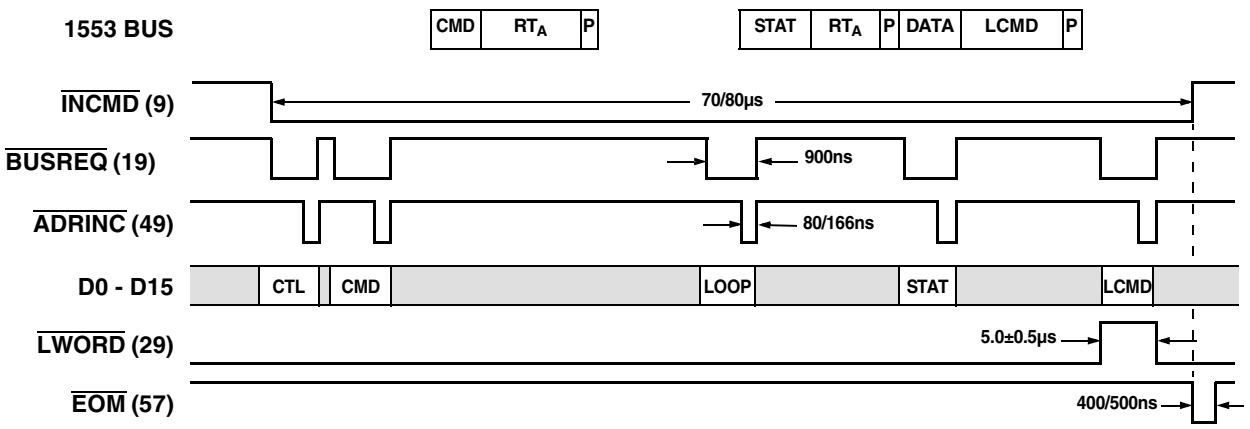
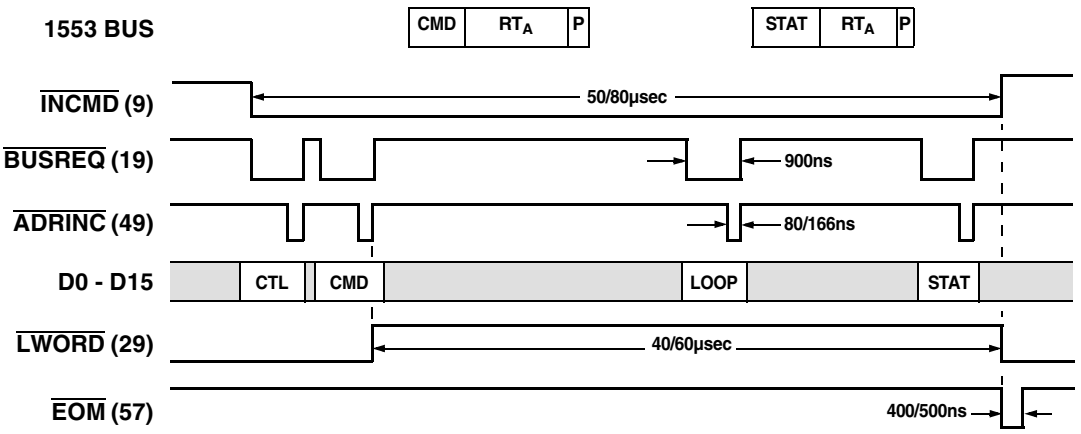


Figure 10 – BC Mode Code Transmit Last Command (10010) Timing



Notes:
All timing is typical unless otherwise noted.

Figure 11 – BC Mode Code Transmit Status Word (00010) Timing

RTU Operation

Each RTU is assigned a unique address on the 1553 bus. It processes commands issued by the BC to its address or through Broadcast commands.

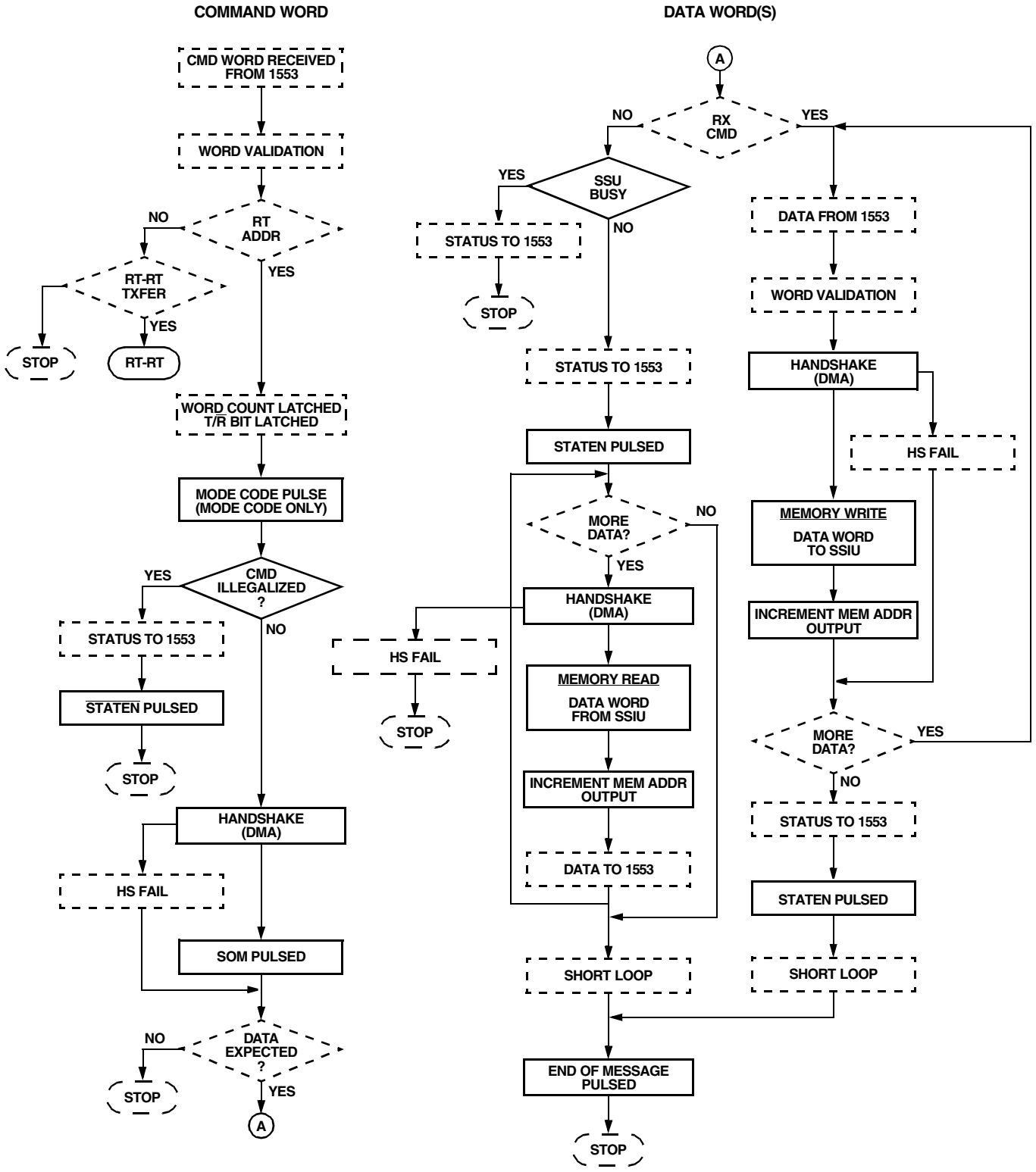
Upon receipt of a valid command in the RTU mode, the CT2565 will attempt to (1) transfer 1553 data received to the subsystem, (2) read data from the subsystem for transmission on the 1553 bus, (3) transmit status information to 1553, or (4) set status conditions. All data block transfers are accompanied by a 1553 Status Word. Figure 12 details a RTU single message transfer.

RTU Address

RTU Address pins 33-34 and 72-74 and Address Parity pin (odd parity) should be programmed to a unique RTU (1553) address. These inputs have internal pull-ups and will default a high state if left unconnected. The CT2565 will not respond if odd parity is compromised (See Error Handling).

RTU Initialization

Initialize the CT2565 as an RTU per Table 2. Upon receipt of valid command word from the serial bus (RTU addressed or broadcast CMD), the CT2565 will pulse $\overline{\text{NBGRNT}}$ (New Bus Grant) pin 42 low.



Notes:
(1) Steps marked with " _ _ _" indicates operation is transparent to user.
(2) Steps marked with " ___" indicates user interaction required.

Figure 12 – RTU Single Message Transfer Flow Diagram

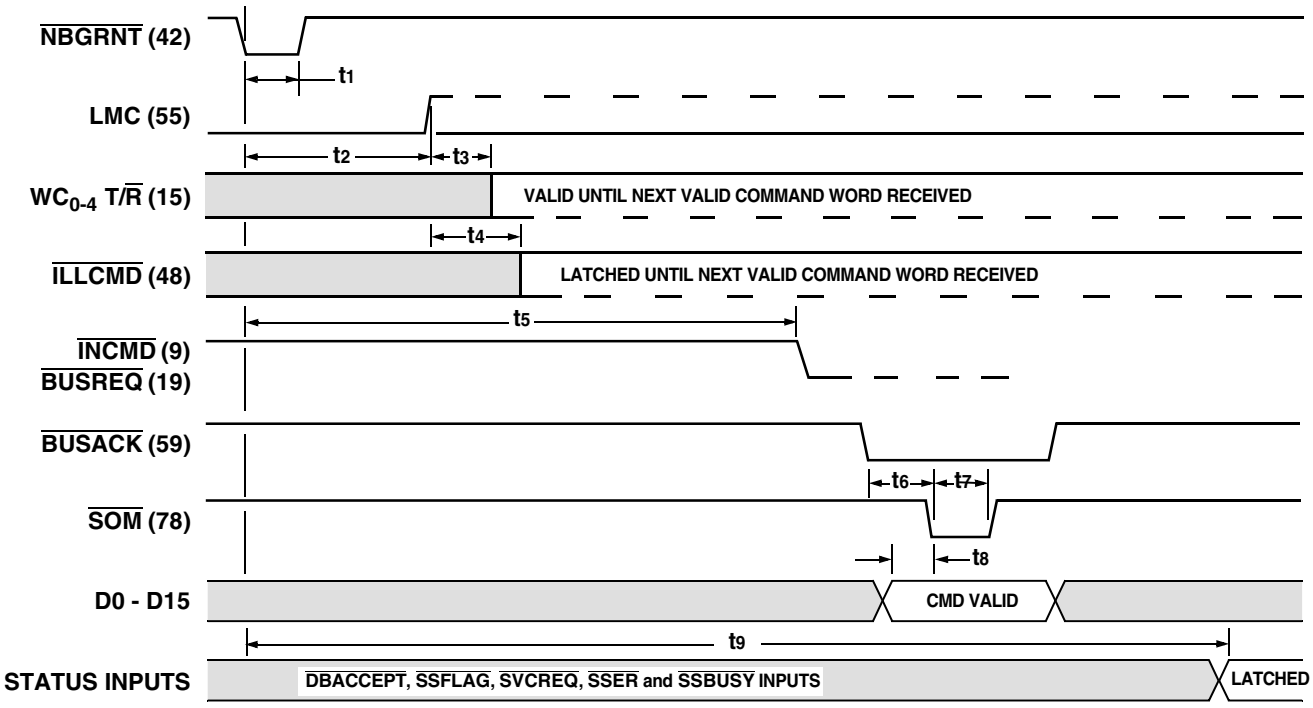
Mode Code Illegalization (Optional)

The word count and TX/$\overline{RX}$ pins will be latched 800ns (typ) after the falling edge of $\overline{NBGRNT}$ (See Figure 13, RTU Command Word Handling). Table 5 lists the CT2565 pins associated with mode code illegalization. If the current command is a mode code, LMC (pin 55) will go high. Mode codes can be illegalized, using an external PROM (<200ns access time recommended), by setting $\overline{ILLCMD}$ low after the $\overline{NBGRNT}$ flag. This will set the message error (status word) and illegal Mode Code (BIT word) bits followed by transmission of the status word. Using the method, mode commands can be "auto-screened" without interrupting subsystem operation. For a complete list of mode codes, refer to Table 8.

Table 5 – Mode Code Illegalization

PIN #	SYMBOL	DESCRIPTION
51	WC0	Word Count LSB
12	WC1	Word Count 1
52	WC2	Word Count 2
13	WC3	Word Count 3
53	WC4	Word Count MSB
15	T/$\overline{R}$	TX/$\overline{RX}$

Note: A word count field of all 0's indicates 32 data words; all 1's = 31 words.



	SYM	DESCRIPTION	MIN	TYP	MAX	UNITS
Illegalize	t1	$\overline{NBGRNT}$ pulse width	151	-	181	ns
	t2	$\overline{NBGRNT}$ to LMC delay	500	-	667	ns
	t3	LMC to WC-T/$\overline{R}$ latch	-	200	-	ns
	t4	LMC to ILLCMD latch	-	-	333	ns
Legal	t5	$\overline{NBGRNT}$ to $\overline{INCMD}$ delay	-	1.0	1.5	µs
	t6	$\overline{BUSACK}$ to $\overline{SOM}$ delay	-	166	-	ns
	t7	$\overline{SOM}$ pulse width	-	166	-	ns
	t8	CMD VALID setup	60	-	100	ns
Status Inputs	t9	$\overline{NBGRNT}$ low to status latch	-	-	3	µs

Note: Memory read/write signals $\overline{CS}$, $\overline{OE}$, and $\overline{ADRINC}$ remain static at logic "1".

Figure 13 – RTU Command Word Handling/Status Inputs

RTU Commands

A command word transfer will be initiated by the CT2565 after the rising edge of NBGRNT (See Figure 14). In order to allow the command word to be stored in user-defined memory space (separate from data), no memory write operation (CS, WR, ADRINC outputs) will be initiated following the usual DMA-type handshake; a Start Of Message (pin 78: SOM low) pulse indicates that the CMD word is currently valid on the data bus. Note that commands are named from the BC point-of-view (i.e., a TRANSMIT CMD dictates that the addressed RTU must transmit data).

Transmit CMD (RT-BC)

If the subsystem is available (pin 47: SSBUSY high): following transmission of the status word, the CT2565 will initiate a handshake/memory-read respectively for the total number of (data) words defined by the Command Word-word count field. Figure 15 shows the RTU Read/Write Timing. Note that possible data word transfer and short-loop test errors will be reflected in the following status word/bit word. A low on the SSBUSY input will set the corresponding status word flag, and no data transfer will be requested (BUSREQ low) following transmission of the status word.

Receive CMD (BC-RT). A DMA handshake will be initiated for each word received over the 1553 data bus (See Figure 16). If successful, the respective handshake will be followed by a corresponding memory write. Transfer errors such as handshake timeout or SS BUSY will not terminate transfer attempts for the remaining data words, error flagging or status word transmission.

RTU(b)-RTU(a) (Transmit/Receive). An RT-RT transfer will appear to both RTU subsystems as a standard transmit or receive command except: (1) transmission of the data block will not be continuous with that of the receive CMD, and, (2) upon detection of a command-sync field following the receive CMD, RTU(a) will recognize an RT-RT transfer and store the transmit CMD-address field for comparison with the address field of the following (RTU(b) status) word (See Figures 17 and 18). If a mismatch is detected, RTU(a) will issue a message error. The transmitting RTU will respond as in an RT-BC Transmit CMD.

RTU Status/Error Handling

Message transfer errors are indicated using the TIMEOUT, HSFAIL, MSGERR and LOOPERR RTU-status outputs (pins 4, 5, 30 and 46 respectively). Additional error detection mechanisms available include status input manipulation (below) and evaluation of the status and BIT words (See BIT Word).

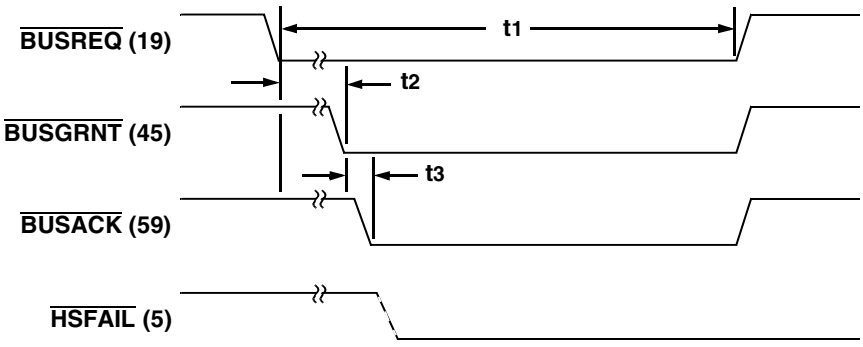
Table 6 describes error handling mechanisms related to each stage in a message transfer (reading left to right) as well as noting errors associated with a specific CT2565 status output (reading right to left).

Short Loop Test. The last word to be transmitted in a given message transfer (Status word, BIT word or Data word) is stored in a CT2565 internal register. As this word is transmitted to the 1553 bus, it is "looped back" through the active receiver channel for auto-RTU, "SHORTLOOP" verification. A LOOPERR low pulse indicates a mismatch between the stored and looped words. Note that short loop testing is initiated for all RTU transfers except a Broadcast transfer.

TRANSFER/CONDITION	DESCRIPTION	ERROR SIGNAL	PIN
COMMAND WORD			
Invalid Word Format	Sync, bit count invalid.	None; input ignored	-
Invalid Command (format error)	Operation disagreement (e.g. Broadcast and Transmit bits set)	MSGERR (also; SW bit)	30
Handshake Failure	BUSREQ to BUSGRNT timeout	HSFAIL, suppress SOM, continue	5 78
Illegal Mode Command	Subsystem set ILLCMD (pin 48).	SW message error bit set	
RT-RT Transfer			
Response Timeout	(Transmit) Command to Status Word time.	TIMEOUT (transmitting RT) (also; MSGERR bit)	4
Address mismatch	Transmit Command Address ≠ Status Word address.	MSGERR (Receiving RT) (also; MSGERR bit)	30
DATA WORD			
Handshake Failure	BUSREQ to BUSGRNT timeout	HSFAIL (1)	5
Transmit Command	(Continue)	Continue message transfer	
Receive Command	(Message terminated)	INCMD high, EOM	9,57
Number Transmitted (2)	Low data word-count received.	MSGERR (3) (SW bit)	30
	High data word count	MSGERR after validation (no transfer) SW and BIT-Word also set.	30
LOOP WORD	Looped back through receiver.		
Short Loop	Received word ≠ to last xmitted 1553 word.	LOOPER (also sets Ter-Flag bit).	46
Long Loop	(BC only)		

Notes:
(1) The HSFAIL low output is reset (high) at the start of the next message transfer (NBGRNT low).
(2) The subsystem can use the status input pins (SW) to report incorrect word count type errors.
(3) MSGERR set 7.5µS after last mid parity bit of last data word.

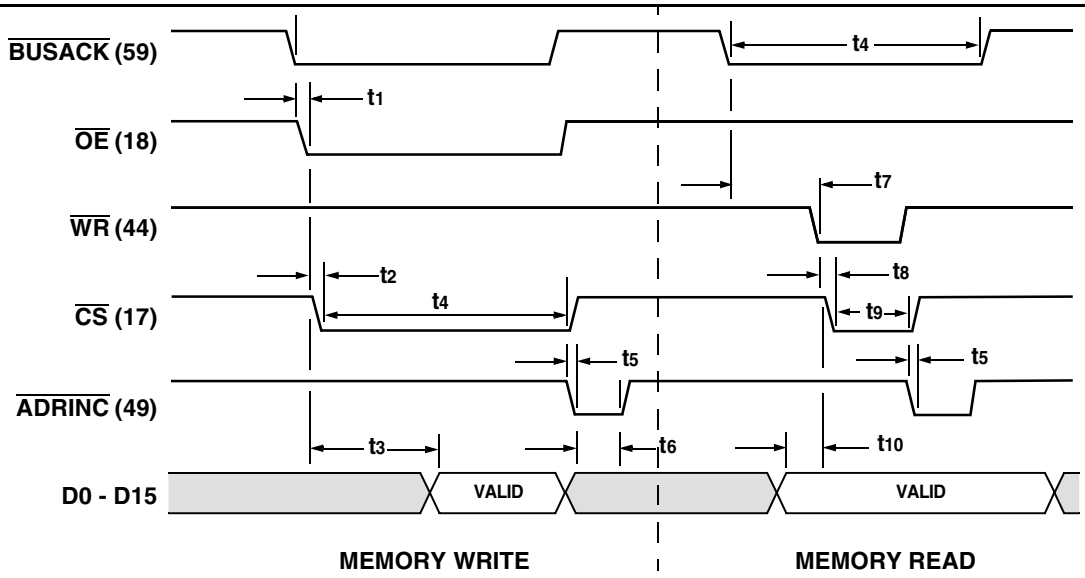
Table 6 – RTU Error Handling



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t1	$\overline{\text{BUSREQ}}$ pulse width	667	-	ns
t2	$\overline{\text{BUSGRNT}}$ delay			
	CMD WORD	0	1.5	µs
	TX DATA WORD	0	15.5	µs
	RX DATA	0	2.33	µs
t3	$\overline{\text{BUSGRNT}}$ to $\overline{\text{BUSACK}}$ delay	40	166	ns

Note: $\overline{\text{HSFAIL}}$ will go low following a $\overline{\text{BUSREQ}}$ to $\overline{\text{BUSGRNT}}$ timeout.

Figure 14 – RTU Handshake Timing



CYCLE	SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
Read	t1	$\overline{\text{BUSACK}}$ to $\overline{\text{OE}}$ delay	-	-	25	ns
	t2	$\overline{\text{OE}}$ to $\overline{\text{CS}}$ delay	-	-	25	ns
	t3	Data setup time	-	-	250	ns
	t4	$\overline{\text{CS}}$, $\overline{\text{OE}}$ and $\overline{\text{BUSACK}}$ pulse width	-	500	-	ns
	t5	$\overline{\text{CS}}$ to $\overline{\text{ADRINC}}$ delay	-	-	25	ns
	t6	$\overline{\text{ADRINC}}$ pulse width	80	-	166	ns
Write	t7	$\overline{\text{BUSACK}}$ to $\overline{\text{CS}}$ delay	-	-	225	ns
	t8	$\overline{\text{WR}}$ to $\overline{\text{CS}}$ delay	-	-	25	ns
	t9	$\overline{\text{CS}}$ and $\overline{\text{WR}}$ pulse width	150	166	180	ns
	t10	Data valid setup prior to leading edge of $\overline{\text{WR}}$	60	-	100	ns

Figure 15 – RTU Read/Write Timing

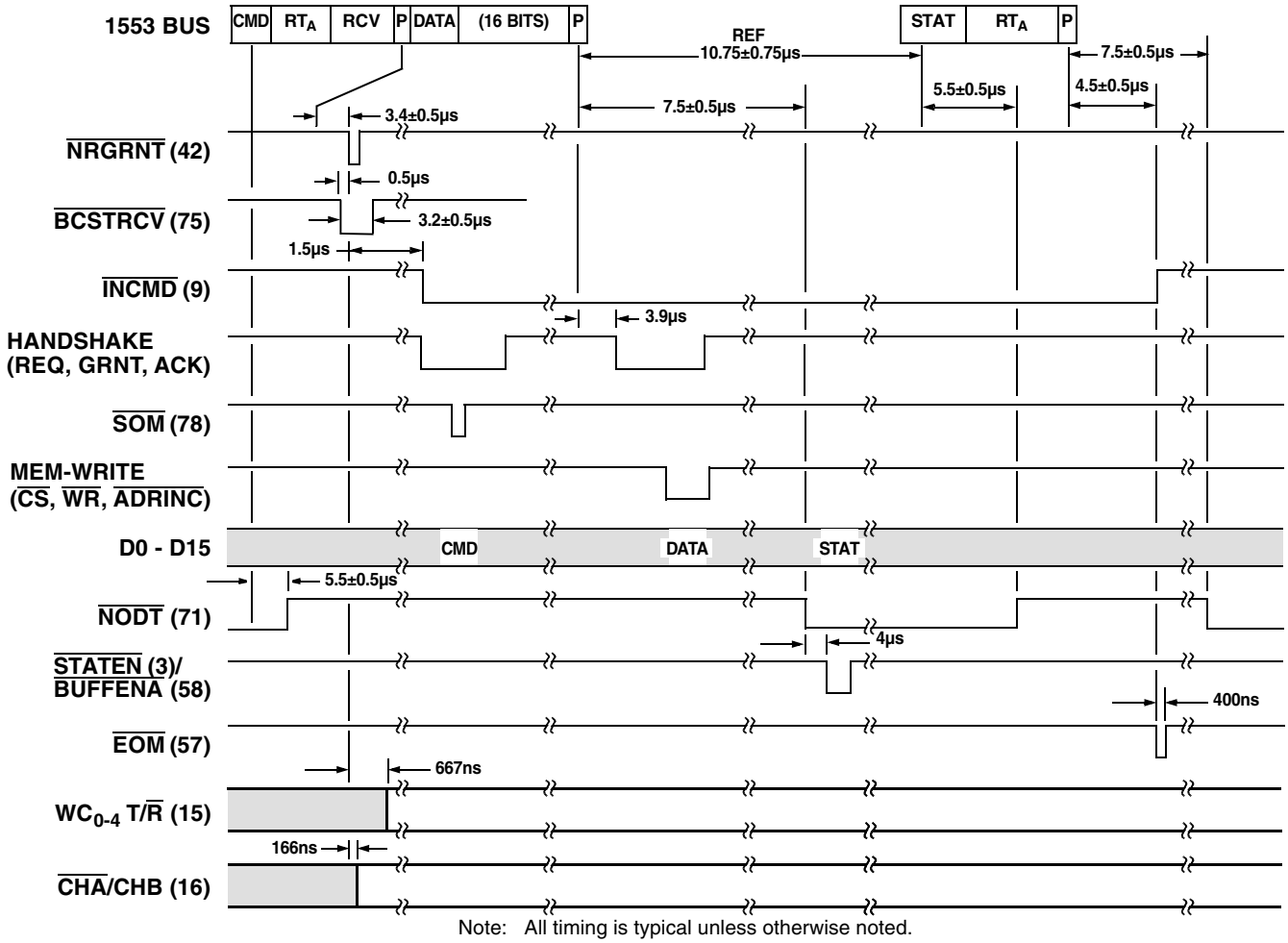
Use of Status Word
The status word may be captured by the subsystem as it is transmitted to the 1553 port by pulsing BUFENA (pin 58) low during $\overline{\text{STATEN}}$ (pin 3: 520ns low pulse). Data becomes valid approximately 50ns after the falling edge of $\overline{\text{BUFENA}}$. This corresponds with all non-broadcast message transfers and the TRANSMIT STATUS WORD mode command. Note that the status word may be transmitted prior to an error condition (See Transmit CMD). These conditions will be indicated in the "next" status word and may be monitored if the BC requests the SW before it is altered (See Mode Commands).

Subsystem Control
The CT2565 allows the subsystem total control over the status word flags using the inputs indicated in Table 7.

BIT Word
The BIT Word (Built-In-Test) becomes available in response to a TRANSMIT BIT WORD mode command and provides additional status information (See Figure 19) to that provided by the status word. The subsystem may capture the BIT word on the parallel data bus by pulsing $\overline{\text{BUFENA}}$ (pin 58) low during $\overline{\text{BITEN}}$ (pin 43: approximately 520ns low pulse). Data Becomes valid approximately 50ns after the falling edge of $\overline{\text{BUFENA}}$. Like the status word, the BIT word cannot be altered by the subsystem.

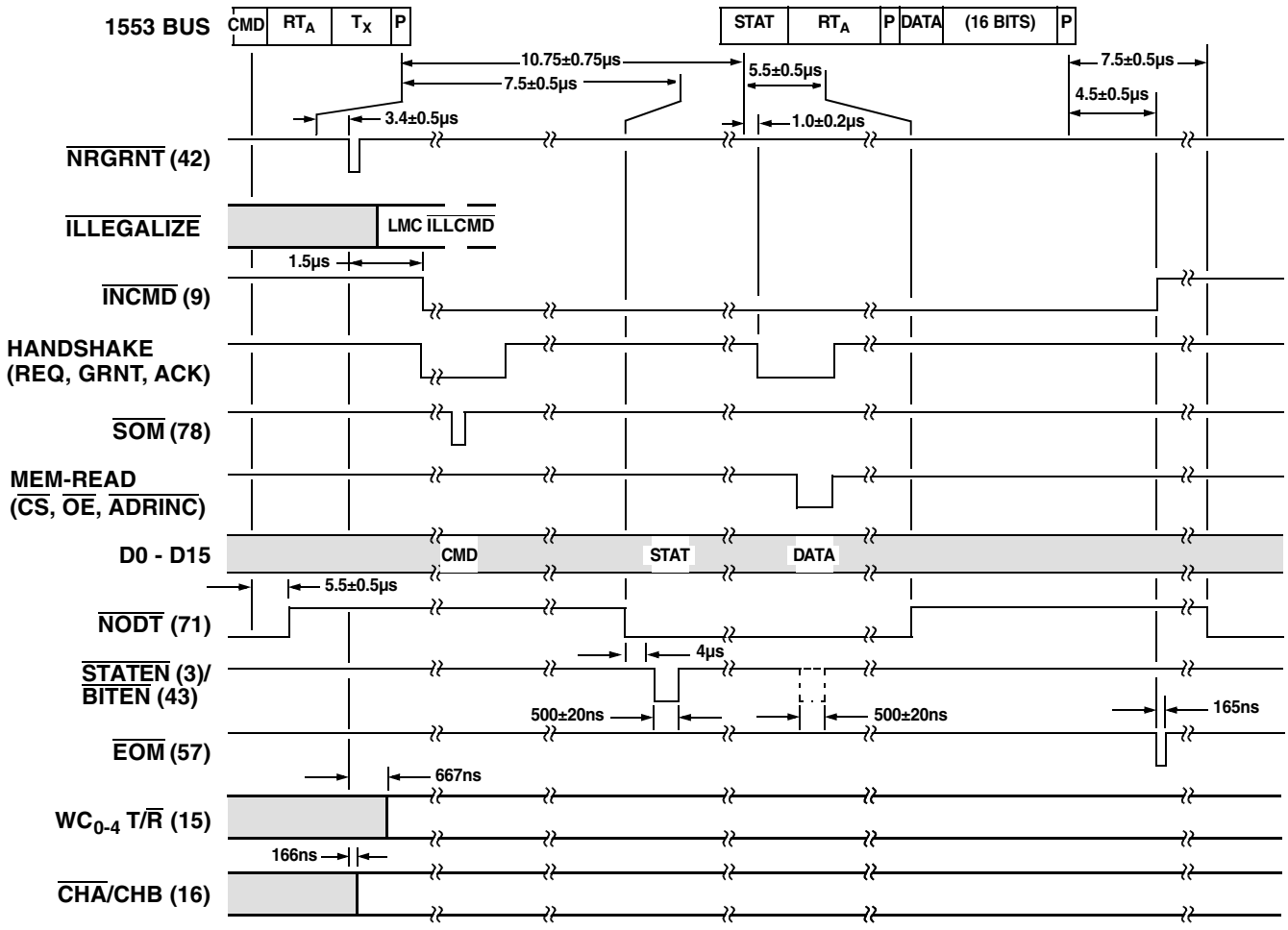
PIN #	SYMBOL	DESCRIPTION
6	DBACCEPT	RT accepts BC operation responsibility (See Table 2).
7	SSFLAG	Transmitted data may be invalid sets SSFLAG bit.
8	SVCREQ	Service Request; see Transmit Vector mode command.
10	SSER	RTU fault exists: sets TERMINAL FLAG bit.
47	SSBUSY	Subsystem cannot service 1553 request at this time.
48	ILLCMD	Mode command subsystem illegalization: Sets MSGERR bit, doesn't suppress status word.

Table 7 – Subsystem Control of RT-Status



Note: All timing is typical unless otherwise noted.

Figure 16 – RT Receive Command Timing



Notes:
(1) All timing is typical unless otherwise noted.
(2) BITEN only occurs when XMIT BIT WD mode code command is received
(Handshake and read/write signals are not generated in this case).

Figure 17 – RT Transmit Command Timing

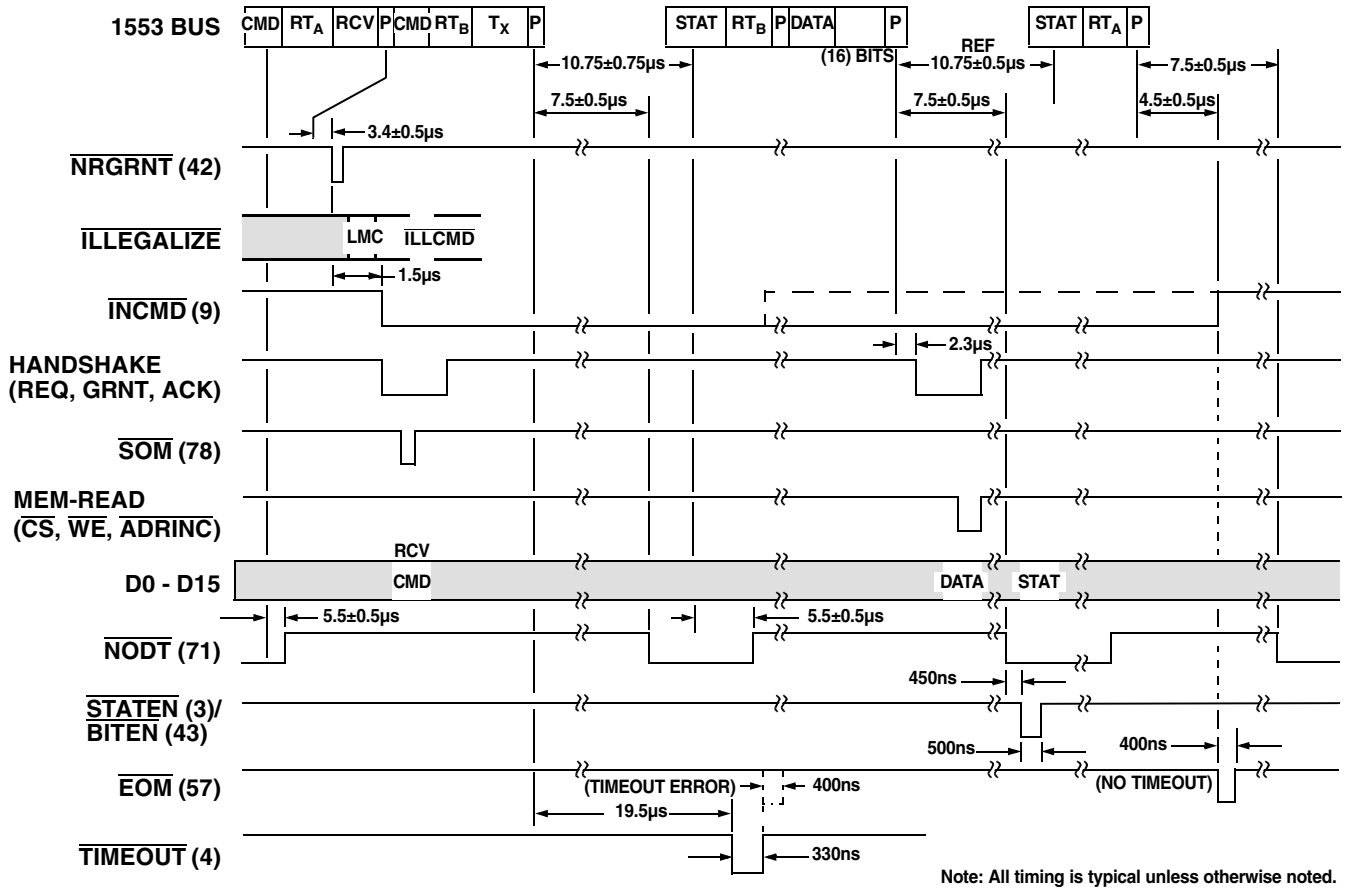
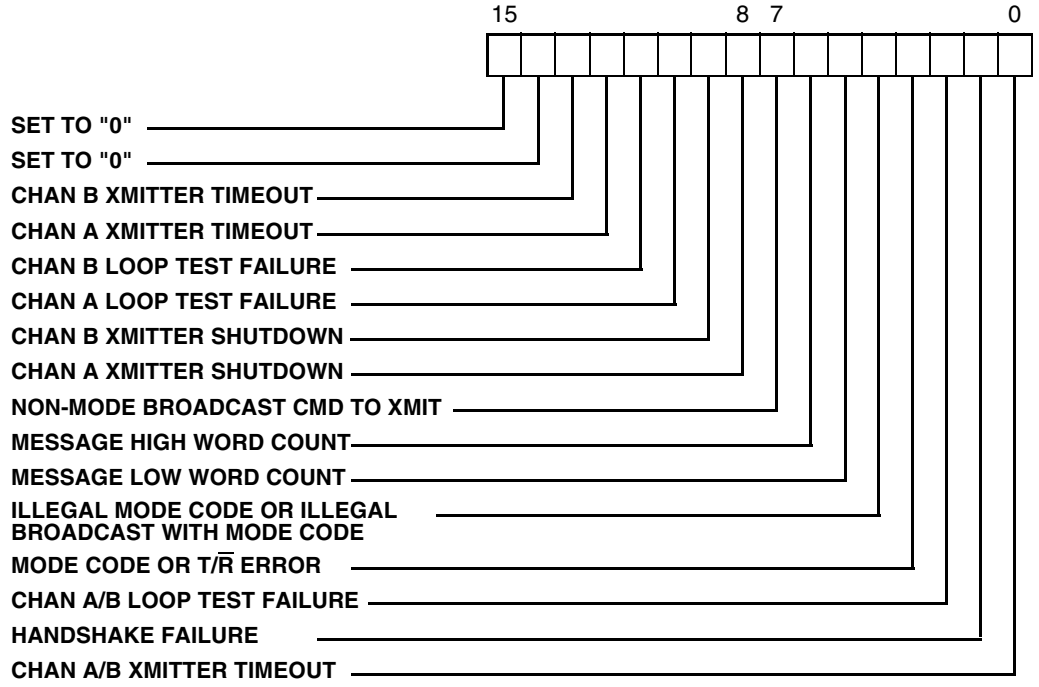


Figure 18 – RT-RT Transfer Timing



Notes:
(1) Bits 0-2 and 10-13 are latched and only cleared by a mode reset command or a master RESET.
(2) Bits 3-7 are cleared at the start of each new message and updated at the end of the message. They reflect the present command word.
(3) Bits 8-9 are set by the mode command for Transmitter Shutdown and are cleared by the mode command for Override Transmitter Shutdown, Reset RT or a master RESET.

Figure 19 – Bit Word

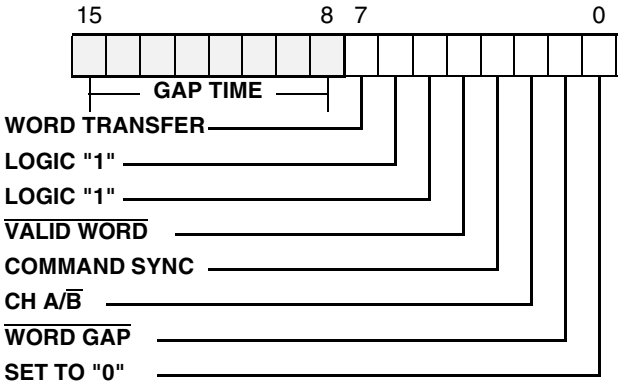
MT Operation

In the MT mode, the CT2565 captures all valid transmissions on both channels of the 1553 bus, allowing the user to monitor bus activity. Each word is transferred to the subsystem along with an identification for interpretation of the 1553 data stream.

MT Initialization

Initialize the CT2565 for MT operation per Table 2. The CT2565 will remain in an idle state until $\overline{\text{BCSTART}}$ (pin 41) is pulsed low. Figure 21 illustrates MT operation.

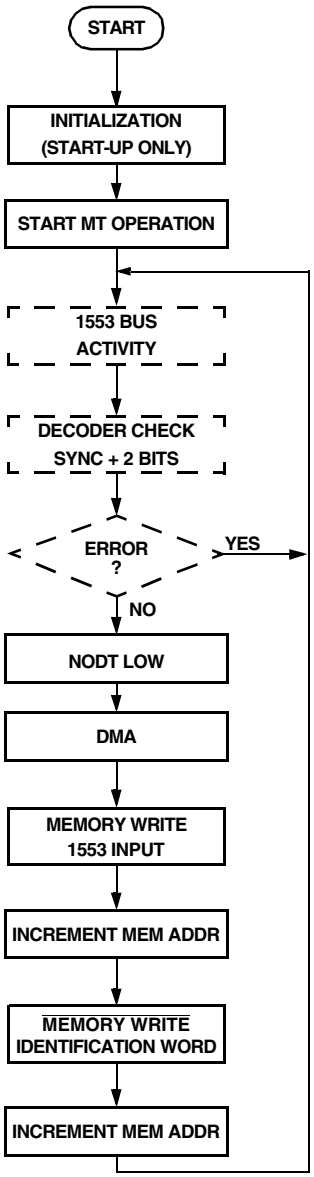
Valid words received by the CT2565 are transferred to the subsystem along with an identification Word by a single DMA handshake with two memory-write operations shown in Figure 22, MT Transfer Timing. Since the decoder will reject words based on sync field errors and/or errors in the first 2 non-sync bits, these words will not be processed further (i.e., the subsystem will receive no indication of the receipt of this word).



NAME	Definition
GAP TIME	$\overline{\text{NODT}}$ low time. 2MHz Clock allows 500ns increments to 128µs (remains static at FF on overflow).
WORD TRANSFER	Logic "1" indicates successful transfer to subsystem.
WORD TRANSFERRED	Indicates successful transfer (See bit 7)
$\overline{\text{VALID WORD}}$	Reset (1) indicates Manchester error, Parity error, Low Bit Count and/or Status sync field.
COMMAND SYNC	Logic "1" indicates Command or Status sync field. Logic "0" indicates data sync.
CHAN A/$\overline{\text{B}}$	Logic "1" if word received on 1553 bus Channel B.
$\overline{\text{WORD GAP}}$	Set (0) if current word was received at least 2µs after receipt of previous word (parity to mid-sync).

Note: Subsystem should clear entire memory prior to start of MT operation.

Figure 20 – Identification Word



Notes:
(1) Steps marked with " _ _ _" indicates operation is transparent to user.
(2) Steps marked with " ___" indicates user interaction required.

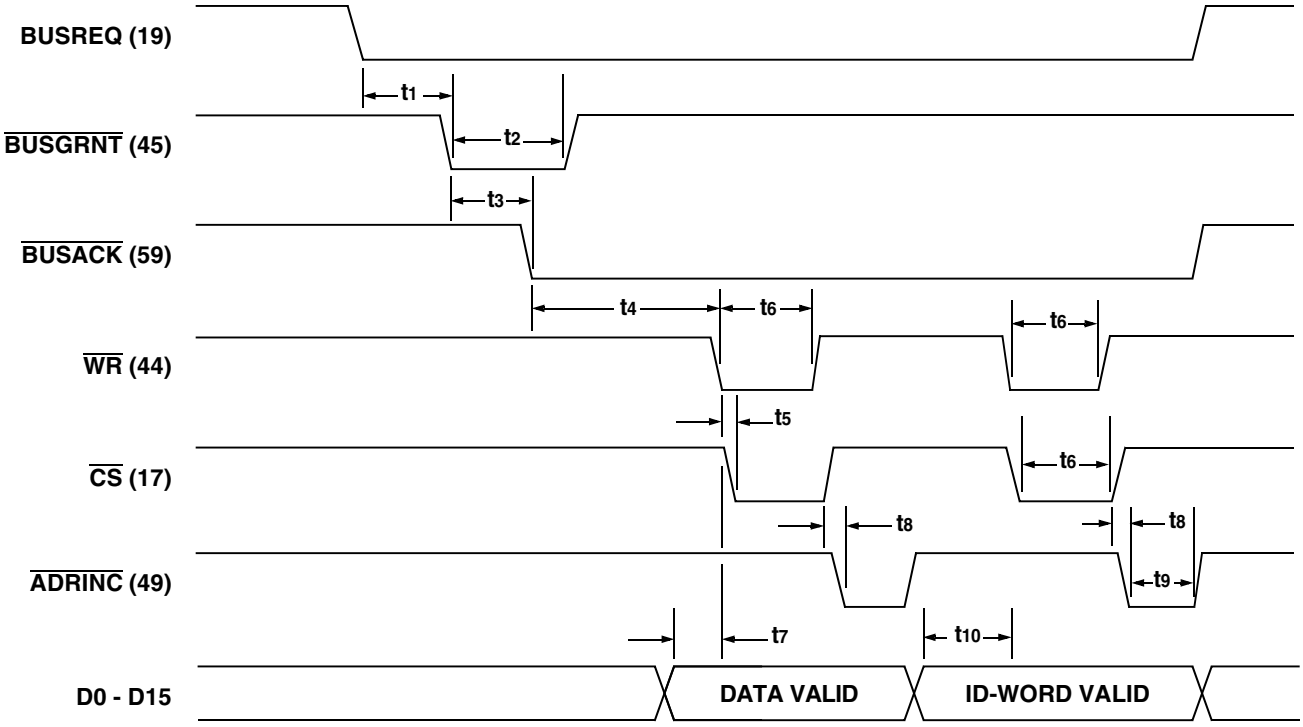
Figure 21 – MT Operation Flow Chart

Simultaneous Transmission
Transmissions appearing simultaneously on alternate 1553-bus channels will be captured by CT2565 sequentially providing that each BUSREQ is answered by the subsystem with a BUSGRNT within the handshake timeout period.

RESET Signal
Pulsing RESET low will suspend MT operation by (1) INCMD goes high (EOM goes low on the rising edge) and (2) the CT2565 enters an idle state. MT operation may be restored by pulsing BCSTART low (above) or another mode of operation may be selected (See Table 2).

Handshake Failure
Note that a handshake failure will abort the current transfer. Monitoring will resume upon receipt of a valid word on the 1553 bus.

MODE CODES
Nine of the 13 available, dual redundant mode codes are handled by the CT2565 without user intervention. Of the four remaining codes, Dynamic Bus Control and Synchronize (no data) require subsystem notification. The remaining two mode codes, Transmit Vector Word and Synchronize (with data) involve data transfer with the subsystem. Mode command illegalization and handling are detailed in the RTU Operation section and listed in Table 8.



CYCLE	SYM	DESCRIPTION	MIN	TYP	MAX	UNITS
Handshake	t1	$\overline{\text{BUSREQ}}$ to $\overline{\text{BUSGRNT}}$ delay	0	-	800	ns
	t2	$\overline{\text{BUSGRNT}}$ pulse width	166	-	-	ns
	t3	$\overline{\text{BUSGRNT}}$ to $\overline{\text{BUSACK}}$ delay	?	-	?	ns
Write Only	t4	$\overline{\text{BUSACK}}$ to $\overline{\text{WR}}$ delay	320	330	370	ns
	t5	$\overline{\text{WR}}$ to $\overline{\text{CS}}$ time	-	-	25	ns
	t6	$\overline{\text{WR}}$ and $\overline{\text{CS}}$ pulse width	150	166	175	ns
	t7	DATA VALID setup	-	-	50	ns
	t8	$\overline{\text{CS}}$ to $\overline{\text{ADRINC}}$ delay	-	-	25	ns
	t9	$\overline{\text{ARINC}}$ pulse width	80	-	166	ns
	t10	ID WORD VALID setup	-	-	100	ns

Figure 22 – MT Transfer Timing

DYNAMIC BUS CONTROL (00000)

MESSAGE SEQUENCE = DBC * STATUS

The CT2565 responds with status. If the subsystem wants control of the bus, it must set DBACC within 2.5us after NBGRT.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (Bit Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

SYNCHRONIZE WITHOUT DATA WORD (00001)

MESSAGE SEQUENCE = SYNC * STATUS

The CT2565 responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

TRANSMIT STATUS WORD (00010)

MESSAGE SEQUENCE = TRANSMIT STATUS * STATUS

The status and BIT word registers are not altered by this command and contain the resulting status from the previous command.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (S/W), Illegal Mode code, T/R Error (BIT Word).

INITIATE SELF-TEST (00011)

MESSAGE SEQUENCE = SELF TEST * STATUS

The CT2565 responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is generated.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).
5. **Faulty Test.** Bits set: terminal flag (SW), A/B Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word).

TRANSMITTER SHUTDOWN (00100)

MESSAGE SEQUENCE - SHUTDOWN * STATUS

This command is only used with dual redundant bus systems. The CT2565 responds with status. At the end of the status transmission, the CT2565 inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be re-activated by Override Transmitter Shutdown or RESET RT commands.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

Table 8 – Mode Codes

OVERRIDE TRANSMITTER SHUTDOWN (00101)

MESSAGE SEQUENCE - OVERRIDE SHUTDOWN - STATUS

This command is only used with dual redundant bus systems. The CT2565 responds with status. At the end of the status transmission, the CT2565 re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

INHIBIT TERMINAL FLAG BIT (00110)

MESSAGE SEQUENCE - INHIBIT TERMINAL FLAG * STATUS

The CT2565 responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)

MESSAGE SEQUENCE - OVERRIDE INHIBIT TERMINAL FLAG * STATUS

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

RESET REMOTE TERMINAL (01000)

MESSAGE SEQUENCE - RESET REMOTE TERMINAL * STATUS

The CT2565 responds with status and internally resets. Transmitter shutdown, mode commands, and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

RESERVED MODE CODES (01001-01111)

MESSAGE SEQUENCE = RESERVED MODE CODES * STATUS

The CT2565 responds with status. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), Illegal Mode Code (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

Table 8 – Mode Codes (continued)

TRANSMIT VECTOR WORD (10000)

MESSAGE SEQUENCE - TRANSMIT VECTOR WORD * STATUS VECTOR WORD

The CT2565 transmits a status word followed by a vector word. The contents of the vector word (from the subsystem) are enabled onto DBO-DB15 with BUSREQ after the command transfer (same as data word in a normal transmit command).

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW) High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode code, (BIT Word).

SYNCHRONIZE WITH DATA WORD (10001)

MESSAGE SEQUENCE - SYNCHRONIZE DATA WORD * STATUS

The data word received following the command word is transferred to the subsystem. The status register is then enabled and its contents transferred onto the data bus and transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count (BIT Word).
3. **Command followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count (BIT word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), T/R Error, High Word Count (BIT Word).
5. **Command, T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), High Word Count, T/R Error (BIT Word).

TRANSMIT LAST COMMAND (10010)

MESSAGE SEQUENCE = TRANSMIT LAST COMMAND * STATUS LAST COMMAND

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, (SW), Illegal Mode Code T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

TRANSMIT BIT WORD (10011)

MESSAGE SEQUENCE - TRANSMIT BIT WORD * STATUS BIT WORD

The CT2565 transmits a status word followed by the BIT word . When activated, BITEN allows the subsystem to latch the BIT word on the parallel data bus. The BIT word is not altered by this command; however, the next SW will reflect errors in this transmission.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode code, (BIT Word).

Table 8 – Mode Codes (continued)

SELECTED TRANSMITTER SHUTDOWN (10100)

MESSAGE SEQUENCE - TRANSMITTER SHUTDOWN DATA * STATUS

The data word received is transferred to the subsystem and status is transmitted. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RTs with more than one dual redundant channel.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High word count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count (BIT Word).

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

MESSAGE SEQUENCE - TRANSMITTER SHUTDOWN DATA * STATUS

The data word received after the command word is transferred to the subsystem. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (Bit Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count, T/R (BIT Word).

RESERVED MODE CODES

MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) * STATUS
RESERVED MODE CODE (T/R = 0) * STATUS

The CT2565 responds with status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

ERROR CONDITIONS (T/R = 1)

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

ERROR CONDITIONS (T/R = 0)

1. **Invalid Command.** No response, command ignored.
2. **Command not Followed by Contiguous Data Word.** No status response. Bits set: message error (SW), High word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

Table 8 – Mode Codes (continued)

Table 9A – Pin Function Table (78 Pin DDIP)

Pin #	Symbol	Description
1	RT/$\overline{BC}$	Mode Select input - logic "1" for RT mode, logic “0” for BC mode.
2	$\overline{MT}$	Monitor mode enable. When unit is operating as a BC, a logic “0” will select monitor mode.
3	$\overline{STATEN}$	Output signal in RT mode that indicates status word is being transferred on the internal bus.
4	$\overline{TIMEOUT}$	Indicates No Response Timeout has occured during BC and RTU (RT to RT transfer).
5	$\overline{HSFAIL}$	Output in RT mode indicating the DMA transfer did not occur in time to allow proper operation on the 1553 bus.
6	$\overline{DBACCEPT}$	Input signal used to set DBACCEPT bit in status register for response to a valid mode command on the 1553 bus.
7	$\overline{SSFLAG}$	Input which controls the SSFLAG bit in the status register.
8	$\overline{SVCREQ}$	Input which controls the service request bit in the status word.
9	$\overline{INCMD}$	Output signal indicating the RT is currently in a message transfer sequence.
10	$\overline{SSER}$	Input which controls the subsystem error bit in the status register.
11	$\overline{TESTOUT}$	Factory test point. Do not connect.
12	WC1	WC bit 1 - latched output of command word.
13	WC3	WC bit 3 - latched output of command word.
14	TXINH B	Transmitter inhibit output for channel B.
15	T/$\overline{R}$	Output indicating T/$\overline{R}$ bit of current command word in RT mode.
16	$\overline{CHA}$/CHB	Output indicating current selected channel (0 = Channel A).
17	$\overline{CS}$	Chip Select output for subsystem memory control.
18	$\overline{OE}$	Output Enable output for subsystem memory control.
19	$\overline{BUSREQ}$	Output signal used to initiate transfer to/from subsystem.
20	+5V	+5 Volt DC input.
21	DB0	Least significant bit - 16 bit parallel data bus.
22	DB2	Bit 2 of data bus.
23	DB4	Bit 4 of data bus.
24	DB6	Bit 6 of data bus.
25	DB8	Bit 8 of data bus.
26	DB10	Bit 10 of data bus.
27	DB12	Bit 12 of data bus.
28	DB14	Bit 14 of data bus.
29	LWORD	Last word output during BC mode indicates last data word of the current message transfer has been transferred on the parallel bus.

Table 9A – Pin Function Table (78 Pin DDIP) (continued)

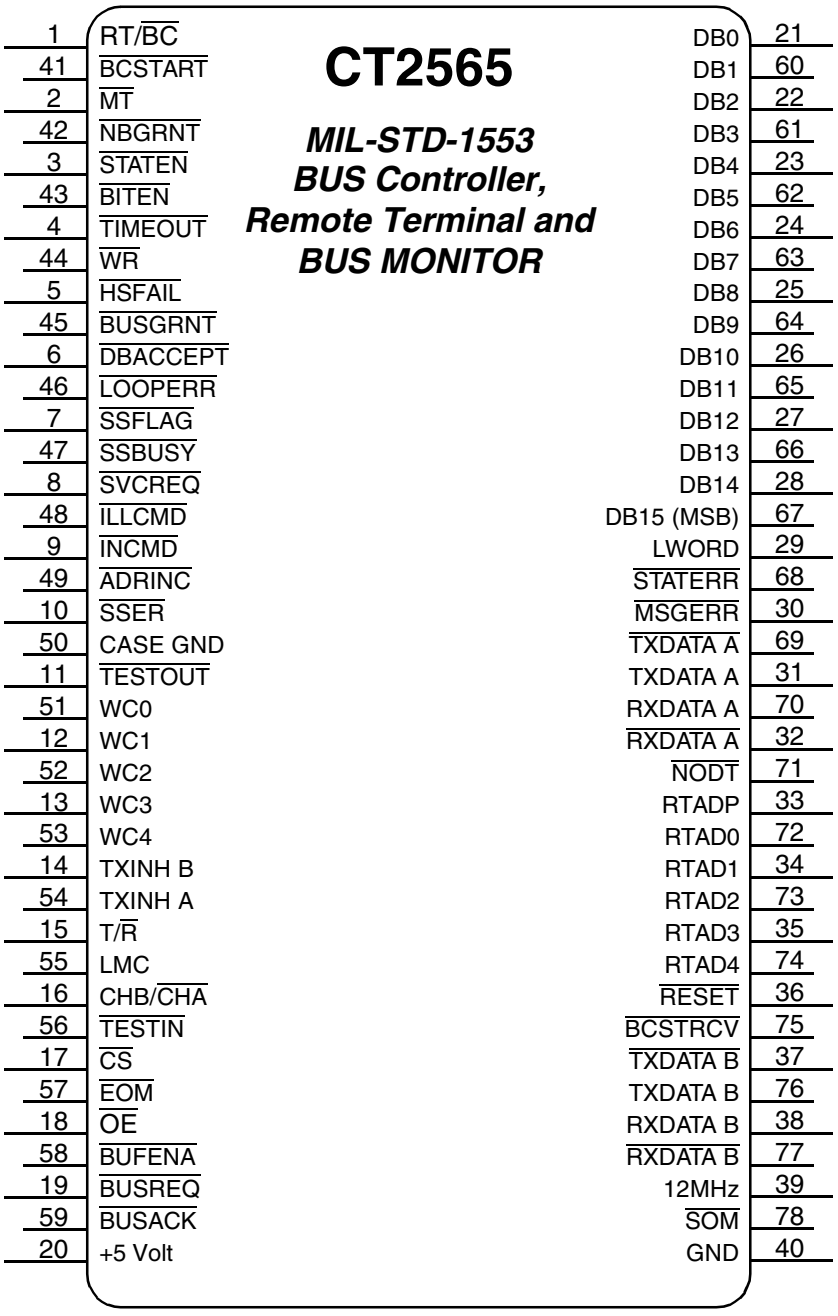
Pin #	Symbol	Description
30	$\overline{\text{MSGERR}}$	Output signal which indicates an error occurred during the current message sequence.
31	TXDATA A	Bipolar serial data output to positive input of bus transceiver.
32	$\overline{\text{RXDATA A}}$	Bipolar serial input from negative output of bus transceiver.
33	RTADP	Parity bit input for RT address.
34	RTAD1	Bit 1 of RT address input.
35	RTAD3	Bit 3 of RT address input.
36	$\overline{\text{RESET}}$	System reset input - resets all inputs in module.
37	$\overline{\text{TXDATA B}}$	Bipolar serial data output to negative input bus transceiver.
38	RXDATA B	Bipolar serial data input from positive output of bus transceiver.
39	12MHz	12MHz TTL clock input.
40	GROUND	Signal ground.
41	$\overline{\text{BCSTART}}$	Cycle enable input Logic "0" initiates bus controller message transfer operation.
42	$\overline{\text{NBGRNT}}$	New bus grant output from RT indicates beginning of message transfer sequence.
43	$\overline{\text{BITEN}}$	Built in Test enable output indicates RT is transferring BIT word on internal 16 bit bus.
44	$\overline{\text{WR}}$	Write enable output for control of subsystem memory.
45	$\overline{\text{BUSGRNT}}$	Bus request input in response to DTREQ. Allows BC/$\overline{\text{RT}}$ to transfer data to subsystem.
46	$\overline{\text{LOOPERR}}$	Loop error output. Logic "0" indicates failure of loop back transmitted data.
47	$\overline{\text{SSBUSY}}$	Subsystem busy input for RT status word.
48	$\overline{\text{ILLCMD}}$	Illegal command input to RT, used to block RT response to an illegal command.
49	$\overline{\text{ADRINC}}$	Increment output pulse. Goes LOW at the completion of each word transfer to/from subsystem. Can increment external address counter.
50	CHASSIS	Frame ground electricity isolated from signal ground
51	WC0	LSB of current command word count field.
52	WC2	Bit 2 of word count field.
53	WC4	Bit 4 of word count field.
54	TXINH A	Transmitter inhibit output signal for Channel A.
55	LMC	Latched Mode Command. Logic "1" indicates current word command is a mode code word, WC0-WC4.
56	$\overline{\text{TESTIN}}$	Factory test point. Do not connect.
57	$\overline{\text{EOM}}$	End of message output. Logic "0" occurs when BC/$\overline{\text{RT}}$ message is completed.
58	$\overline{\text{BUFENA}}$	Buffer enable input, may be driven LOW by $\overline{\text{STATEN}}$ or $\overline{\text{BITEN}}$ if subsystem must read bit or Status words. Enables internal 16 bit bus onto subsystem bus.

Table 9A – Pin Function Table (78 Pin DDIP) (continued)

Pin #	Symbol	Description
59	$\overline{\text{BUSACK}}$	Bus acknowledge output. LOW during DMA Handshake, in response to $\overline{\text{BUSGRNT}}$.
60	DB1	Bit 1 of 16 bit parallel bus.
61	DB3	Bit 3 of 16 bit parallel bus.
62	DB5	Bit 5 of 16 bit parallel bus.
63	DB7	Bit 7 of 16 bit parallel bus.
64	DB9	Bit 9 of 16 bit parallel bus.
65	DB11	Bit 11 of 16 bit parallel bus.
66	DB13	Bit 13 of 16 bit parallel bus.
67	DB15	Bit 15 of 16 bit parallel bus.
68	$\overline{\text{STATERR}}$	BC output indicates one or more bits set or address mismatch in a received status word.
69	$\overline{\text{TXDATA A}}$	Bipolar serial data output to negative input of bus transceiver.
70	RXDATA A	Bipolar serial data input from positive output of bus transceiver.
71	$\overline{\text{NODT}}$	No data input. Logic "0" indicates the 1553 bus is idle; HIGH means device front end is active.
72	RTAD0	LSB of 5 bit RT address.
73	RTAD2	Bit 2 of RT address.
74	RTAD4	Bit 4 of RT address.
75	$\overline{\text{BCSTRCV}}$	Broadcast receive. Logic "0" means the current command was a broadcast command.
76	TXDATA B	Bipolar serial output to positive input of bus transceiver.
77	$\overline{\text{RXDATA B}}$	Bipolar serial input from negative output of bus transceiver.
78	$\overline{\text{SOM}}$	Start of message output indicates beginning of RT/$\overline{\text{BC}}$ message transfer sequence.

Table 9B – CT2565 Pin Out Description (DDIP)

Pin #	Function	Pin #	Function
1	RT/$\overline{BC}$	40	GND
2	$\overline{MT}$	41	$\overline{BCSTART}$
3	$\overline{STATEN}$	42	$\overline{NBGRNT}$
4	$\overline{TIMEOUT}$	43	$\overline{BITEN}$
5	$\overline{HSFAIL}$	44	$\overline{WR}$
6	$\overline{DBACCEPT}$	45	$\overline{BUSGRNT}$
7	$\overline{SSFLAG}$	46	$\overline{LOOPERR}$
8	$\overline{SVCREQ}$	47	$\overline{SSBUSY}$
9	$\overline{INCMD}$	48	$\overline{ILLCMD}$
10	$\overline{SSER}$	49	$\overline{ADRINC}$
11	$\overline{TESTOUT}$	50	CASE GND
12	WC1	51	WC0
13	WC3	52	WC2
14	TXINH B	53	WC4
15	T/$\overline{R}$	54	TXINH A
16	CHB/$\overline{CHA}$	55	LMC
17	$\overline{CS}$	56	$\overline{TESTIN}$
18	$\overline{OE}$	57	$\overline{EOM}$
19	$\overline{BUSREQ}$	58	$\overline{BUFENA}$
20	+ 5 Volt	59	$\overline{BUSACK}$
21	DB0 (LSB)	60	DB1
22	DB2	61	DB3
23	DB4	62	DB5
24	DB6	63	DB7
25	DB8	64	DB9
26	DB10	65	DB11
27	DB12	66	DB13
28	DB14	67	DB15 (MSB)
29	LWORD	68	$\overline{STATERR}$
30	$\overline{MSGERR}$	69	$\overline{TXDATA\ A}$
31	TXDATA A	70	RXDATA A
32	$\overline{RXDATA\ A}$	71	$\overline{NODT}$
33	RTADP	72	RTAD0
34	RTAD1	73	RTAD2
35	RTAD3	74	RTAD4
36	$\overline{RESET}$	75	$\overline{BCSTRCV}$
37	$\overline{TXDATA\ B}$	76	TXDATA B
38	RXDATA B	77	$\overline{RXDATA\ B}$
39	12MHz	78	$\overline{SOM}$



DDIP Pin Connection Diagram, CT2565 and Pinout

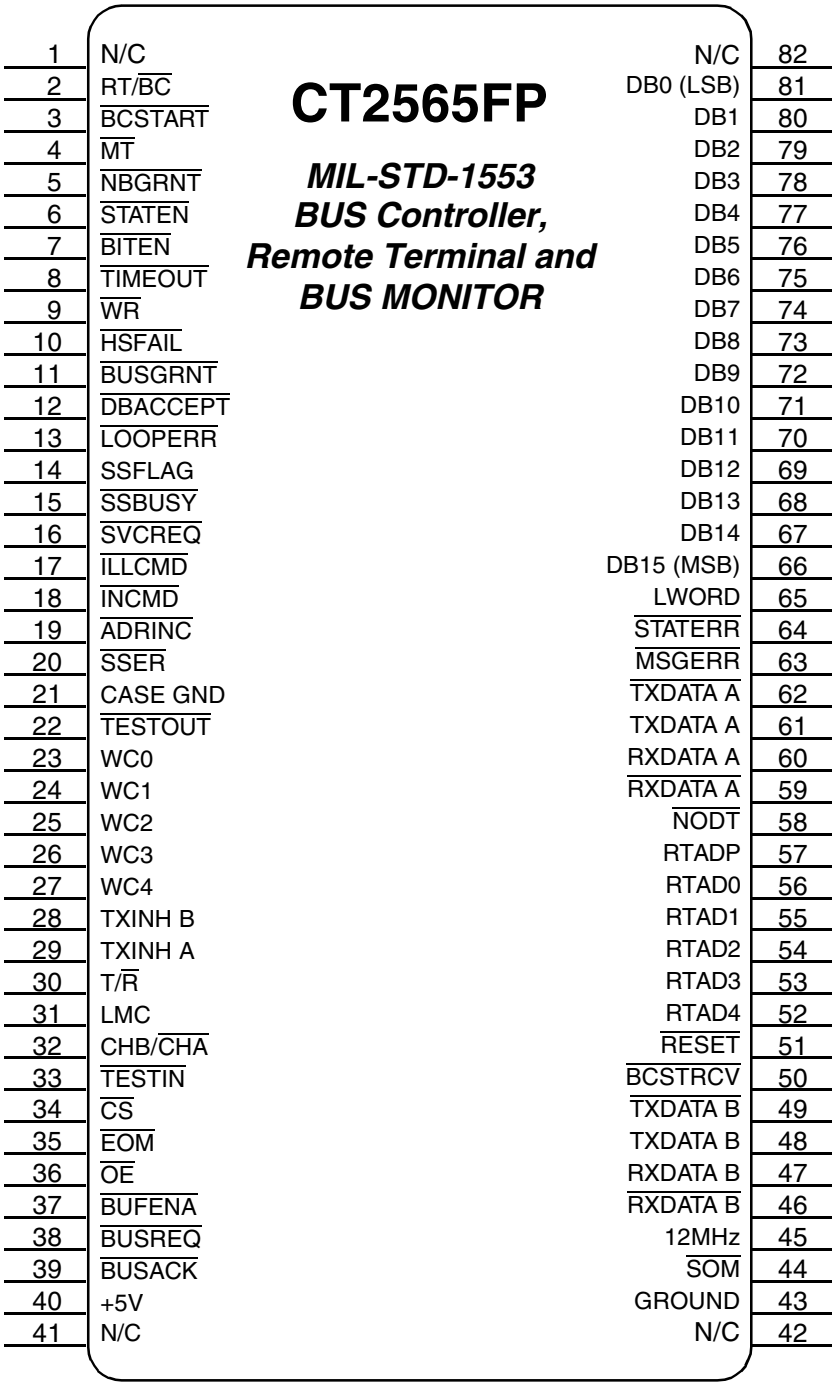


Table 10 – CT2565 Pin Out Description (FP)

Pin #	Function	Pin #	Function
1	N/C	42	N/C
2	RT/$\overline{BC}$	43	GROUND
3	$\overline{BCSTART}$	44	$\overline{SOM}$
4	$\overline{MT}$	45	12MHz
5	$\overline{NBGRNT}$	46	$\overline{RXDATA\ B}$
6	$\overline{STATEN}$	47	RXDATA B
7	$\overline{BITEN}$	48	TXDATA B
8	$\overline{TIMEOUT}$	49	$\overline{TXDATA\ B}$
9	$\overline{WR}$	50	$\overline{BCSTRCV}$
10	$\overline{HSFAIL}$	51	$\overline{RESET}$
11	$\overline{BUSGRNT}$	52	RTAD4
12	$\overline{DBACCEPT}$	53	RTAD3
13	$\overline{LOOPERR}$	54	RTAD2
14	SSFLAG	55	RTAD1
15	$\overline{SSBUSY}$	56	RTAD0
16	$\overline{SVCREQ}$	57	RTADP
17	$\overline{ILLCMD}$	58	$\overline{NODT}$
18	$\overline{INCMD}$	59	$\overline{RXDATA\ A}$
19	$\overline{ADRINC}$	60	RXDATA A
20	$\overline{SSER}$	61	TXDATA A
21	CASE GND	62	$\overline{TXDATA\ A}$
22	$\overline{TESTOUT}$	63	$\overline{MSGERR}$
23	WC0	64	$\overline{STATERR}$
24	WC1	65	LWORD
25	WC2	66	DB15 (MSB)
26	WC2	67	DB14
27	WC4	68	DB13
28	TXINH B	69	DB12
29	TXINH A	70	DB11
30	T/$\overline{R}$	71	DB10
31	LMC	72	DB9
32	CHB/$\overline{CHA}$	73	DB8
33	$\overline{TESTIN}$	74	DB7
34	$\overline{CS}$	75	DB6
35	$\overline{EOM}$	76	DB5
36	$\overline{OE}$	77	DB4
37	$\overline{BUFENA}$	78	DB3
38	$\overline{BUSREQ}$	79	DB2
39	$\overline{BUSACK}$	80	DB1
40	+5V	81	DB0 (LSB)
41	N/C	82	N/C

Flat Package Pin Connection Diagram, CT2566 and Pinout

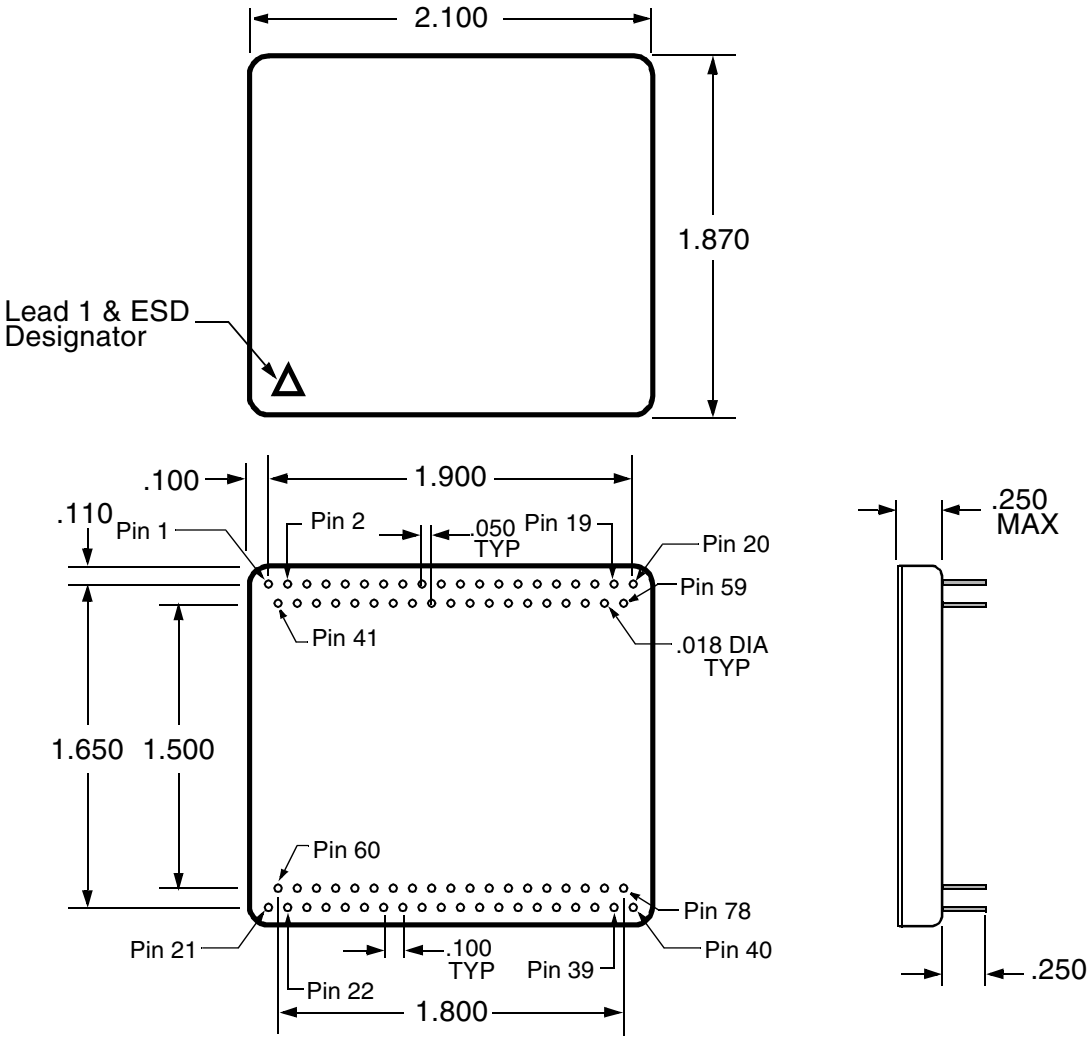


Figure 23 – Plug In Package Outline

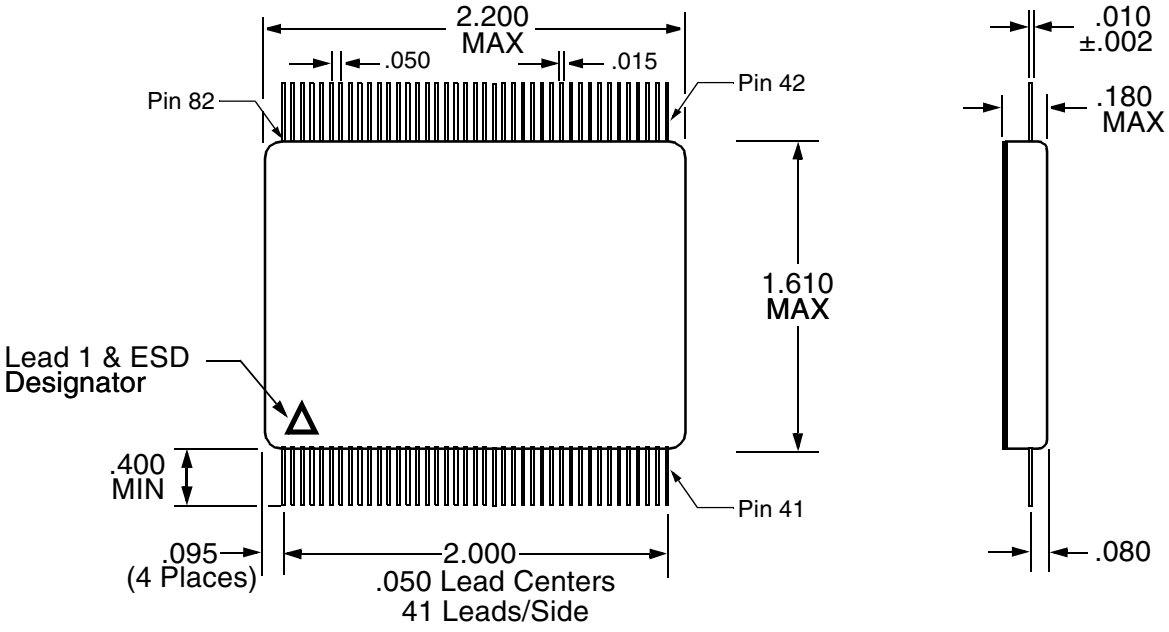


Figure 24 – Flat Package Outline

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Ordering Information

Model Number	Screening	DESC SMD #	Package
CT2565	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883	-	Plug in
CT2565-FP		-	Flat Package
CT2565-001-1	Per SMD	5962-8858501XA	Plug in
CT2565-001-2		5962-8858501XC	Plug in
CT2565-201-1		5962-8858501YA	Flat Package
CT2565-201-2		5962-8858501YC	Flat Package

Specifications subject to change without notice

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