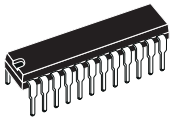
L6226

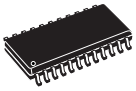
DMOS DUAL FULL BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 2.8A OUTPUT PEAK CURRENT (1.4A DC)
- $R_{DS(ON)}$ 0.73Ω TYP. VALUE @ T_j = 25 °C
- OPERATING FREQUENCY UP TO 100KHz
- PROGRAMMABLE HIGH SIDE OVERCURRENT DETECTION AND PROTECTION
- DIAGNOSTIC OUTPUT
- PARALLELED OPERATION
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- UNDER VOLTAGE LOCKOUT
- INTEGRATED FAST FREE WHEELING DIODES



PowerDIP24 (20+2+2)

PowerSO36



SO24 (20+2+2)

ORDERING NUMBERS:
L6226N (PowerDIP24)
L6226PD (PowerSO36)
L6226D (SO24)

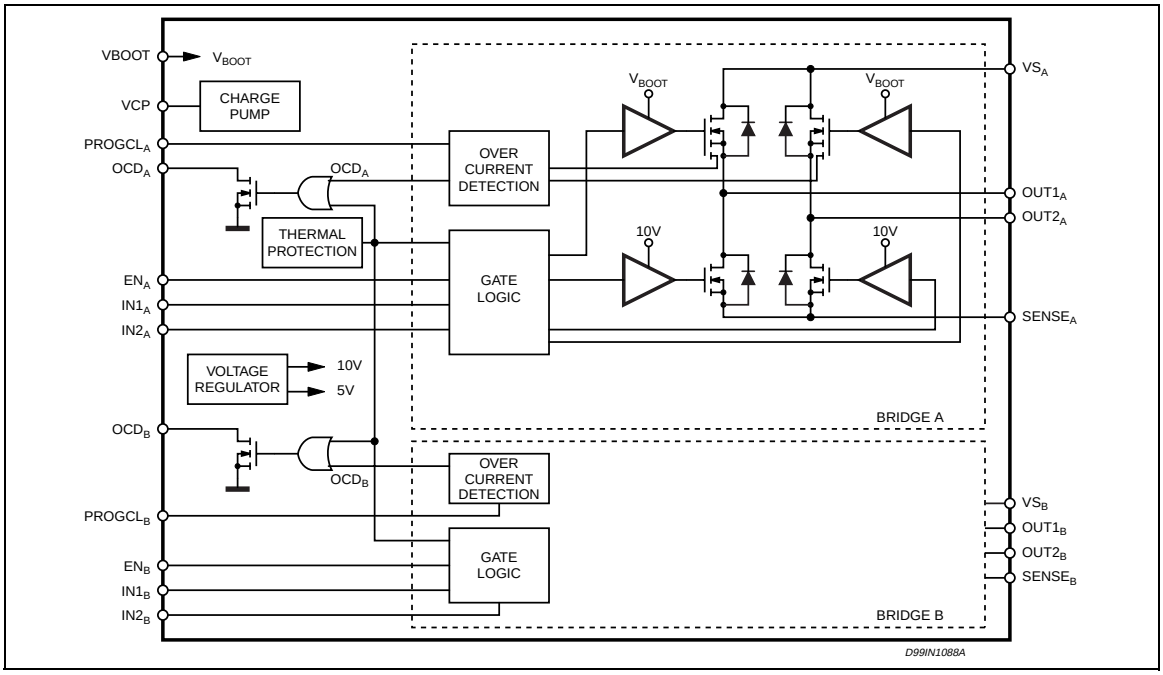
TYPICAL APPLICATIONS

- BIPOLAR STEPPER MOTOR
- DUAL OR QUAD DC MOTOR

DESCRIPTION

The L6226 is a DMOS Dual Full Bridge designed for motor control applications, realized in MultiPower-BCD technology, which combines isolated DMOS Power Transistors with CMOS and bipolar circuits on the same chip. Available in PowerDIP24 (20+2+2), PowerSO36 and SO24 (20+2+2) packages, the L6226 features thermal shutdown and a non-dissipative overcurrent detection on the high side Power MOSFETs plus a diagnostic output that can be easily used to implement the overcurrent protection.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential Voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60V$; $V_{SENSEA} = V_{SENSEB} = GND$	60	V
OCD_A,OCD_B	OCD pins Voltage Range		-0.3 to +10	V
$PROGCL_A$, $PROGCL_B$	PROGCL pins Voltage Range		-0.3 to +7	V
V_{BOOT}	Bootstrap Peak Voltage	$V_{SA} = V_{SB} = V_S$	V_S + 10	V
V_{IN},V_{EN}	Input and Enable Voltage Range		-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$		-1 to +4	V
$I_{S(peak)}$	Pulsed Supply Current (for each V_S pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1ms$	3.55	A
I_S	RMS Supply Current (for each V_S pin)	$V_{SA} = V_{SB} = V_S$	2.8	A
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

RECOMMENDED OPERATING CONDITIONS

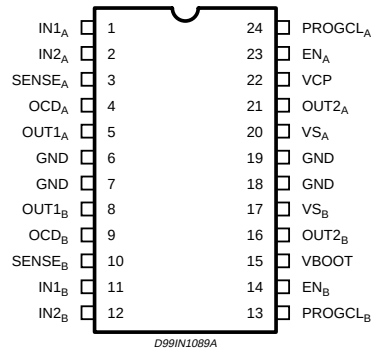
Symbol	Parameter	Test Conditions	MIN	MAX	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential Voltage Between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$		52	V
V_{SENSEA}, V_{SENSEB}	Voltage Range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V V
I_{OUT}	RMS Output Current			1.4	A
T_j	Operating Junction Temperature		-25	+125	°C
f_{sw}	Switching Frequency			100	KHz

THERMAL DATA

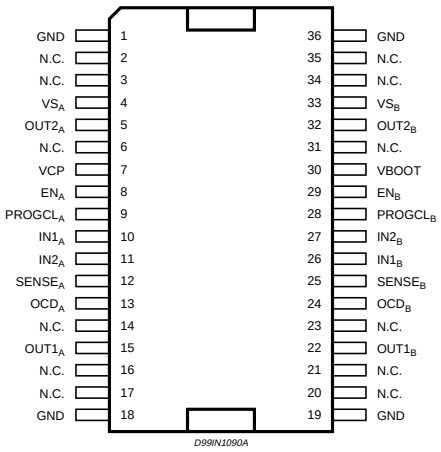
Symbol	Description	PowerDIP24	SO24	PowerSO36	Unit
$R_{th\text{-}j\text{-}pins}$	MaximumThermal Resistance Junction-Pins	19	15	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	2	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient [1]	44	52	-	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [2]	-	-	36	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient [3]	-	-	16	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient [4]	59	78	63	°C/W

(1) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the bottom side of 6 cm^2 (with a thickness of 35 µm).
(2) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm).
(3) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer.
(4) Mounted on a multi-layer FR4 PCB without any heat sinking surface on the board.

PIN CONNECTIONS (Top View)



PowerDIP24/SO24



PowerSO36(5)

(5) The slug is internally connected to pins 1,18,19 and 36 (GND pins).

PIN DESCRIPTION

PACKAGE		Name	Type	Function
SO24/ PowerDIP24	PowerSO36			
PIN #	PIN #			
1	10	$IN1_A$	Logic input	Bridge A Logic Input 1.
2	11	$IN2_A$	Logic input	Bridge A Logic Input 2.
3	12	$SENSE_A$	Power Supply	Bridge A Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
4	13	OCD_A	Open Drain Output	Bridge A Overcurrent Detection and thermal protection pin. An internal open drain transistor pulls to GND when overcurrent on bridge A is detected or in case of thermal protection.
5	15	$OUT1_A$	Power Output	Bridge A Output 1.
6, 7, 18, 19	1, 18, 19, 36	GND	GND	Signal Ground terminals. In Power DIP and SO packages, these pins are also used for heat dissipation toward the PCB.
8	22	$OUT1_B$	Power Output	Bridge B Output 1.
9	24	OCD_B	Open Drain Output	Bridge B Overcurrent Detection and thermal protection pin. An internal open drain transistor pulls to GND when overcurrent on bridge B is detected or in case of thermal protection.
10	25	$SENSE_B$	Power Supply	Bridge B Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
11	26	$IN1_B$	Logic Input	Bridge B Input 1
12	27	$IN2_B$	Logic Input	Bridge B Input 2
13	28	$PROGCL_B$	R Pin	Bridge B Overcurrent Level Programming. A resistor connected between this pin and Ground sets the programmable current limiting value for the bridge B. By connecting this pin to Ground the maximum current is set. This pin cannot be left non-connected.
14	29	EN_B	Logic Input	Bridge B Enable. LOW logic level switches OFF all Power MOSFETs of Bridge B. If not used, it has to be connected to +5V.
15	30	VBOOT	Supply Voltage	Bootstrap Voltage needed for driving the upper Power MOSFETs of both Bridge A and Bridge B.
16	32	$OUT2_B$	Power Output	Bridge B Output 2.
17	33	VS_B	Power Supply	Bridge B Power Supply Voltage. It must be connected to the supply voltage together with pin VS_A.
20	4	VS_A	Power Supply	Bridge A Power Supply Voltage. It must be connected to the supply voltage together with pin VS_B.
21	5	$OUT2_A$	Power Output	Bridge A Output 2.

PIN DESCRIPTION (continued)

PACKAGE		Name	Type	Function
SO24/ PowerDIP24	PowerSO36			
PIN #	PIN #			
22	7	VCP	Output	Charge Pump Oscillator Output.
23	8	EN_A	Logic Input	Bridge A Enable. LOW logic level switches OFF all Power MOSFETs of Bridge A. If not used, it has to be connected to +5V.
24	9	$PROGCL_A$	R Pin	Bridge A Overcurrent Level Programming. A resistor connected between this pin and Ground sets the programmable current limiting value for the bridge A. By connecting this pin to Ground the maximum current is set. This pin cannot be left non-connected.

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{Sth(ON)}$	Turn-on Threshold		5.8	6.3	6.8	V
$V_{Sth(OFF)}$	Turn-off Threshold		5	5.5	6	V
I_S	Quiescent Supply Current	All Bridges OFF; T_j = -25°C to 125°C (6)		5	10	mA
$T_{j(OFF)}$	Thermal Shutdown Temperature			165		°C
Output DMOS Transistors						
$R_{DS(ON)}$	High-Side + Low-Side Switch ON Resistance	T_j = 25 °C		1.47	1.69	Ω
		T_j =125 °C (6)		2.35	2.70	Ω
I_{DSS}	Leakage Current	EN = Low; OUT = V_S			2	mA
		EN = Low; OUT = GND	-0.3			mA
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 2.8A, EN = LOW		1.15	1.3	V
t_{rr}	Reverse Recovery Time	I_f = 1.4A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Logic Input						
V_{IL}	Low level logic input voltage		-0.3		0.8	V
V_{IH}	High level logic input voltage		2		7	V
I_{IL}	Low Level Logic Input Current	GND Logic Input Voltage	-10			µA
I_{IH}	High Level Logic Input Current	7V Logic Input Voltage			10	µA
$V_{th(ON)}$	Turn-on Input Threshold			1.8	2.0	V

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{th(OFF)}$	Turn-off Input Threshold		0.8	1.3		V
$V_{th(HYS)}$	Input Threshold Hysteresis		0.25	0.5		V
Switching Characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time (8)	I_{LOAD} =1.4A, Resistive Load	500		800	ns
$t_{D(on)IN}$	Input to out turn ON delay time	I_{LOAD} =1.4A, Resistive Load (dead time included)		1.9		µs
t_{RISE}	Output rise time(8)	I_{LOAD} =1.4A, Resistive Load	40		250	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time (8)	I_{LOAD} =1.4A, Resistive Load	500	800	1000	ns
$t_{D(off)IN}$	Input to out turn OFF delay time	I_{LOAD} =1.4A, Resistive Load	500	800	1000	ns
t_{FALL}	Output Fall Time (8)	I_{LOAD} =1.4A, Resistive Load	40		250	ns
t_{dt}	Dead Time Protection		0.5	1		µs
f_{CP}	Charge pump frequency	-25°C<T_j <125°C		0.6	1	MHz
Over Current Detection						
$I_{s\ over}$	Input Supply Over Current DetectionThreshold	-25°C<T_j <125 °C; RCL= 39 kΩ -25°C<T_j <125 °C; RCL= 5 kΩ -25°C<T_j <125 °C; RCL= GND	-10% -10% -30%	0.29 2.21 2.8	+10% +10% +30%	A A A
R_{OPDR}	Open Drain ON Resistance	I = 4mA		40	60	Ω
$t_{OCD(ON)}$	OCD Turn-on Delay Time (8)	I = 4mA; C_{EN} < 100pF		200		ns
$t_{OCD(OFF)}$	OCD Turn-off Delay Time (8)	I = 4mA; C_{EN} < 100pF		100		ns

(6) Tested at 25°C in a restricted range and guaranteed by characterization.
(7) See Fig. 1.
(8) See Fig. 2.

Figure 1. Switching Characteristic Definition

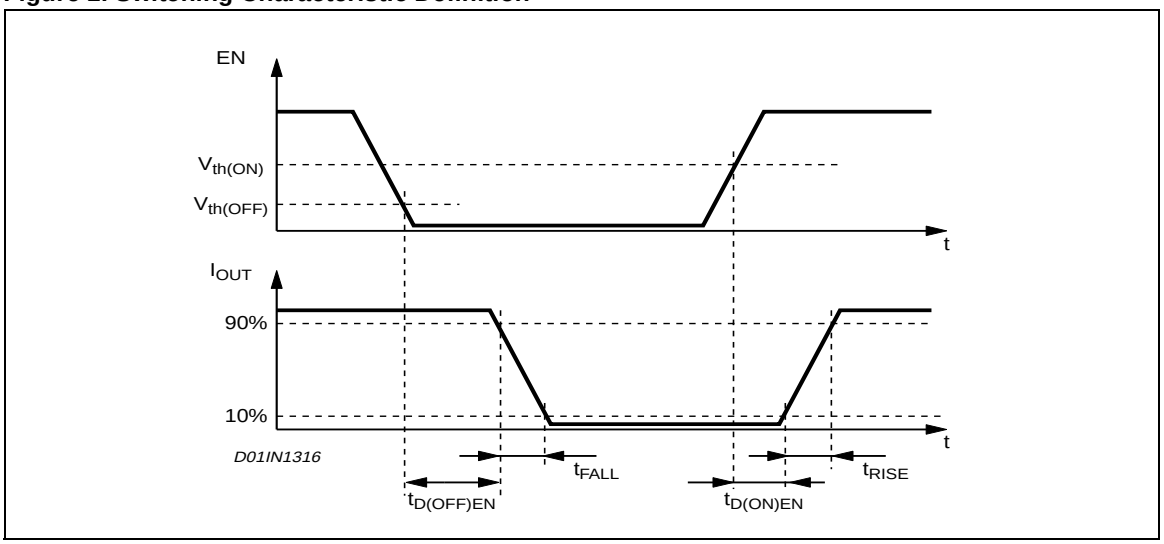
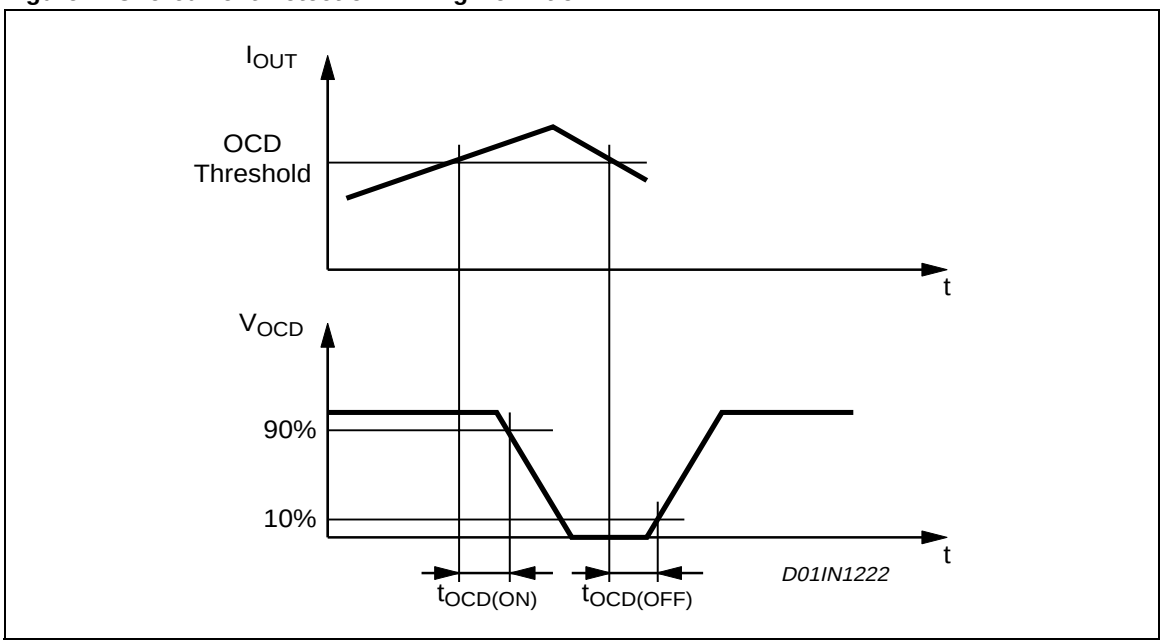


Figure 2. Overcurrent Detection Timing Definition



CIRCUIT DESCRIPTION

POWER STAGES and CHARGE PUMP

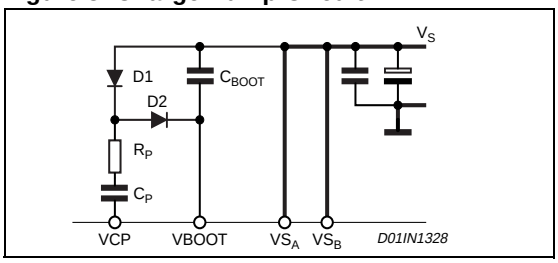
The L6226 integrates two independent Power MOS Full Bridges. Each Power MOS has an Rdson=0.73ohm (typical value @ 25°C), with intrinsic fast freewheeling diode. Cross conduction protection is achieved using a dead time (td = 1µs typical) between the switch off and switch on of two Power MOS in one leg of a bridge.

Using N Channel Power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The Bootstrapped (Vboot) supply is obtained through an internal Oscillator and few external components to realize a charge pump circuit as shown in Figure 3. The oscillator output (VCP) is a square wave at 600kHz (typical) with 10V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table1.

Table 1. Charge Pump External Components Values

C_{BOOT}	220nF
C_P	10nF
R_P	100Ω
D1	1N4148
D2	1N4148

Figure 3. Charge Pump Circuit



LOGIC INPUTS

Pins $IN1_A$, $IN2_A$, $IN1_B$, $IN2_B$, EN_A and EN_B are TTL/CMOS and uC compatible logic inputs. The internal structure is shown in Fig. 4. Typical value for turn-on and turn-off thresholds are respectively Vthon=1.8V and Vthoff = 1.3V.

Pins EN_A and EN_B are commonly used to implement Overcurrent and Thermal protection by connecting them respectively to the outputs OCD_A and OCD_B, which are open-drain outputs. If that type of connection is chosen, some care needs to be taken in driving these pins. Two configurations are shown in Fig. 5 and Fig. 6. If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in Fig. 5. If the driver is a standard Push-Pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in Fig. 6. The resistor R_{EN} should be chosen in the range from 2.2kΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF. More information on selecting the values is found in the Overcurrent Protection section.

Figure 4. Logic Inputs Internal Structure

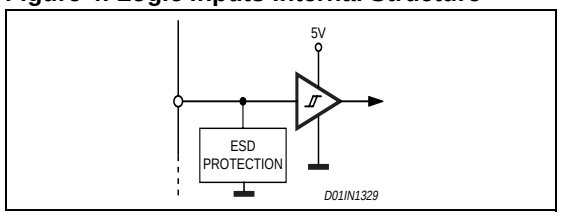


Figure 5. EN_A and EN_B Pins Open Collector Driving

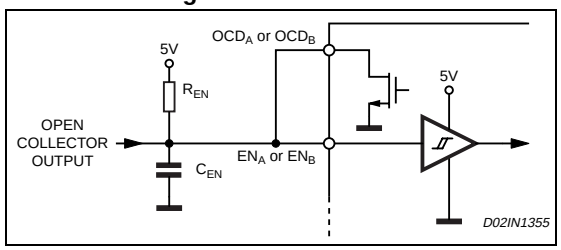
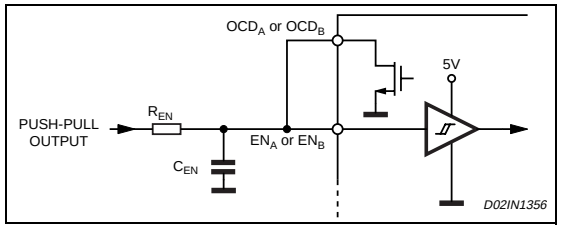


Figure 6. EN_A and EN_B Pins Push-Pull Driving



TRUTH TABLE

INPUTS			OUTPUTS	
EN	**IN1**	**IN2**	**OUT1**	**OUT2**
L	X	X	High Z	High Z
H	L	L	GND	GND
H	H	L	Vs	GND
H	L	H	GND	Vs
H	H	H	Vs	Vs

X = Don't care
High Z = High Impedance Output

NON-DISSIPATIVE OVERCURRENT DETECTION AND PROTECTION

In addition to the PWM current control, an overcurrent detection circuit (OCD) is integrated. This circuit can be used to provides protection against a short circuit to ground or between two phases of the bridge as well as a roughly regulation of the load current. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Fig. 7 shows a simplified schematic of the overcurrent detection circuit for the Bridge A. Bridge B is provided of an analogous circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold Isover the OCD comparator signals a fault condition. When a fault condition is detected, an internal open drain MOS with a pull down capability of 4mA connected to OCD pin is turned on. Fig. 8 shows the OCD operation.

This signal can be used to regulate the output current simply by connecting the OCD pin to EN pin and adding an external R-C as shown in Fig.7. The off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

I_{REF} and, therefore, the output current detection threshold are selectable by R_{CL} value, following the equations:

– Isover = 2.8A ±30% at -25°C < T_j < 125°C if R_{CL} = 0Ω (PROGCL connected to GND)

– $Isover = \frac{11050}{R_{CL}}$ ±10% at -25°C < T_j < 125°C if 5KΩ < R_C < 40kΩ

Fig. 9 shows the output current protection threshold versus R_{CL} value in the range 5kΩ to 40kΩ.

The Disable Time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in Figure 10. The Delay Time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in Figure 11.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable Delay Time and the R_{EN} value should be chosen according to the desired Disable Time.

The resistor R_{EN} should be chosen in the range from 2.2KΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF that allow obtaining 200µs Disable Time.

Figure 7. Overcurrent Protection Simplified Schematic

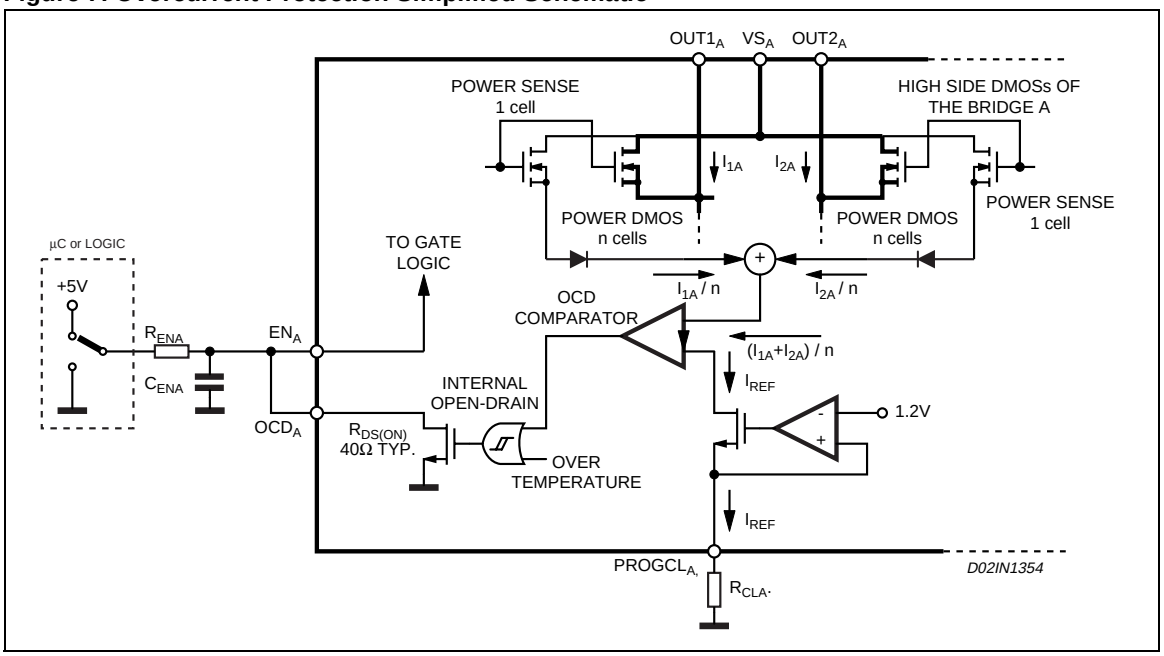


Figure 8. Overcurrent Protection Waveforms

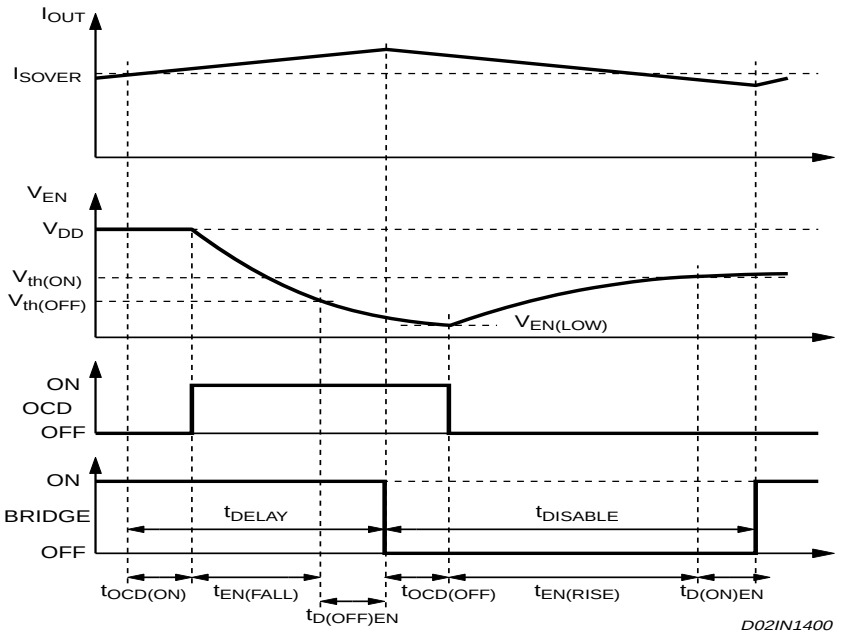


Figure 9. Output Current Protection Threshold versus R_{CL} Value

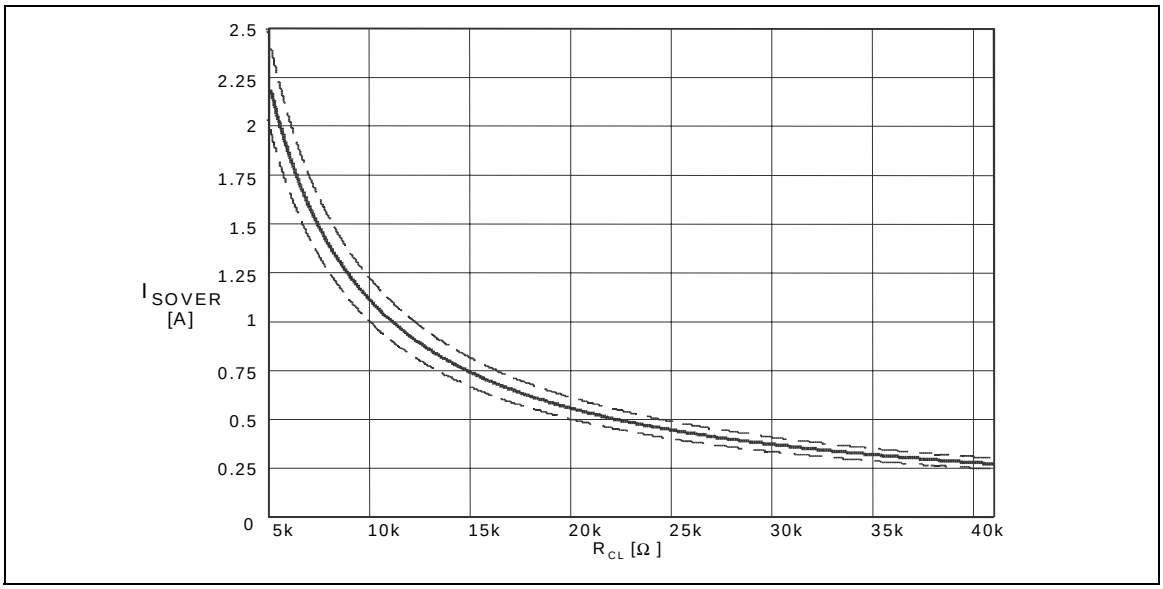


Figure 10. $t_{DISABLE}$ versus C_{EN} and R_{EN} (V_{DD} = 5V).

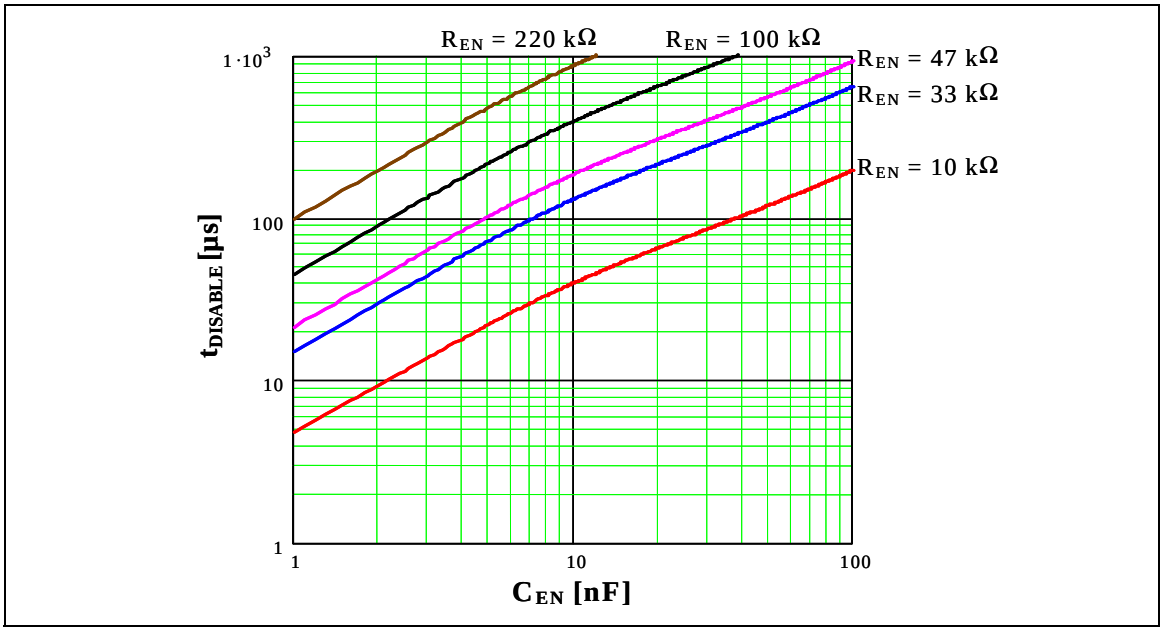
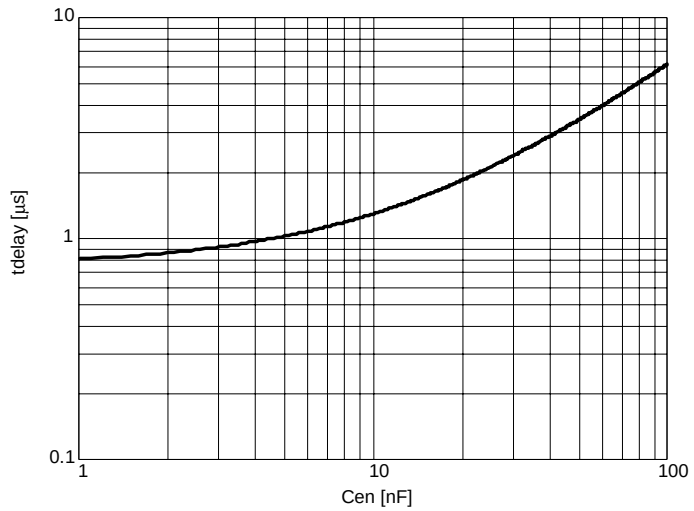


Figure 11. t_{DELAY} versus C_{EN} (V_{DD} = 5V).



THERMAL PROTECTION

In addition to the Ovecurrent Detection, the L6226 integrates a Thermal Protection for preventing the device destruction in case of junction over temperature. It works sensing the die temperature by means of a sensible element integrated in the die. The device switch-off when the junction temperature reaches 165°C (typ. value) with 15°C hysteresis (typ. value).

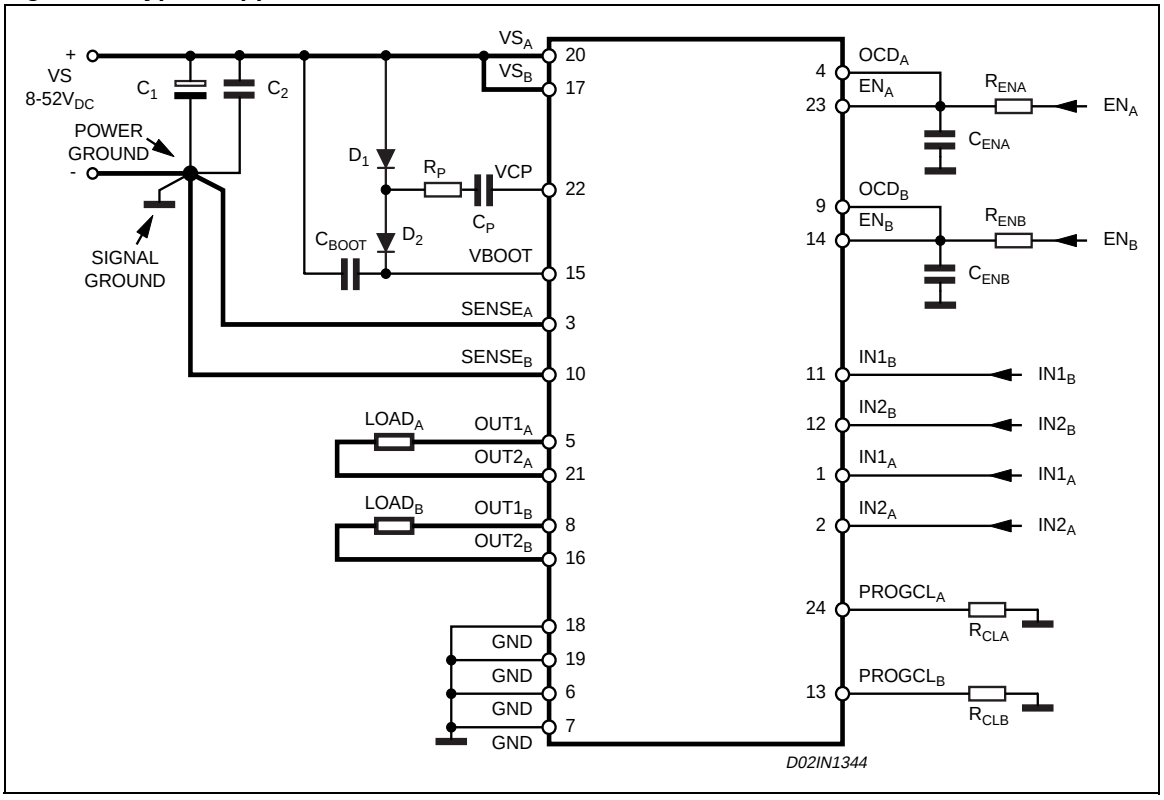
APPLICATION INFORMATION

A typical application using L6226 is shown in Fig. 12. Typical component values for the application are shown in Table 2. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6226 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN_A/OCD_A and EN_B/OCD_B nodes to ground set the shut down time for the Brgidge A and Bridge B respectively when an over current is detected (see Overcurrent Protection). The two current sources ($SENSE_A$ and $SENSE_B$) should be connected to Power Ground with a trace length as short as possible in the layout. To increase noise immunity, unused logic pins are best connected to 5V (High Logic Level) or GND (Low Logic Level) (see pin description). It is recommended to keep Power Ground and Signal Ground separated on PCB.

Table 2. Component Values for Typical Application

C_1	100uF	D_1	1N4148
C_2	100nF	D_2	1N4148
C_{BOOT}	220nF	R_{CLA}	5KΩ
C_P	10nF	R_{CLB}	5KΩ
C_{ENA}	5.6nF	R_{ENA}	100kΩ
C_{ENB}	5.6nF	R_{ENB}	100kΩ
C_{REF}	68nF	R_P	100Ω

Figure 12. Typical Application



PARALLELED OPERATION

The outputs of the L6226 can be paralleled to increase the output current capability or reduce the power dissipation in the device at a given current level. It must be noted, however, that the internal wire bond connections from the die to the power or sense pins of the package must carry current in both of the associated half bridges. When the two halves of one full bridge (for example $OUT1_A$ and $OUT2_A$) are connected in parallel, the peak current rating is not increased since the total current must still flow through one bond wire on the power supply or sense pin. In addition the over current detection senses the sum of the current in the upper devices of each bridge (A or B) so connecting the two halves of one bridge in parallel does not increase the over current detection threshold.

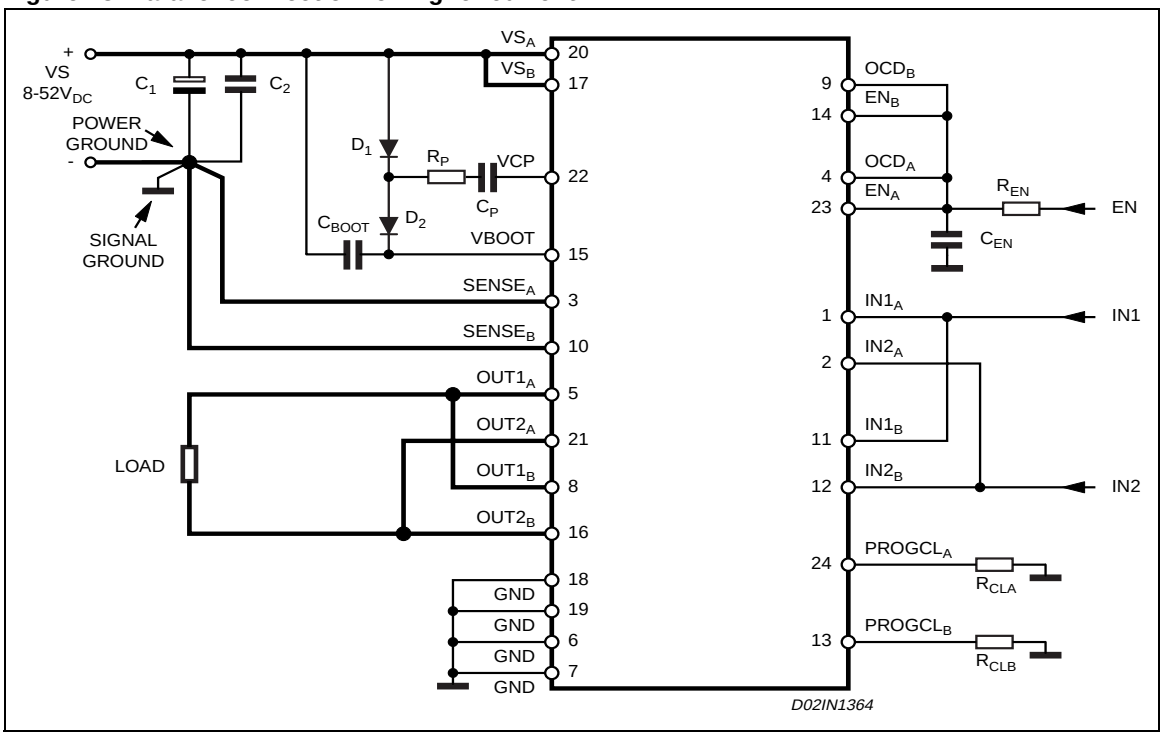
For most applications the recommended configuration is Half Bridge 1 of Bridge A paralleled with the Half Bridge 1 of the Bridge B, and the same for the Half Bridges 2 as shown in Figure 13. The current in the two devices connected in parallel will share very well since the $R_{DS(ON)}$ of the devices on the same die is well matched.

When connected in this configuration the over current detection circuit, which senses the current in each bridge (A and B), will sense the current in upper devices connected in parallel independently and the sense circuit with the lowest threshold will trip first. With the enables connected in parallel, the first detection of an over current in either upper DMOS device will turn of both bridges. Assuming that the two DMOS devices share the current equally, the resulting over current detection threshold will be twice the minimum threshold set by the resistors R_{CLA} or R_{CLB} in figure 13. It is recommended to use $R_{CLA} = R_{CLB}$.

In this configuration the resulting Bridge has the following characteristics.

- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$ 0.37Ω Typ. Value @ T_J = 25°C
- 2.8A max RMS Load Current
- 5.6A max OCD Threshold

Figure 13. Parallel connection for higher current



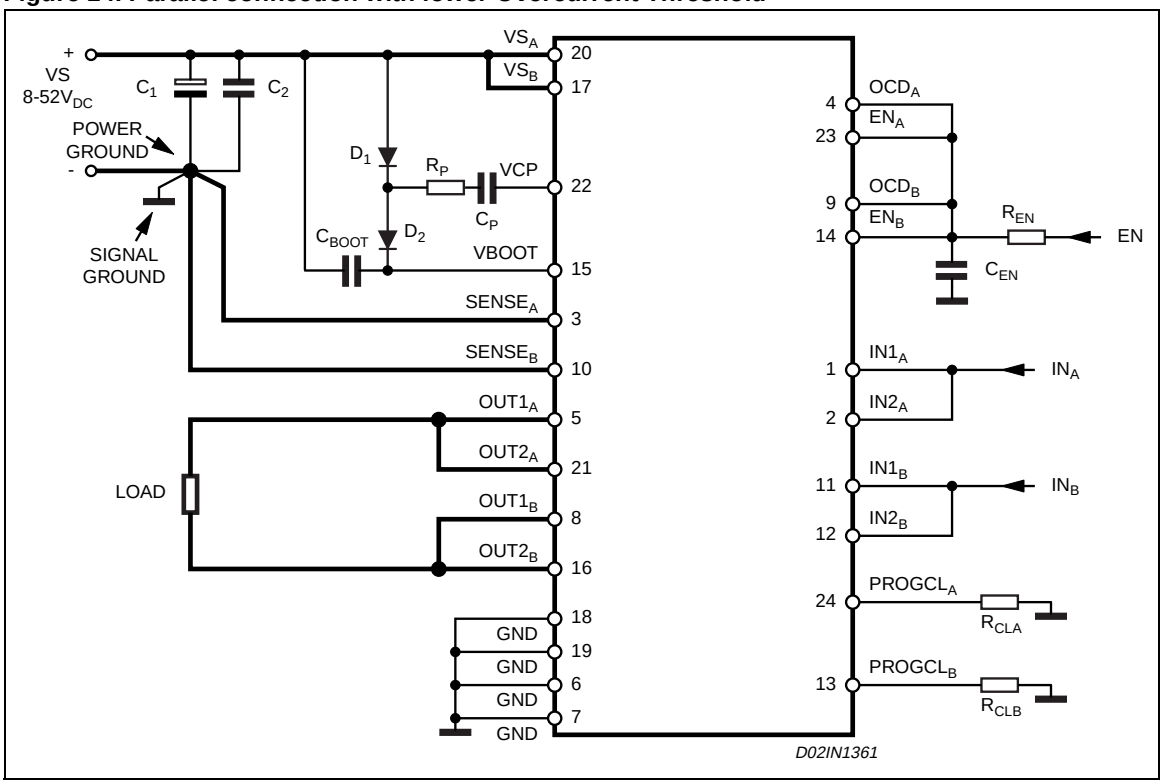
To operate the device in parallel and maintain a lower over current threshold, Half Bridge 1 and the Half Bridge 2 of the Bridge A can be connected in parallel and the same done for the Bridge B as shown in Figure 14. In this configuration, the peak current for each half bridge is still limited by the bond wires for the supply and sense pins so the dissipation in the device will be reduced, but the peak current rating is not increased.

When connected in this configuration the over current detection circuit, senses the sum of the current in upper devices connected in parallel. With the enables connected in parallel, an over current will turn of both bridges. Since the circuit senses the total current in the upper devices, the over current threshold is equal to the threshold set the resistor R_{CLA} or R_{CLB} in figure 14. R_{CLA} sets the threshold when outputs $OUT1_A$ and $OUT2_A$ are high and resistor R_{CLB} sets the threshold when outputs $OUT1_B$ and $OUT2_B$ are high.
It is recommended to use $R_{CLA} = R_{CLB}$.

In this configuration, the resulting bridge has the following characteristics.

- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$ 0.37Ω Typ. Value @ T_J = 25°C
- 1.4A max RMS Load Current
- 2.8A max OCD Threshold

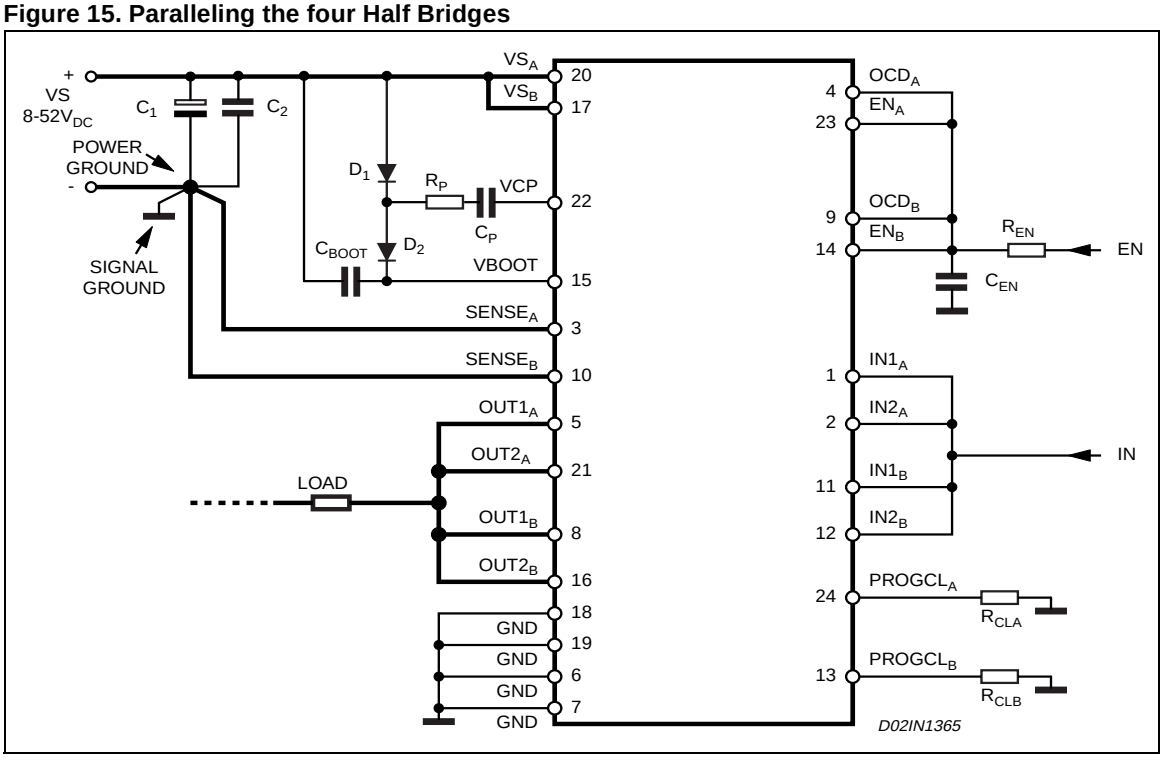
Figure 14. Parallel connection with lower Overcurrent Threshold



It is also possible to parallel the four Half Bridges to obtain a simple Half Bridge as shown in Fig. 15. In this configuration the, the over current threshold is equal to twice the minimum threshold set by the resistors R_{CLA} or R_{CLB} in Figure 15. It is recommended to use $R_{CLA} = R_{CLB}$.

The resulting half bridge has the following characteristics.
- Equivalent Device: HALF BRIDGE
- $R_{DS(ON)}$ 0.18Ω Typ. Value @ T_J = 25°C
- 2.8A max RMS Load Current
- 5.6A max OCD Threshold

Figure 15. Paralleling the four Half Bridges



OUTPUT CURRENT CAPABILITY AND IC POWER DISSIPATION

In Fig. 16 and Fig. 17 are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

– One Full Bridge ON at a time (Fig.16) in which only one load at a time is energized.

– Two Full Bridges ON at the same time (Fig.17) in which two loads at the same time are energized.

For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125°C maximum).

Figure 16. IC Power Dissipation versus Output Current with One Full Bridge ON at a time.

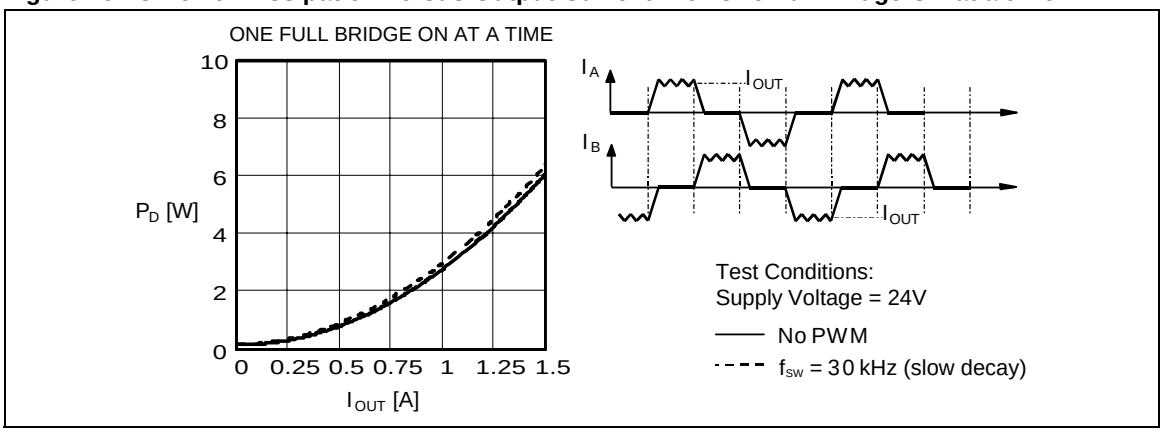
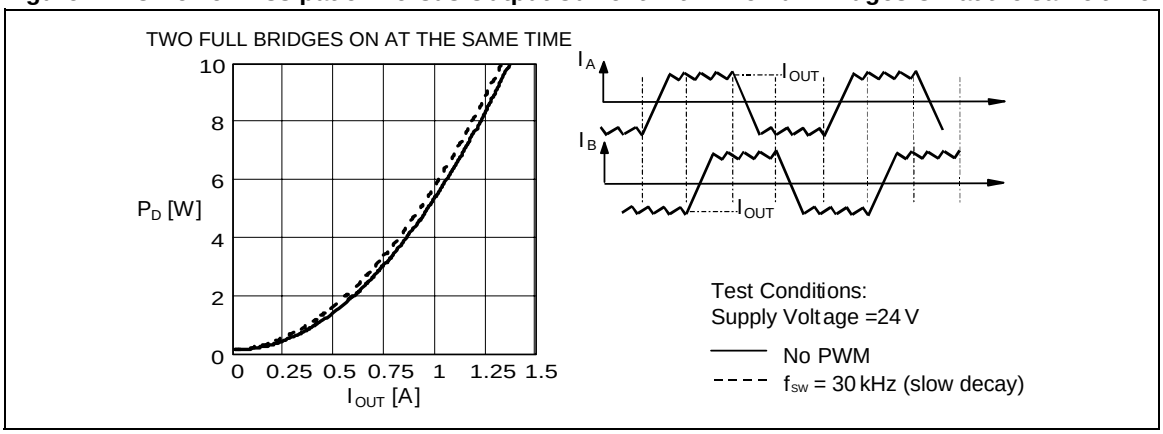


Figure 17. IC Power Dissipation versus Output Current with Two Full Bridges ON at the same time.



THERMAL MANAGEMENT

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be deliver by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Figures 19, 20 and 21 show the Junction-to-Ambient Thermal Resistance values for the PowerSO36, PowerDIP24 and SO24 packages.

For instance, using a PowerSO package with copper slug soldered on a 1.5 mm copper thickness FR4 board with 6cm^2 dissipating footprint (copper thickness of 35µm), the $R_{th\ j\text{-}amb}$ is about 35°C/W. Fig. 18 shows mounting methods for this package. Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15°C/W.

Figure 18. Mounting the PowerSO package.

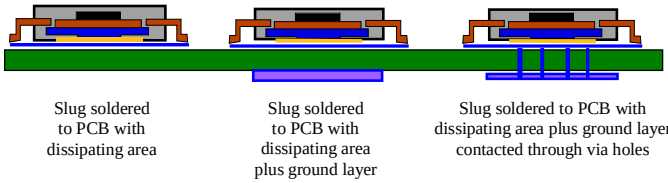


Figure 19. PowerSO36 Junction-Ambient thermal resistance versus on-board copper area.

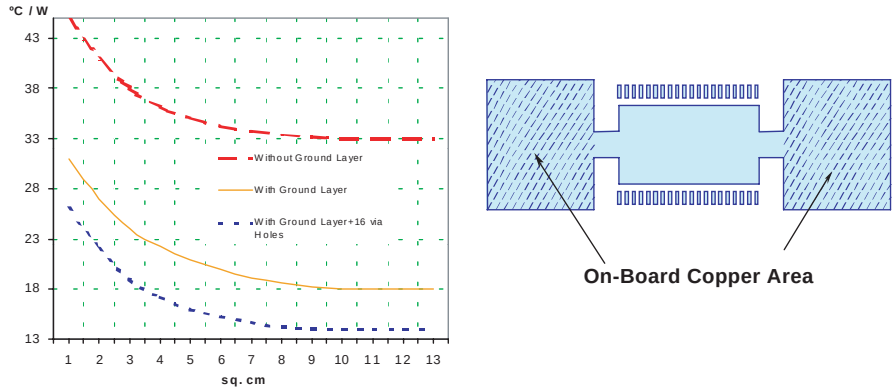


Figure 20. PowerDIP24 Junction-Ambient thermal resistance versus on-board copper area.

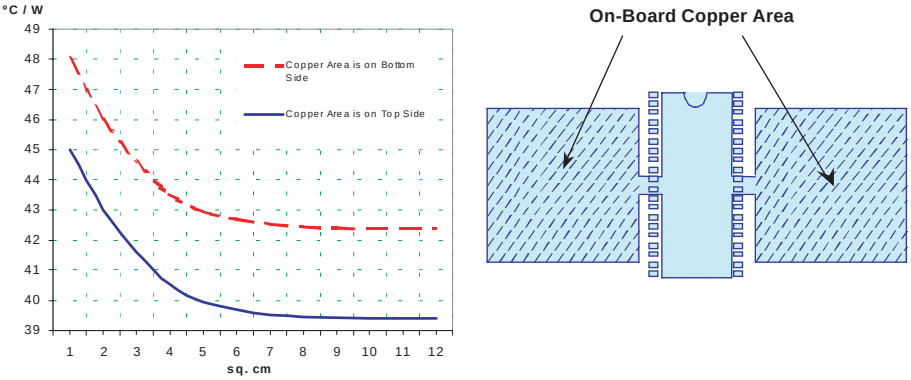
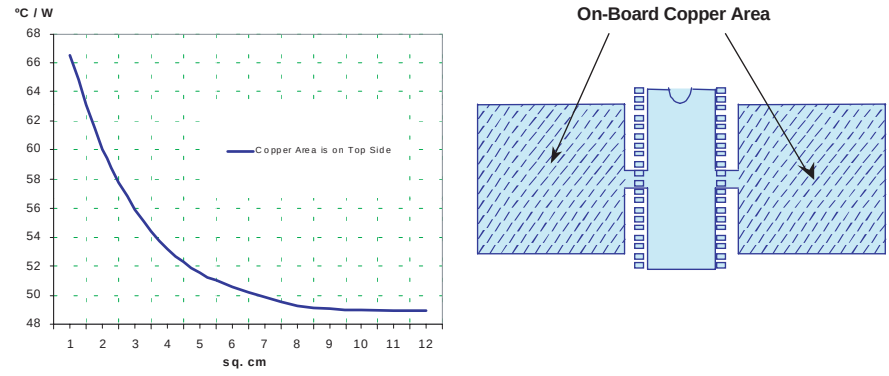


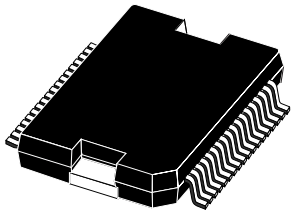
Figure 21. SO24 Junction-Ambient thermal resistance versus on-board copper area.



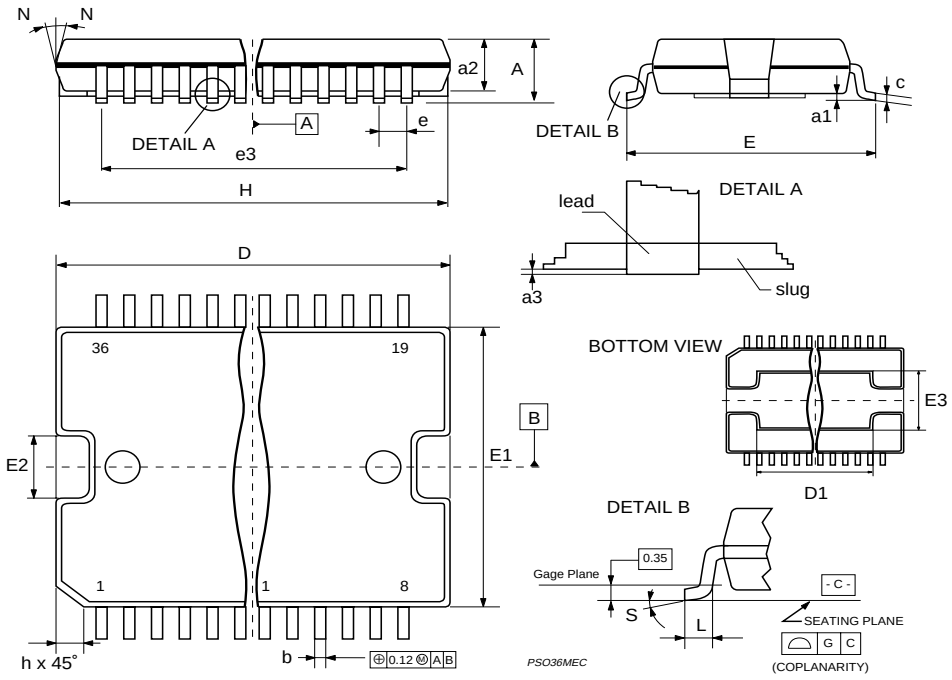
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8 °(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA

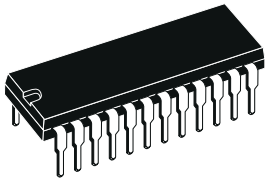


PowerSO36

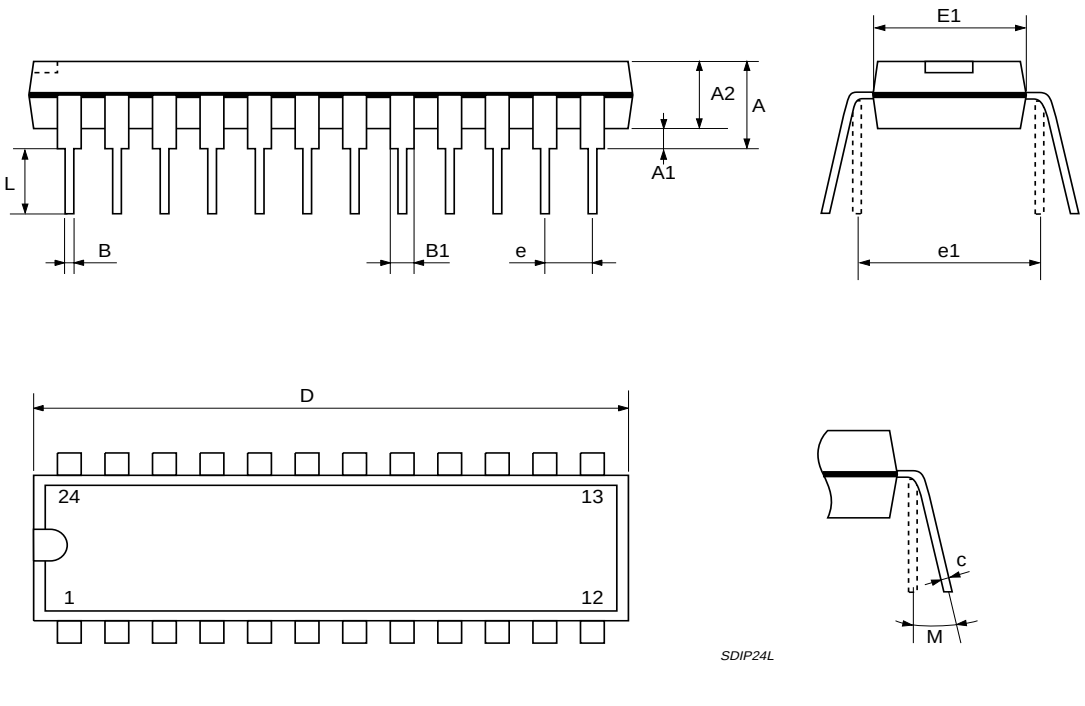


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.320			0.170
A1	0.380			0.015		
A2		3.300			0.130	
B	0.410	0.460	0.510	0.016	0.018	0.020
B1	1.400	1.520	1.650	0.055	0.060	0.065
c	0.200	0.250	0.300	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.620		8.260	0.300		0.325
e		2.54			0.100	
E1	6.350	6.600	6.860	0.250	0.260	0.270
e1		7.620			0.300	
L	3.180		3.430	0.125		0.135
M	0° min, 15° max.					

OUTLINE AND MECHANICAL DATA



Powerdip 24

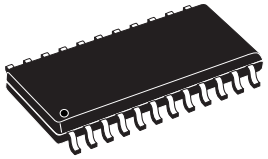


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0;75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

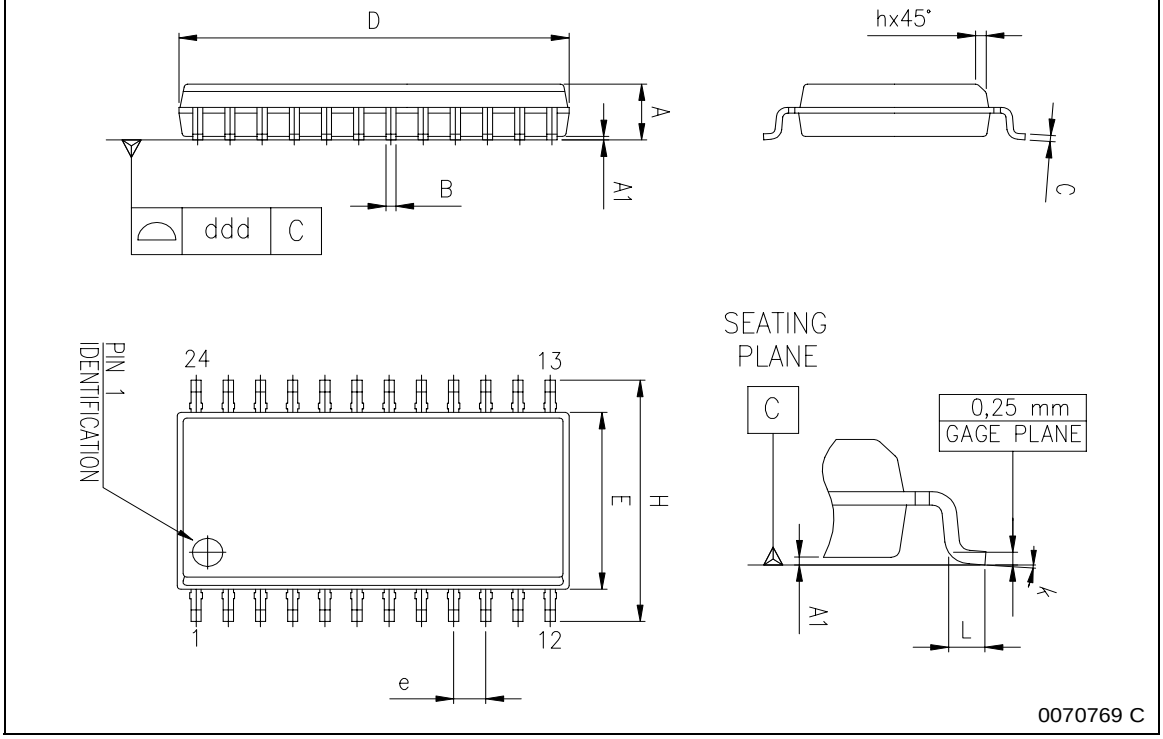
(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

Weight: 0.60gr



SO24



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