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**CONVOLUTIONAL ENCODER**

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**VITERBI DECODER**

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**STEL-5269**

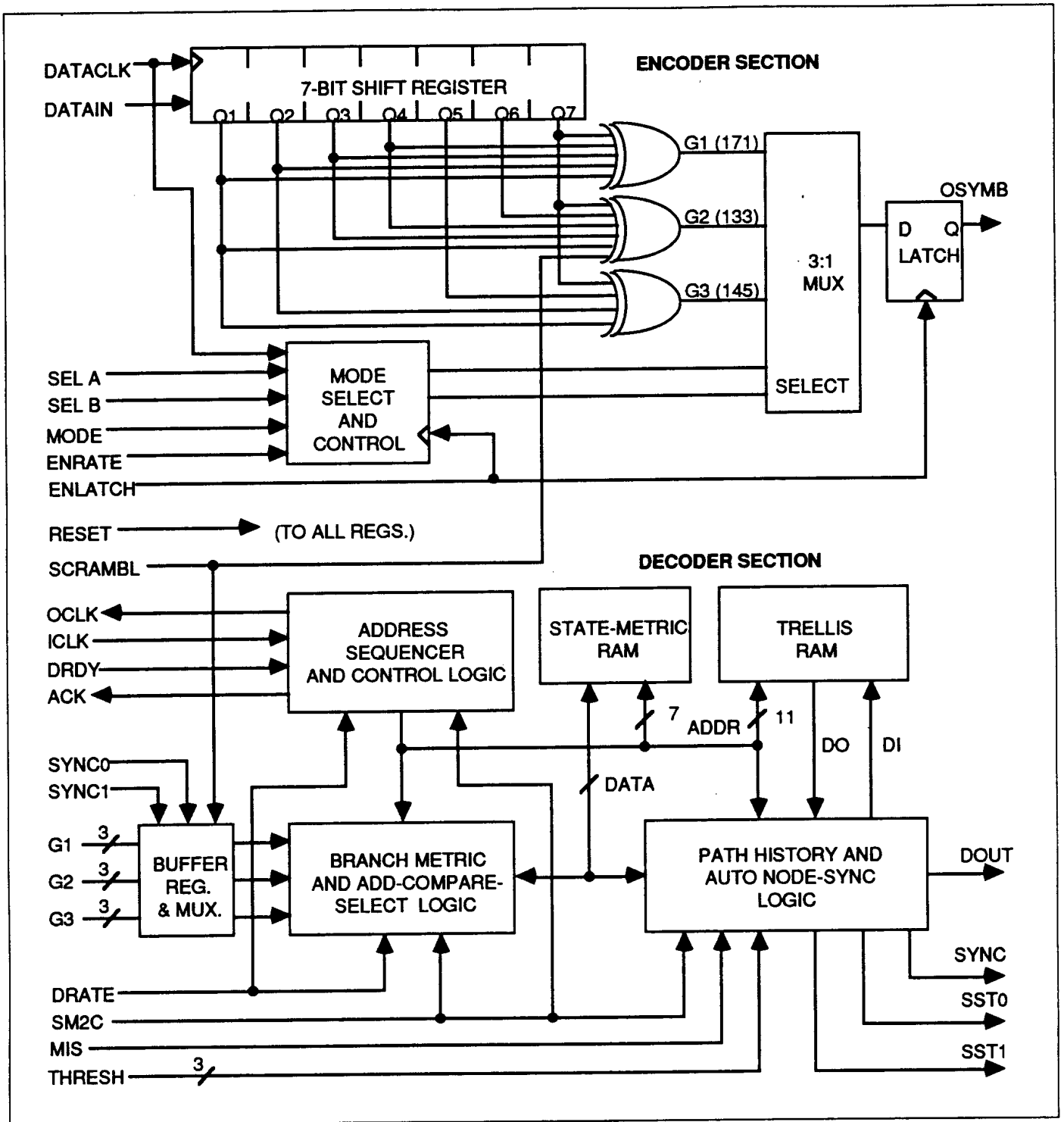
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# BLOCK DIAGRAM



## FEATURES

- CONSTRAINT LENGTH 7
- RATE  $1/3$  AND  $1/2$
- THREE BIT SOFT-DECISION IN SIGNED MAGNITUDE OR 2'S COMPLEMENT FORMAT
- UP TO 256 Kbps DATA RATE ( $0^\circ$  to  $70^\circ$  C)
- CODING GAIN OF 5.2 dB (AT  $10^{-5}$  BER, RATE  $1/2$ )
- CODING GAIN OF 6.0 dB (AT  $10^{-5}$  BER, RATE  $1/3$ )
- BOTH ENCODING AND DECODING FUNCTIONS PERFORMED
- INDUSTRY STANDARD POLYNOMIALS  
G1=171<sub>8</sub>, G2=133<sub>8</sub>, G3=145<sub>8</sub>,
- LOW POWER CONSUMPTION
- SINGLE 5V SUPPLY
- 44 PIN PLCC PACKAGE
- COMMERCIAL AND MILITARY TEMPERATURE RANGES AVAILABLE
- AVAILABLE TO MIL-STD 883C

## FUNCTIONAL DESCRIPTION

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-5269 is a specialized product designed to perform this specific communications related function.

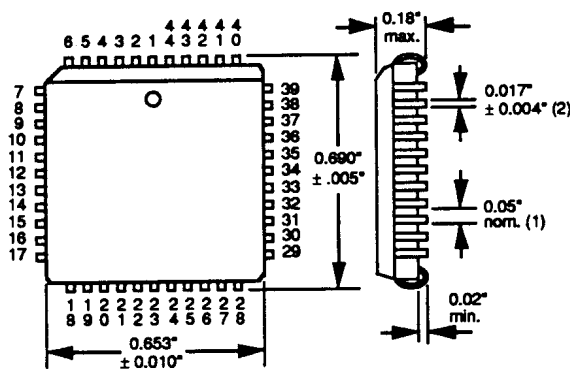
The encoder creates a stream of symbols which are transmitted at 2 (Rate  $1/2$ ) or 3 (Rate  $1/3$ ) times the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of information despite a high symbol error rate resulting from a noisy link.

The STEL-5269 incorporates all the memories required to perform these functions. The STEL-5269 is available in a 44-pin PLCC (plastic leaded chip carrier) and also in a ceramic leaded chip carrier (J-bend leads).

## PIN CONFIGURATION

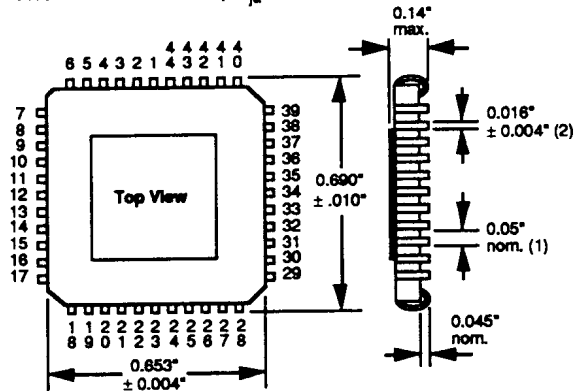
Package: 44 pin PLCC

Thermal coefficient,  $\theta_{ja} = 40^\circ\text{C/W}$



Package: 44 pin CLDCC

Thermal coefficient,  $\theta_{ja} = 50^\circ\text{C/W}$



Notes: (1) Tolerances on pin spacing are not cumulative

(2) Dimensions apply at seating plane

(3) PLCC and CLDCC packages have different corners and may not fit into sockets designed for the other type. Universal sockets are available without alignment locators

## PIN CONNECTIONS

1 SYNC	12 MIS	23 V <sub>SS</sub>	34 V <sub>SS</sub>
2 V <sub>SS</sub>	13 DOUT	24 THRESH <sub>0</sub>	35 SST1
3 ACK	14 OSYMB	25 THRESH <sub>1</sub>	36 SYNC1
4 DATACLK	15 G2D0	26 RESET	37 SST0
5 DRDY	16 G2D1	27 DRATE	38 SYNC0
6 DATAIN	17 G2D2	28 SEL A	39 SEL B
7 G3D0	18 G1D0	29 THRESH <sub>2</sub>	40 SM2C
8 G3D1	19 G1D1	30 V <sub>DD</sub>	41 ICLK
9 G3D2	20 G1D2	31 V <sub>SS</sub>	42 OCLK
10 MODE	21 ENLATCH	32 I.C.	43 SCRAMBL
11 V <sub>SS</sub>	22 V <sub>DD</sub>	33 ERATE	44 I.C.

Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

# FUNCTION BLOCK DESCRIPTION

## ENCODER

The convolutional coder is functionally independent of the decoder. A single data bit is clocked into the 7-bit shift register on the rising edge of **DATA CLK**. There are two modes of operation, controlled by the **MODE** input. When **MODE** is low the timing of the **SEL A**, **SEL B** and **ENLATCH** signals determine whether 2 or 3 symbol bits are generated for every data bit. When **MODE** is high the symbols are automatically generated sequentially every clock cycle. In this case, the state of **ENRATE** determines whether the device generates symbols for Rate  $1/2$  or Rate  $1/3$  operation. The symbols **G1**, **G2**, and **G3** are generated from the modulo-2 sum (exclusive-OR) of the inputs to the 3 generators from the taps on the shift register. The 3 polynomials are  $171_8$  (**G1**),  $133_8$  (**G2**), and  $145_8$  (**G3**). Example inputs are shown in the timing diagram for both rate  $1/2$  and rate  $1/3$  operation.

## DECODER

The STEL-5269 is designed to accept symbols either synchronously or in a handshake mode. Symbols are latched into the decoder input registers on the falling edge of the **DRDY** input. **ACK** is returned by the decoder to indicate that the symbols have been accepted.

The **RATE** input determines whether the decoder will operate in Rate  $1/2$  or Rate  $1/3$  mode. When operating at Rate  $1/2$  the **G3** symbol is ignored by the decoder.

For hard decision binary symbols the **G1**, **G2**, **G3** symbol bits should be connected to pins **G1D2**, **G2D2** and **G3D2** respectively, and the other symbol input pins should be tied high ( $V_{DD}$ ). Three-bit soft decision symbols may be input in Signed Magnitude or Inverted Two's Complement code, according to the setting of the code control pin, **SM2C**. The code should be set to Signed Magnitude when using hard decision data.

A single decoded data bit is output for every set of input symbols. The data bit corresponding to a particular symbol set will be output after a delay of 42 symbols. Therefore, when using the STEL-5269 to decode blocks of data 42 additional dummy symbols and 42 **DRDY** signals need to be added to the data stream to flush the last 42 decoded data bits out of the decoder.

Node synchronization (correctly grouping incoming symbols into **G1**, **G2**, and **G3** sets) is inherent with many communication techniques such as TDMA and

spread spectrum systems. If node synchronization is not an inherent property of the communications link then the internal auto node sync circuit can be used to do this. This is accomplished by connecting the node sync outputs (**SST0** and **SST1**) to the node sync inputs (**SYNC0** and **SYNC1**). The threshold for determining the out of sync condition is user selectable by means of the **THRESH<sub>2,4</sub>** inputs. Alternatively, the **SYNC0** and **SYNC1** pins can be used with an external algorithm to achieve the same result.

Further information on the theory of operation of Viterbi decoders may be obtained from text books such as "Error-Correcting Codes", by Peterson and Weldon (MIT Press), or "Error Control Coding", by Lin and Costello (Prentice-Hall). An alternative source of information is the many papers on this subject that have appeared in the IEEE transactions, such as "Convolutional Codes and their Performance in Communication Systems", by Dr. A. J. Viterbi, IEEE Trans. on Communications Technology, October 1971.

## INPUT SIGNALS

### RESET

Asynchronous master **Reset**. A logic low on this pin will clear all registers on the STEL-5269 in both the encoder and decoder sections of the chip. **RESET** should remain low for at least 3 cycles of **ICLK**.

### DATACLK

This is the encoder Shift Register Clock. A rising edge on this clock latches **DATAIN** into the encoder shift register. This signal should nominally be a square wave with a maximum frequency of 256 KHz.

### DATAIN

This is the encoder input. The data present at this pin is latched into the encoder shift register on the rising edge of **DATACLK**. This signal should be stable at the rising edge of **DATACLK**.

### MODE

The state of the **MODE** input determines the method of symbol sequencing in the encoder. When **MODE** is set low the sequencing is generated externally under the control of the **SEL A** and **SEL B** inputs, and when **MODE** is set high it is generated automatically.

### SEL A, SEL B

When **MODE** is set low **SEL A** and **SEL B** select the encoded symbol, G1, G2 or G3, which will appear on the **OSYMB** pin on the next rising edge of **ENLATCH** according to the table:

SEL A	SEL B	SYMBOL	POLYNOMIAL
0	1	G1	171 <sub>8</sub> (1111001 <sub>2</sub> )
1	0	G2	133 <sub>8</sub> (1011011 <sub>2</sub> )
0	0	G3	145 <sub>8</sub> (1100101 <sub>2</sub> )

When **MODE** is set high the symbol sequence is generated automatically and the **SEL A** and **SEL B** inputs are inactive.

### ERATE

When **MODE** is high the Encoder Rate input determines whether symbols for Rate 1/2 (**ERATE=1**) or Rate 1/3 (**ERATE=0**) operation are generated. When **MODE** is low this input is inactive.

### SCRAMBL

When the Scramble input is set high the G2 symbol generated at the encoder and the G2 symbol received at the decoder will be inverted. This ensures that the output symbol stream is not a string of zeroes when the input data stream is all zeroes, thereby making it easier for the demodulator to recover the clock information under these conditions. When **SCRAMBL** is set low the normal symbol stream is generated.

### ENLATCH

This is the encoder Output Latch Enable. The new symbol is clocked into the output latch and appears on the **OSYMB** pin on the rising edge of **ENLATCH**. When **MODE** is low the symbol selected will depend on the states of the **SEL A** and **SEL B** lines, which should be stable on the rising edge of **ENLATCH**. When **MODE** is high the symbol selection is internal, and the frequency of the **ENLATCH** signal should be 2 or 3 times the frequency of the **DATACLK**, depending on the rate selected.

### ICLK, OCLK

System Clock. A crystal may be connected between **ICLK** and **OCLK** or a CMOS level clock may be fed into **ICLK** only. The clock frequency should be at least 70 times the data rate but no more than 18 MHz.

### DRATE

The Decoder Rate input selects whether the decoder will read two symbols (**DRATE** set high) or three symbols (**DRATE** set low) for every data bit decoded.

During rate 1/2 operation the symbol G3 on inputs **G3D2-G3D0** is completely ignored by the decoder.

### G1D2-G1D0, G2D2-G2D0, G3D2-G3D0

The three 3-bit soft decision symbols are connected to these inputs and loaded into the input registers on the falling edge of **DRDY**. The order in which the symbols are entered into the decoder from the registers depends on the state of the **SYNC0** and **SYNC1** inputs. The decoder can make use of soft decision information, which includes both polarity information and a confidence measure, to improve the decoder performance. If hard decision (single bit) symbols are used the signals are connected to pins **G1D2**, **G2D2** and **G3D2** and the other inputs are connected to  $V_{DD}$ . See **SM2C** for a description of the input data codes.

### DRDY

The Data Ready signal is used to load symbols into the decoder. This signal is edge triggered and a new set of symbols is latched into the input registers on each falling edge of the **DRDY** input.

### SM2C

The state of the Signed Magnitude/2's Complement input determines the format of the incoming soft-decision symbols into the decoder. When **SM2C** is high the input code is Signed Magnitude, and when it is low the code is Two's Complement. The codes are shown in the following table:

CODE CONTROL: SYMBOL INPUT:	SM2C=1 GXD2-GXD0	SM2C=0 GXD2-GXD0
Most Confident '+' level Data = 0	0 1 1	0 1 1
	0 1 0	0 1 0
	0 0 1	0 0 1
Least Confident '+' level	0 0 0	0 0 0
Least Confident '-' level Data = 1	1 0 0	1 1 1
	1 0 1	1 1 0
	1 1 0	1 0 1
Most Confident '-' level	1 1 1	1 0 0

**SM2C** should be set high when using hard decision data.

### SYNC0, SYNC1

The Symbol **Sync0** and Symbol **Sync1** inputs are used for auto node sync operation. When using the internal auto node sync mode these two pins are connected to **SST0** and **SST1**, respectively. The operation of the decoder is affected in the following way by the **SYNC0** and **SYNC1** inputs:

RATE	SYNC0	SYNC1	Symbol entered into decoder during symbol period N		
			G1	G2	G3
1	0	0	G1 <sub>N</sub>	G2 <sub>N</sub>	–
1	1	0	G2 <sub>N-1</sub>	G1 <sub>N</sub>	–
1	0	1	G2 <sub>N</sub>	G1 <sub>N</sub>	–
1	1	1	Invalid state		
0	0	0	G1 <sub>N</sub>	G2 <sub>N</sub>	G3 <sub>N</sub>
0	1	0	G3 <sub>N-1</sub>	G1 <sub>N</sub>	G2 <sub>N</sub>
0	0	1	G2 <sub>N-1</sub>	G3 <sub>N-1</sub>	G1 <sub>N</sub>
0	1	1	Invalid state		

Note that whenever the states of the **SYNC0** and **SYNC1** inputs are changed there will be a delay of 42 bit periods before valid data starts appearing at **DOUT**.

### MIS

Two algorithms for auto node-sync are incorporated into the STEL-5269. When **MIS** is set high the Traceback Mismatch algorithm is selected, and when **MIS** is set low the Metric Renormalization algorithm is selected.

### THRESH<sub>2,0</sub>

A counter is used to determine the number of either traceback mismatches or metric renormalizations per 256 bits in the auto node-sync circuit, and the threshold at which the counter triggers the **SST0** and **SST1** outputs to change states is set with the data on the **THRESH<sub>2,0</sub>** inputs. The threshold values will be as shown in the table below.

THRESH <sub>2,0</sub>	Threshold value
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Since the actual error rate obtained will depend on the signal to noise ratio ( $E_b/N_o$ ) in the signal, the optimum value of the threshold will also depend on  $E_b/N_o$  and should be set accordingly. Suggested initial values for **THRESH<sub>2,0</sub>** are 5 for the Mismatch algorithm and 3 for the Renormalization algorithm.

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## OUTPUT SIGNALS

### OSYMB

Output Symbol from the Encoder. This output depends on the seven most recent data bits (**DATAIN**) clocked into the encoder shift register and on the select lines **SEL A** and **SEL B**. The individual symbols are formed by the modulo-2 sum of the inputs to the generators from the 7-bit shift register.

### ACK

A low level pulse on the Acknowledge pin indicates that the decoder has input the current set of two or three symbols. The signal will pulse low between 68 and 69 clock cycles after the falling edge of **DRDY**.

### DOUT

Decoded Data Out. The signal is latched into the output register on the falling edge of **DRDY**. There is a delay of 42 data bits from the time a set of symbols is input to the time the corresponding data bit is output. Consequently, in order to flush the last 42 bits of data out of the system at the end of a burst it is necessary to continue pulsing the **DRDY** line for 42 symbol periods after the last valid symbol has been entered.

### SST0, SST1

The Sync State 0 and Sync State 1 signals are the outputs of the internal auto node sync circuit. They should be connected to **SYNC0** and **SYNC1** respectively to use the internal auto node sync capability. They may also be used in conjunction with an external node sync algorithm implementation which can use the **SST0** and **SST1** outputs.

### SYNC

The Sync output provides an indication of the status of the internal auto node sync circuit. When it is high it indicates that node sync has been lost, and when it is low it indicates that the system is assumed to be in sync, as determined by the error rate estimate.

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to  $V_{SS}$ .

Symbol	Parameter	Range	Units
$T_{stg}$	Storage Temperature	$\begin{cases} -40 \text{ to } +125 \\ -65 \text{ to } +150 \end{cases}$	$^{\circ}\text{C}$ (Plastic package) $^{\circ}\text{C}$ (Ceramic package)
$V_{DDmax}$	Supply voltage on $V_{DD}$	-0.3 to +7	volts
$V_{I(max)}$	Input voltage	-0.3 to $V_{DD}+0.3$	volts
$I_I$	DC input current	$\pm 10$	mA

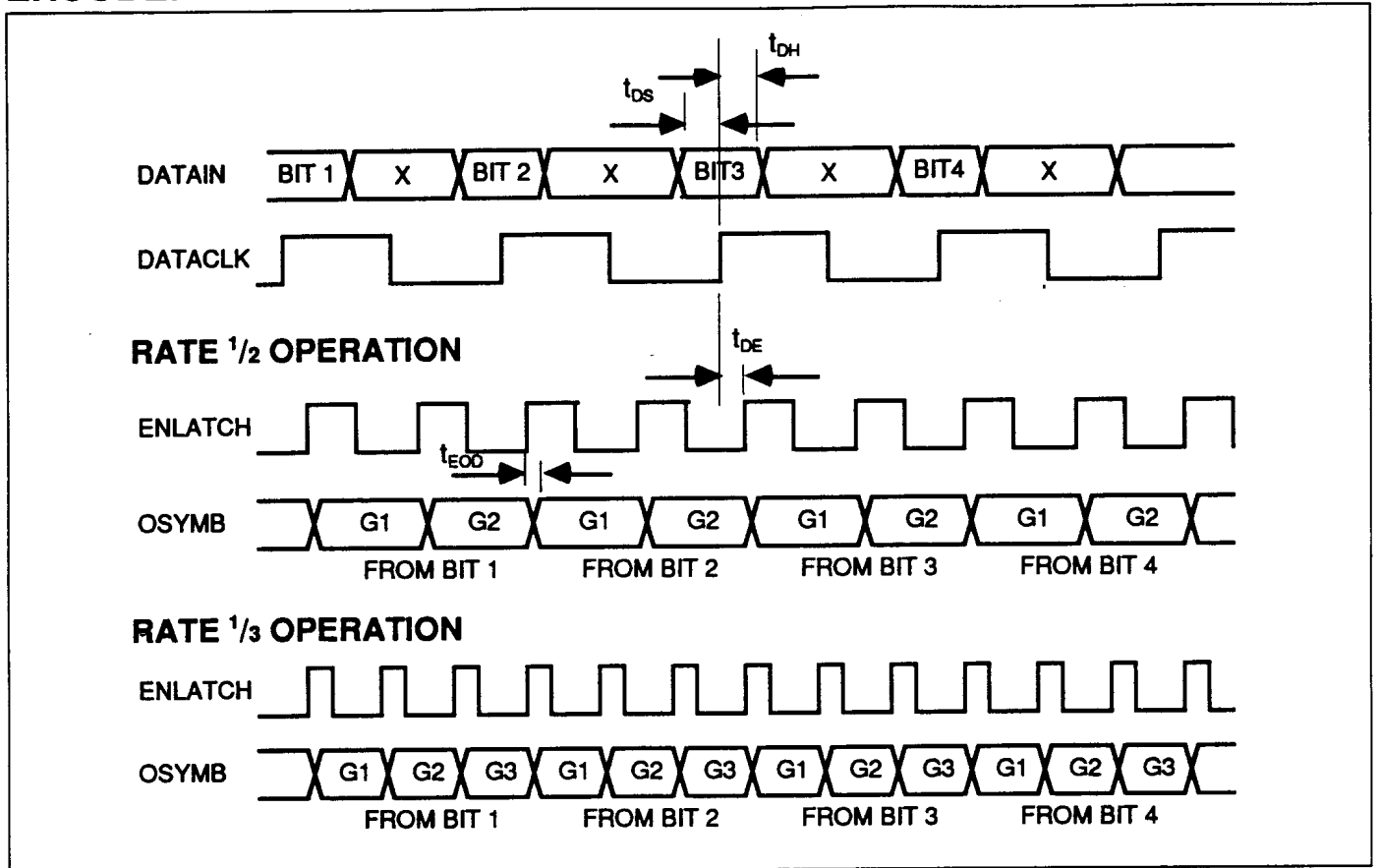
### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
$V_{DD}$	Supply Voltage	$\begin{cases} +5 \pm 5\% \\ +5 \pm 10\% \end{cases}$	Volts (Commercial grade) Volts (Military grade)
$T_a$	Operating Temperature (Ambient)	$\begin{cases} 0 \text{ to } +70 \\ -55 \text{ to } +125 \end{cases}$	$^{\circ}\text{C}$ (Commercial grade) $^{\circ}\text{C}$ (Military grade)

**D.C. CHARACTERISTICS** (Operating Conditions:  $V_{DD}=5.0\text{ V} \pm 5\%$ ,  $V_{SS}=0\text{ V}$ ,  $T_a=0^{\circ}\text{ C}$  to  $70^{\circ}\text{ C}$ , Commercial  
 $V_{DD}=5.0\text{ V} \pm 10\%$ ,  $V_{SS}=0\text{ V}$ ,  $T_a=-55^{\circ}\text{ C}$  to  $125^{\circ}\text{ C}$ , Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
$I_{DD}$	Supply Current, Operational			2.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	$\mu\text{A}$	DRDY, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	-130	-45	-15	$\mu\text{A}$	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	$I_O = -6.0\text{ mA}$
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	$I_O = +6.0\text{ mA}$
$I_{OS}$	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$ , $V_{DD} = \text{max}$
		-10	-45	-130	mA	$V_{OUT} = V_{SS}$ , $V_{DD} = \text{max}$
$C_{IN}$	Input Capacitance		2		pF	All inputs
$C_{OUT}$	Output Capacitance		4		pF	All outputs

## ENCODER TIMING. MODE=1



## ENCODER ELECTRICAL CHARACTERISTICS

**A.C. CHARACTERISTICS** (Operating Conditions:  $V_{DD}=5.0\text{ V} \pm 5\%$ ,  $V_{SS}=0\text{ V}$ ,  $T_a=0^\circ\text{ to }70^\circ\text{ C}$ , Commercial  
 $V_{DD}=5.0\text{ V} \pm 10\%$ ,  $V_{SS}=0\text{ V}$ ,  $T_a=-55^\circ\text{ to }125^\circ\text{ C}$ , Military)

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
$t_{RS}$	RESET pulse width	$3 \cdot t_{CLK}$		$3 \cdot t_{CLK}$		nsec.
$t_{SR}$	RESET to ICLK setup	2		3		nsec.
$t_{DS}$	DATAIN to DATACLK setup	10		12		nsec.
$t_{DH}$	DATAIN to DATACLK hold	10		12		nsec.
$t_{SS}$	SEL A or SEL B to ENLATCH setup	10		12		nsec.
$t_{SH}$	SEL A or SEL B to ENLATCH hold	5		8		nsec.
$t_{DE}$	DATACLK to ENLATCH delay	10		12		nsec.
$t_{EOD}$	ENLATCH to OSYMB stable delay		10		12	nsec.

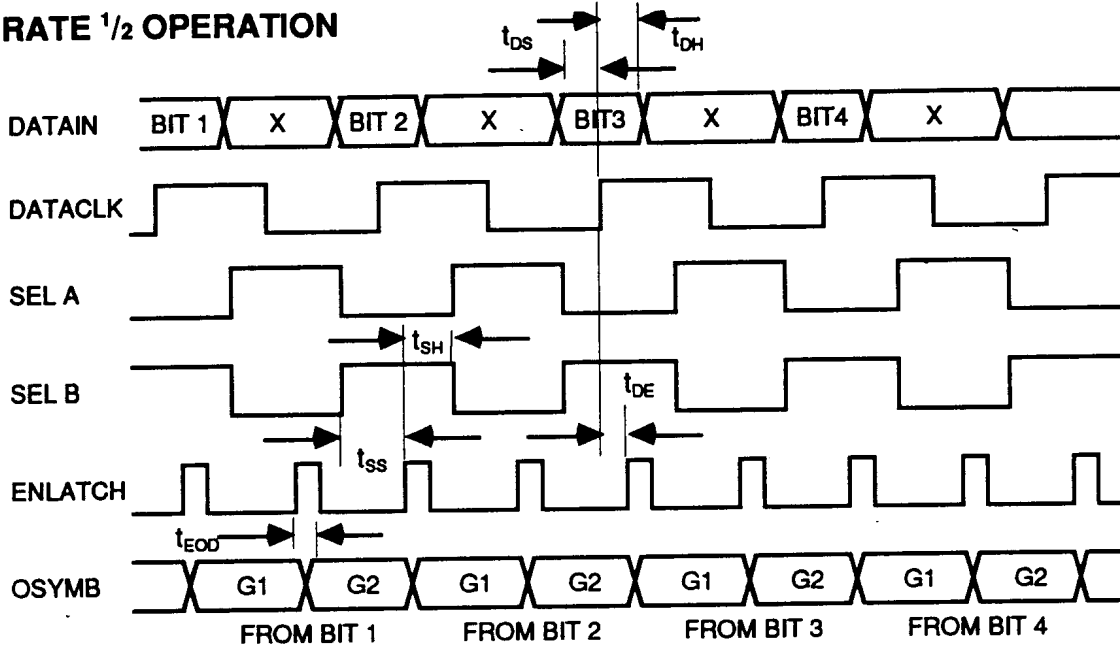
Notes:  $t_{CLK}$  = Period of ICLK  $= (1 / f_{CLK})$ .

$t_{SR}$  is only relevant if operation is to commence during the first clock cycle after RESET goes high.

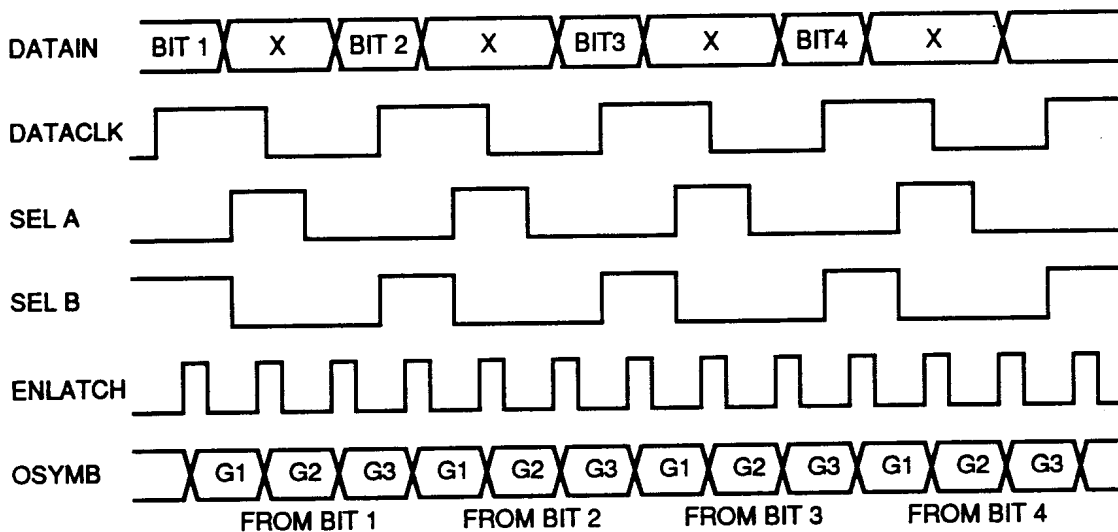


## ENCODER TIMING. MODE=0 (STEL-5268 EMULATION MODE)

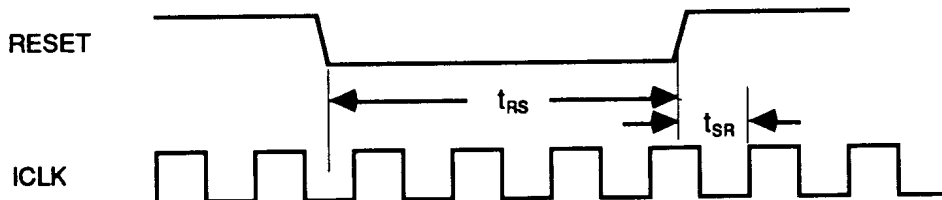
### RATE 1/2 OPERATION



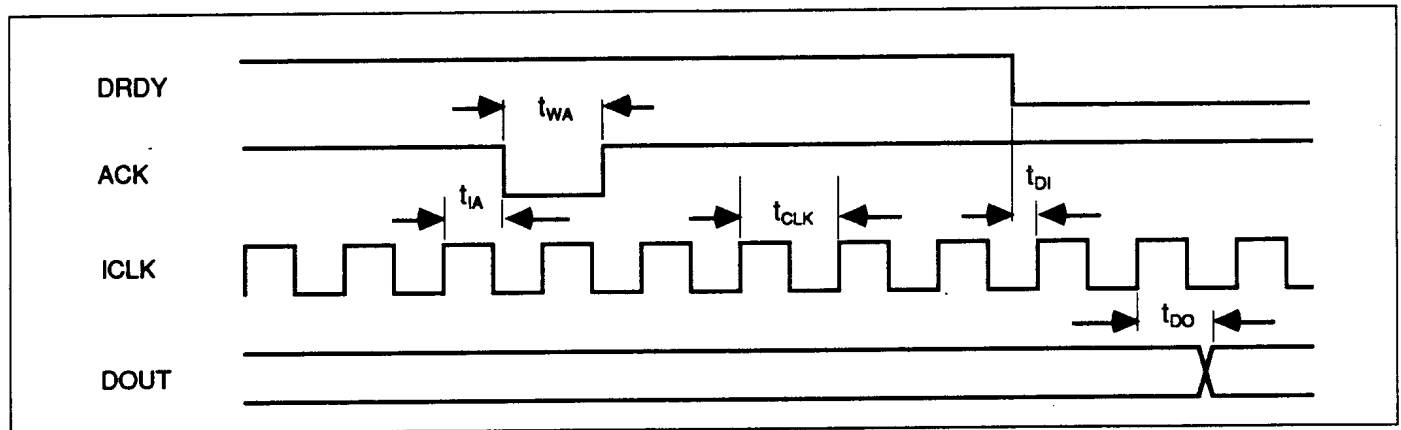
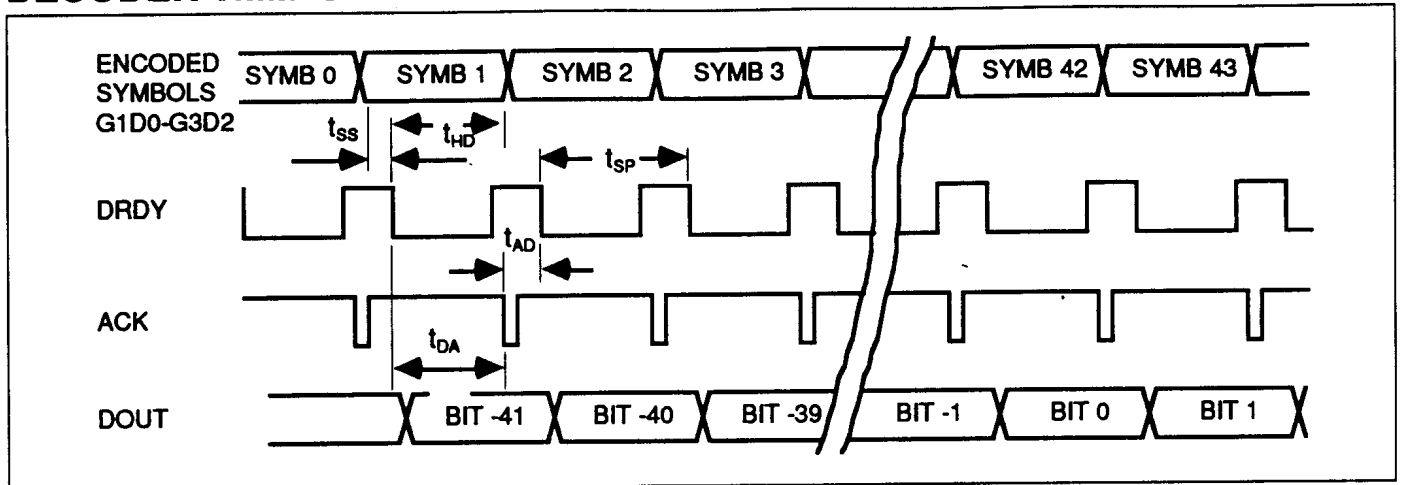
### RATE 1/3 OPERATION



## RESET TIMING



## DECODER TIMING



## DECODER ELECTRICAL CHARACTERISTICS

**A.C. CHARACTERISTICS** (Operating Conditions:  $V_{DD}=5.0\text{ V} \pm 5\%$ ,  $V_{SS}=0\text{ V}$ ,  $T_a=0^\circ\text{ to }70^\circ\text{ C}$ , Commercial  
 $V_{DD}=5.0\text{ V} \pm 10\%$ ,  $V_{SS}=0\text{ V}$ ,  $T_a=-55^\circ\text{ to }125^\circ\text{ C}$ , Military)

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
$f_{CLK}$	ICLK Frequency	$70 \cdot f_{DRDY}$	18	$70 \cdot f_{DRDY}$	14	MHz
$t_{SS}$	SYMBOL to DRDY setup	20		25		nsec.
$t_{HD}$	SYMBOL to DRDY hold	5		8		nsec.
$t_{SP}$	SYMBOL Period	3.9		5		$\mu\text{sec.}$
$t_{DA}$	DRDY to ACK	$35 + 68 \cdot t_{CLK}$	$30 + 69 \cdot t_{CLK}$	$35 + 68 \cdot t_{CLK}$	$30 + 69 \cdot t_{CLK}$	nsec.
$t_{AD}$	ACK to DRDY	$2 \cdot t_{CLK}$		$2 \cdot t_{CLK}$		nsec.
$t_{WA}$	ACK pulse width	$t_{CLK}$		$t_{CLK}$		nsec.
$t_{DI}$	DRDY to ICLK setup	5		8		nsec.
$t_{IA}$	ICLK to ACK	10	31			nsec.
$t_{DO}$	ICLK to DOUT	10	35			nsec.
$t_{SR}$	RESET to ICLK setup	2		3		nsec.

Notes:  $f_{DRDY}$  = Frequency of DRDY,  $t_{CLK}$  = Period of ICLK  $(=1/f_{CLK})$ .

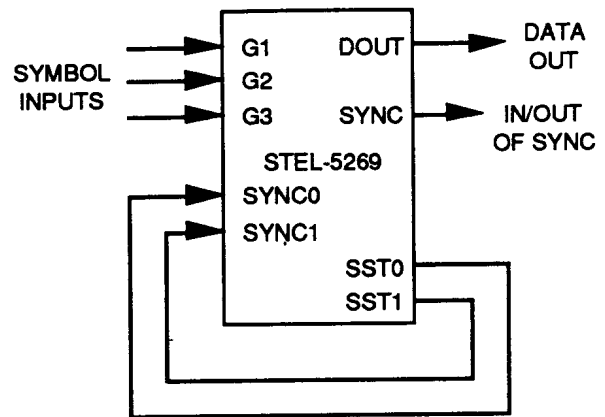
$t_{SR}$  is only relevant if operation is to commence during the first clock cycle after RESET goes high.

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# APPLICATION INFORMATION -

## USING AUTOMATIC NODE SYNC

The automatic node sync circuit built into the STEL-5269 can be used to provide node sync in applications where this is not intrinsic to the nature of the operation. The automatic node sync is enabled by connecting the SST1 and SST0 outputs to the SYNC1 and SYNC0 inputs, as shown below. The threshold should be set according to the expected signal to noise ratio of the input signal for optimum operation of the system.



## BPSK COMMUNICATION SYSTEM USING CONVOLUTIONAL ENCODING AND VITERBI DECODING. RATE = 1/2

The STEL-5269 can be used in a variety of different environments. One example is shown below. It cannot be used as a common encoder or decoder in multi-channel applications because of memory incorporated on the chip which is dedicated to a single channel.

An example of a system using the convolutional coder and Viterbi decoder is illustrated here. The system modulates a data stream of rate 512 Kbps using binary PSK (BPSK). To be able to use convolutional coding/decoding, the system must have available the additional bandwidth needed to transmit symbols at twice the data rate (for rate 1/2 encoding). Alternatively, the system could make use of two parallel channels to transmit two streams of symbols at the data rate. The performance improvement that can be expected is shown in the graph below.

The convolutional encoder is functionally independent from the decoder. A single data bit is clocked into the 7 bit shift register on the rising edge of DATA CLK. The decoder portion of the STEL-5269 is designed to accept symbols synchronously. DRDY is supplied by the user to clock in the symbols. The maximum data rate is 256 Kbps, using a clock frequency of 18 MHz. This corresponds to 512 K symbols per second at rate 1/2 and 768 K symbols per second at rate 1/3. 18 MHz crystals are readily available, and this clock frequency can be used at all data rates, although the power consumption can be reduced by using lower clock frequencies.

