

### IXDF502 / IXDI502 / IXDN502 2 Ampere Dual Low-Side Ultrafast MOSFET Drivers

#### Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS<sup>™</sup> processes
- Latch-Up Protected up to 2 Amps
- High 2A Peak Output Current
- Wide Operating Range: 4.5V to 30V
- -55°Cto+125°CExtendedOperating Temperature
- High Capacitive Load Drive Capability: 1000pF in <10ns</li>
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current
- Two Drivers in Single Chip

### Applications

- Driving MOSFETs and IGBTs
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Class D Switching Amplifiers
- Power Charge Pumps

#### **General Description**

The IXDF502, IXDI502 and IXDN502 each consist of two 2-Amp CMOS high speed MOSFET Gate Drivers for driving the latest IXYS MOSFETs & IGBTs. Each of the Dual Outputs can source and sink 2 Amps of Peak Current while producing voltage rise and fall times of less than 15ns. The input of each Driver is TTL or CMOS compatible and is virtually immune to latch up. Patented\* design innovations eliminate cross conduction and current "shoot-through". Improved speed and drive capabilities are further enhanced by very quick & matched rise and fall times.

The IXDF502 is configured with one Gate Driver Inverting plus one Gate Driver Non-Inverting. The IXDI502 is configured as a Dual Inverting Gate Driver, and the IXDN502 is configured as a Dual Non-Inverting Gate Driver.

The IXDF502, IXDI502 and IXDN502 are each available in the 8-Pin P-DIP (PI) package, the 8-Pin SOIC (SIA) package, and the 6-Lead DFN (D1) package, (which occupies less than 65% of the board area of the 8-Pin SOIC).

\*United States Patent 6,917,227

Part Number	Description	Package Type	Packing Style	Pack Qty	Configuration	
IXDF502PI	2A Low Side Gate Driver I.C.	8-Pin PDIP	Tube	50	Dual, with one	
IXDF502SIA	2A Low Side Gate Driver I.C.	8-Pin SOIC	Tube	94	Driver Inverting	
IXDF502SIAT/R	2A Low Side Gate Driver I.C.	8-Pin SOIC	13" Tape and Reel	2500	and one Driver	
IXDF502D1	2A Low Side Gate Driver I.C.	6-Lead DFN	2" x 2" Waffle Pack	56	Non-Inverting	
IXDF502D1T/R	2A Low Side Gate Driver I.C.	6-Lead DFN	13" Tape and Reel	2500	5	
IXDI502PI	2A Low Side Gate Driver I.C.	8-Pin PDIP	Tube	50		
IXDI502SIA	2A Low Side Gate Driver I.C.	8-Pin SOIC	Tube	94	Dual, with both	
IXDI502SIAT/R	2A Low Side Gate Driver I.C.	8-Pin SOIC	13" Tape and Reel	2500	Drivers	
IXDI502D1	2A Low Side Gate Driver I.C.	6-Lead DFN	2" x 2" Waffle Pack	56	Inverting	
IXDI502D1T/R	2A Low Side Gate Driver I.C.	6-Lead DFN	13" Tape and Reel	2500		
IXDN502PI	2A Low Side Gate Driver I.C.	8-Pin PDIP	Tube	50		
IXDN502SIA	2A Low Side Gate Driver I.C.	8-Pin SOIC	Tube	94	Dual, with both	
IXDN502SIAT/R	2A Low Side Gate Driver I.C.	8-Pin SOIC	13" Tape and Reel	2500	Drivers Non-	
IXDN502D1	2A Low Side Gate Driver I.C.	6-Lead DFN	2" x 2" Waffle Pack	56	Inverting	
IXDN502D1T/R	2A Low Side Gate Driver I.C.	6-Lead DFN	13" Tape and Reel	2500		

#### Ordering Information

NOTE: All parts are lead-free and RoHS Compliant

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### IXDF502 / IXDI502 / IXDN502

Figure 1 - IXDF502 Inverting + Non-Inverting 2A Gate Driver Functional Block Diagram

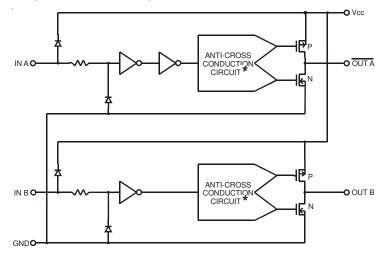


Figure 2 - IXDI502 Dual Inverting 2A Gate Driver Functional Block Diagram

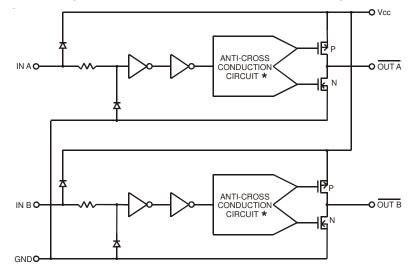
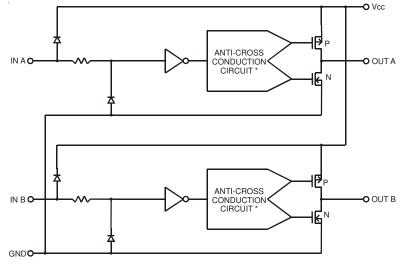


Figure 3 - IXDN502 Dual 2A Non-Inverting Gate Driver Functional Block Diagram



\* United States Patent 6,917,227

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## IXDF502 / IXDI502 / IXDN502

#### Absolute Maximum Ratings (1)

Parameter	Value
Supply Voltage	35V
All Other Pins	-0.3 V to V <sub>cc</sub> + 0.3V
Junction Temperature	150 °C
StorageTemperature	-65 °C to 150 °C
Lead Temperature (10 Sec)	300 °C

#### **Operating Ratings**<sup>(2)</sup>

Parameter	Value		
<b>Operating Supply</b>			4.5V to 30V
Operating Tempera	ature Rang	je	-55 °C to 125 °C
Package Thermal F	Resistance	)*	
8-Pin PDIP	(PI)	$\theta_{IA}$ (typ)	125°C/W
8-PinSOIC	(SIA)	$\theta_{J-A}(typ)$	200 °C/W
6-Lead DFN	(D1)	$\theta_{\downarrow}$ (typ)	125-200 °C/W
6-Lead DFN	(D1)	$\theta_{LC}(max)$	3.3°C/W
6-Lead DFN	(D1)	$\theta_{J-S}(typ)$	7.3°C/W

### Electrical Characteristics @ $\rm T_{A}$ = 25 °C $^{\rm (3)}$

#### Unless otherwise noted, $~4.5V \leq V_{_{CC}} \leq ~30V$ .

All voltage measurements with respect to GND. IXD\_502 configured as described in Test Conditions. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ <sup>(4)</sup>	Max	Units
V <sub>IH</sub>	High input voltage $4.5V \le V_{CC} \le 18V$		3.0			V
VIL	Low input voltage	$4.5V \le V_{CC} \le 18V$			0.8	V
V <sub>IN</sub>	Input voltage range		-5		$V_{CC} + 0.3$	V
I <sub>IN</sub>	Input current	$0V \le V_{IN} \le V_{CC}$	-10		10	μA
V <sub>OH</sub>	High output voltage		V <sub>CC</sub> - 0.025			V
V <sub>OL</sub>	Low output voltage				0.025	V
R <sub>OH</sub>	High state output resistance	$V_{CC} = 15V$		2.5	4	Ω
R <sub>OL</sub>	Low state output resistance	$V_{CC} = 15V$		2	3	Ω
I <sub>PEAK</sub>	Peak output current	$V_{CC} = 15V$		2		А
I <sub>DC</sub>	Continuous output current				1	А
t <sub>R</sub>	Rise time	$C_{LOAD} = 1000 pF V_{CC} = 15V$		7.5	10	ns
t <sub>F</sub>	Fall time	$C_{LOAD} = 1000 pF V_{CC} = 15V$		6.5	9	ns
t <sub>ONDLY</sub>	On-time propagation delay	$C_{LOAD} = 1000 pF V_{CC} = 15V$		25	32	ns
t <sub>OFFDLY</sub>	Off-time propagation delay	$C_{LOAD} = 1000 pF V_{CC} = 15V$		20	30	ns
V <sub>CC</sub>	Power supply voltage		4.5	15	30	V
I <sub>CC</sub>	Power supply current	$V_{IN} = 3.5V$ $V_{IN} = 0V$ $V_{IN} = +V_{CC}$		1 0	3 15 15	mΑ μΑ μΑ



#### Electrical Characteristics @ temperatures over -55 °C to 125 °C (3)

Unless otherwise noted,  $4.5V \le V_{CC} \le 30V$  , Tj < 150°C

All voltage measurements with respect to GND. IXD 502 configured as described in Test Conditions. All specifications are for one channel.

Symbol	Parameter	ameter Test Conditions		Тур	Max	Units V
V <sub>IH</sub>	High input voltage $4.5V \le V_{CC} \le 15V$		3.1			
V <sub>IL</sub>	Low input voltage	$4.5V \le V_{CC} \le 15V$			0.8	V
V <sub>IN</sub>	Input voltage range		-5		$V_{CC} + 0.3$	V
I <sub>IN</sub>	Input current	$0V \le V_{IN} \le V_{CC}$	-10		10	μA
V <sub>OH</sub>	High output voltage		V <sub>CC</sub> - 0.025			V
V <sub>OL</sub>	Low output voltage				0.025	V
R <sub>OH</sub>	High state output resistance				6	Ω
R <sub>OL</sub>	Low state output resistance	$V_{CC} = 15V$			5	Ω
I <sub>DC</sub>	Continuous output current				1	А
t <sub>R</sub>	Rise time	$C_{LOAD} = 1000 pF V_{CC} = 15V$			11	ns
t <sub>F</sub>	Fall time	$C_{LOAD} = 1000 pF V_{CC} = 15V$				ns
t <sub>ONDLY</sub>	On-time propagation delay	$C_{LOAD} = 1000 pF V_{CC} = 15V$			40	ns
t <sub>OFFDLY</sub>	Off-time propagation delay	$C_{LOAD} = 1000 pF V_{CC} = 15V$			38	ns
V <sub>CC</sub>	Power supply voltage		4.5	15	30	V
I <sub>cc</sub>	Power supply current			1 0	3 40 40	mA μA μA

#### Notes:

- 1. Operating the device beyond the parameters listed as "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 2. The device is not intended to be operated outside of the Operating Ratings.
- 3. Electrical Characteristics provided are associated with the stated Test Conditions.
- 4. Typical values are presented in order to communicate how the device is expected to perform, but not necessarily to highlight any specific performance limits within which the device is guaranteed to function.

\* The following notes are meant to define the conditions for the  $\theta_{_{J-A}}, \theta_{_{J-C}}$  and  $\theta_{_{J-S}}$  values:

1) The  $\theta_{J,A}$  (typ) is defined as junction to ambient. The  $\theta_{J,A}$  of the standard single die 8-Lead PDIP and 8-Lead SOIC are dominated by the resistance of the package, and the IXD\_5XX are typical. The values for these packages are natural convection values with vertical boards and the values would be lower with forced convection. For the 6-Lead DFN package, the  $\theta_{J,A}$  value supposes the DFN package is soldered on a PCB. The  $\theta_{J,A}$  (typ) is 200 °C/W with no special provisions on the PCB, but because the center pad provides a low thermal resistance to the die, it is easy to reduce the  $\theta_{J,A}$  by adding connected copper pads or traces on the PCB. These can reduce the  $\theta_{J,A}$  (typ) to 125 °C/W easily, and potentially even lower. The  $\theta_{J,A}$  for DFN on PCB without heatsink or thermal management will vary significantly with size, construction, layout, materials, etc. This typical range tells the user what he is likely to get if he does no thermal management.

2)  $\theta_{J,C}$  (max) is defined as juction to case, where case is the large pad on the back of the DFN package. The  $\theta_{J,C}$  values are generally not published for the PDIP and SOIC packages. The  $\theta_{J,C}$  for the DFN packages are important to show the low thermal resistance from junction to the die attach pad on the back of the DFN, -- and a guardband has been added to be safe.

3) The  $\theta_{JS}$  (typ) is defined as junction to heatsink, where the DFN package is soldered to a thermal substrate that is mounted on a heatsink. The value must be typical because there are a variety of thermal substrates. This value was calculated based on easily available IMS in the U.S. or Europe, and not a premium Japanese IMS. A 4 mil dialectric with a thermal conductivity of 2.2W/mC was assumed. The result was given as typical, and indicates what a user would expect on a typical IMS substrate, and shows the potential low thermal resistance for the DFN package.



#### Pin Description

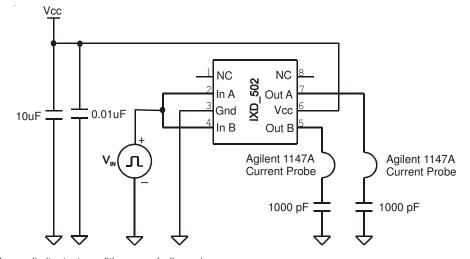
PIN	PACKAGE	SYMBOL	FUNCTION	DESCRIPTION
2 1	SOIC, DIP DFN	IN A	A Channel Input	A Channel Input signal-TTL or CMOS compatible.
3 2	SOIC, DIP DFN	GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.
4 3	SOIC, DIP DFN	IN B	B Channel Input	B Channel Input signal-TTL or CMOS compatible.
5 4	SOIC, DIP DFN	OUT B	B Channel Output	B Channel Driver output. For application purposes, this pin is connected via a resistor to a gate of a MOSFET/IGBT.
6 5	SOIC, DIP DFN	V <sub>CC</sub>	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 30V.
7 6	SOIC, DIP DFN	OUT A	A Channel Output	A Channel Driver output. For application purposes, this pin is connected via a resistor to a gate of a MOSFET/IGBT.

#### CAUTION: Follow proper ESD procedures when handling and assembling this component.

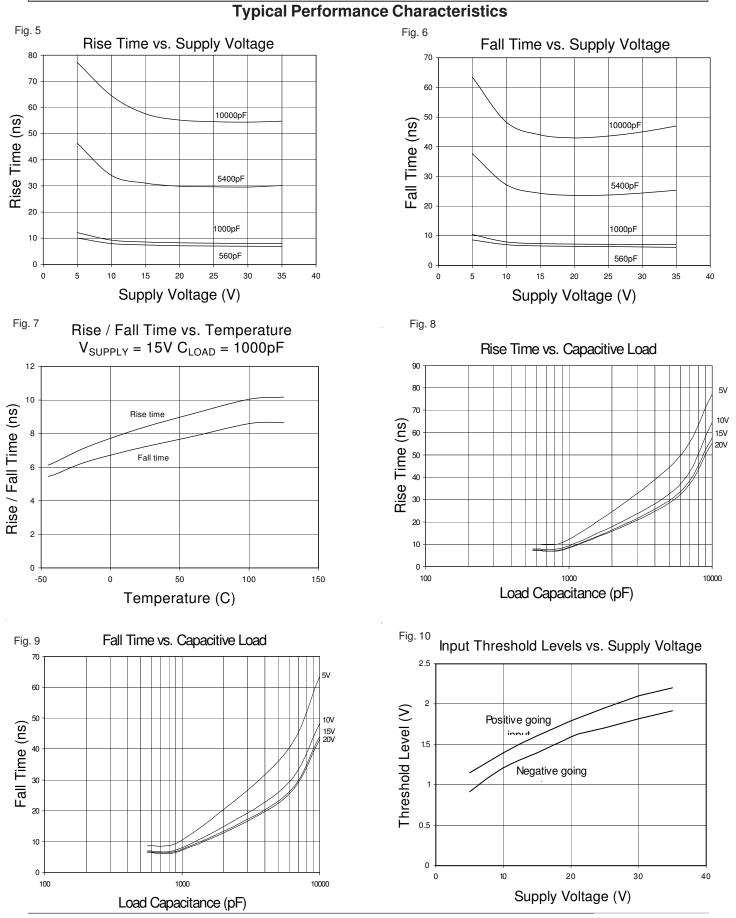
#### **Pin Configuration IXDF502 IXDI502 IXDN502** 1 NC 1 NC NC NC 8 8 1 NC NC 8 OUT A 2 IN A OUT 2 7 2 7 IN A IN A OUT A 3 GND V 6 3 GND 6 V. 3 GND V. 6 4 INB 5 OUT B 4 INB 5 4 5 OUT B INB OUT B 8 Lead PDIP (PI) 8 Pin SOIC (SIA) 8 Lead PDIP (PI) 8 Lead PDIP (PI) 8 Pin SOIC (SIA) 8 Pin SOIC (SIÁ) 6 Lead DFN (D1) 6 Lead DFN (D1) 6 Lead DFN(D1) (Bottom View) (Bottom View) (Bottom View) OUTA IN A OUTA INA GND Vcc /cc GNE /cc GN INE фитв IN B **OUTB** фитв IN

NOTE: Solder tabs on bottoms of DFN packages are grounded

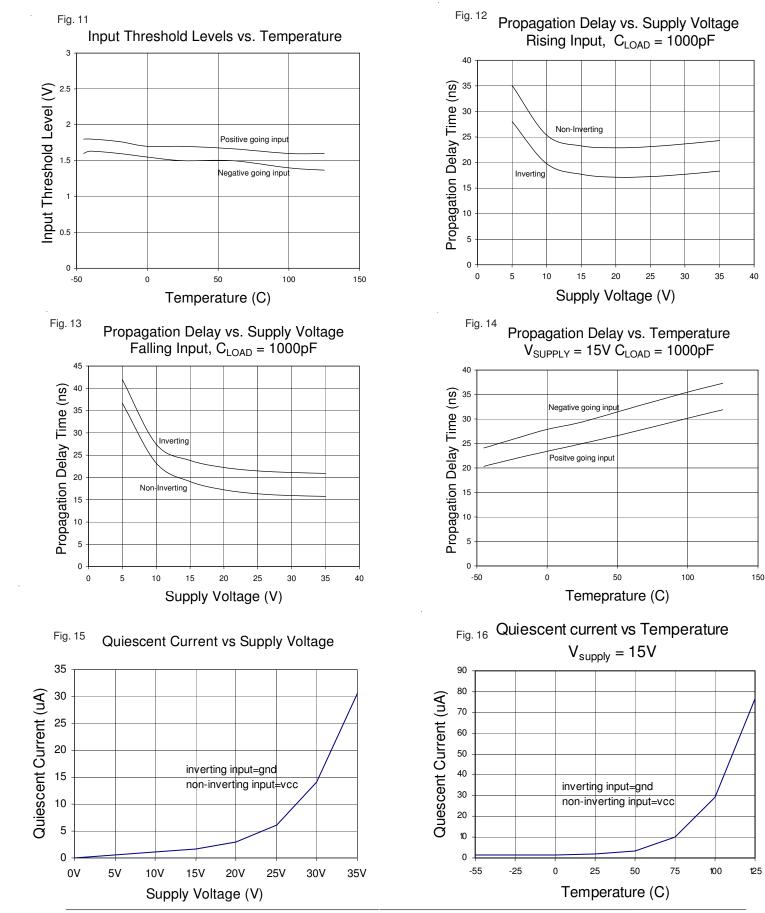
#### Figure 4 - Characteristics Test Diagram













10000pF

5400pF

1000pF

560pF

10000pF

5400p

10000

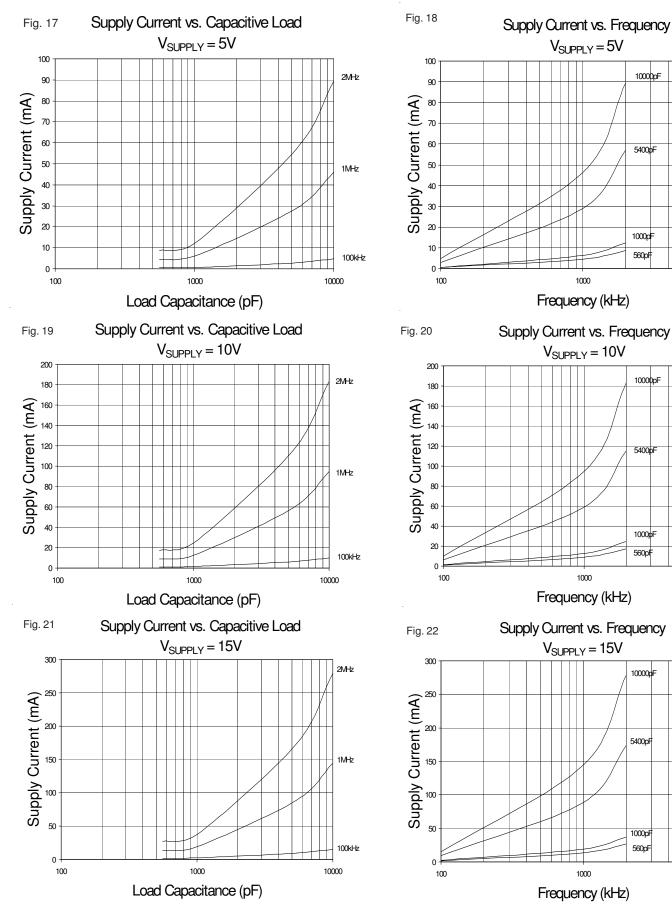
560pF

10000pF

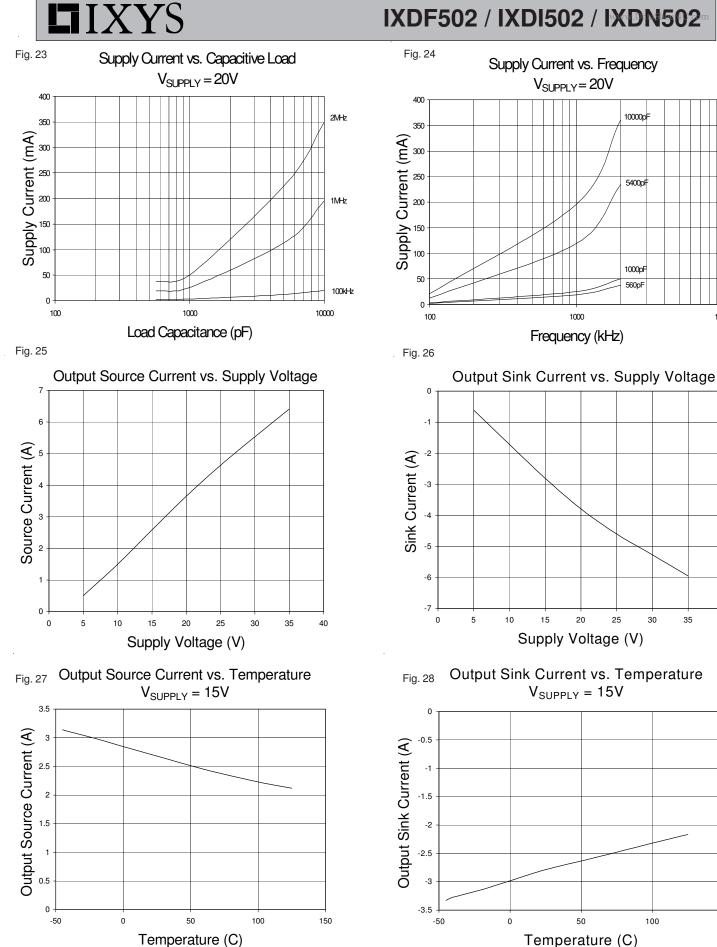
5400pF

1000pF 560pF 10000

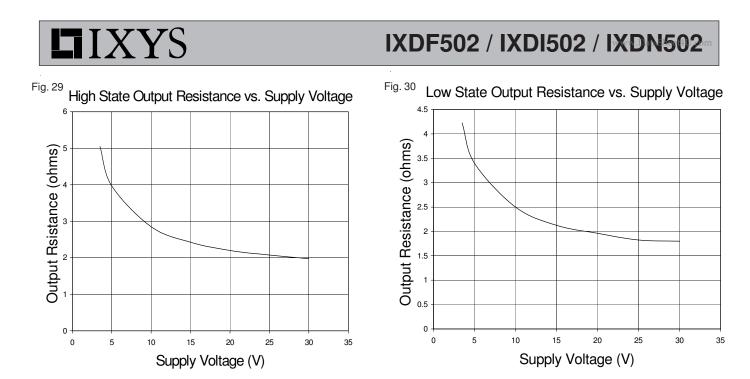
10000



10000



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#### Supply Bypassing, Grounding Practices And Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXD\_502, it is very important to observe certain design criteria in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXD\_502 to charge a 1500pF capacitive load from 0 to 25 volts in 25ns.

Using the formula:  $I = C \Delta V/\Delta t$ , where  $\Delta V=25V C=1500 pF \& \Delta t=25 ns$ , we can determine that to charge 1500 pF to 25 volts in 25 ns will take a constant current of 1.5A. (In reality, the charging current won't be constant, and will peak somewhere around 2A).

#### SUPPLY BYPASSING

In order for our design to turn the load on properly, the IXD\_502 must be able to draw this 1.5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is an order of magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected and should have low inductance, low resistance and high-pulse current-service ratings). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXD\_502 to an absolute minimum.

#### GROUNDING

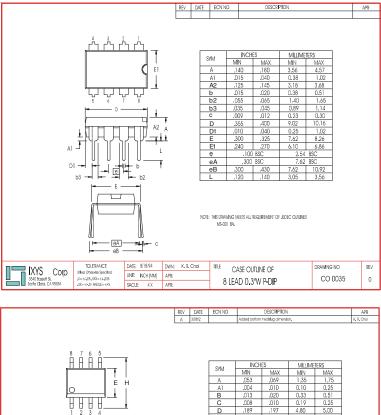
In order for the design to turn the load off properly, the IXD\_502 must be able to drain this 1.5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXD\_502 and its load. Path #2 is between the IXD\_502 and its power supply. Path #3 is between the IXD\_502 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXD\_502.

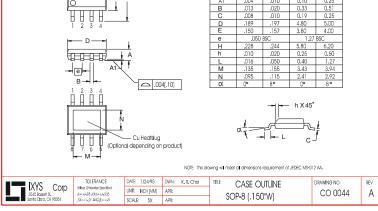
#### **OUTPUT LEAD INDUCTANCE**

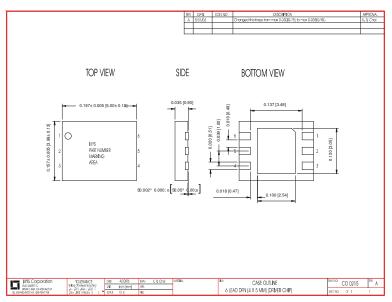
Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible. If the driver must be placed farther than 0.2" (5mm) from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connected directly to the ground terminal of the load.

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### IXDF502 / IXDI502 / IXDN502







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