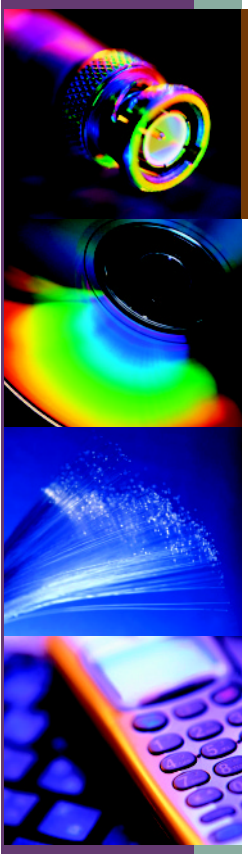

CS3110/12

Reed-Solomon Encoders

AMPHION™

Virtual Components for the Converging World

The CS3110 and CS3112 Reed-Solomon encoders are designed to provide high performance solutions for a broad range of applications requiring forward error correction. These application specific cores are developed for high data rate digital video and audio, satellite broadcast or data storage and retrieval applications and are fully compliant with the European DVB (CS3110) and IntelSat (CS3112) Standards. The cores are configurable Reed-Solomon encoders featuring user-selectable codeword length (50-255 symbols) and number of parity symbols (0-20 symbols) providing up to 1.6 Gigabits per second data throughput. The CS3110 and CS3112 are available in both ASIC and programmable logic versions that have been handcrafted by Amphion for optimal performance while minimizing power consumption and silicon area.

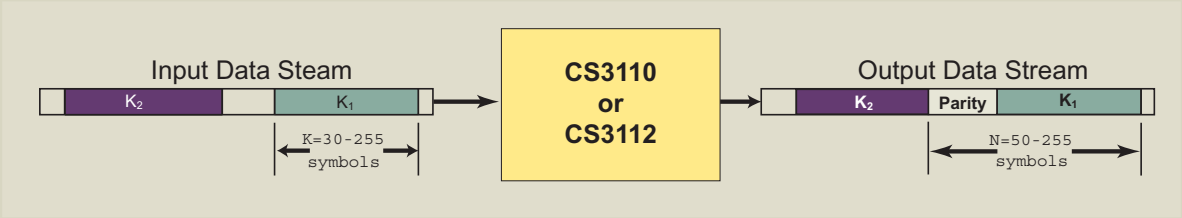

Figure 1: CS3110/12 Function

ENCODER FEATURES

- **Configurable Codeword Length (N) and Number of Parity Symbols (T)**
  - N = 50 – 255 symbols
  - T = 0 – 20 symbols
  - Single implementation supports any valid block length and parity length
- **High Performance Solution for High Data Rate Reed Solomon Encoding**
  - Can process burst and continuous data
  - Low latency – 2 clock cycles
- **Supports a Range of Standards, Including Intelsat IESS 308/309, European DVB Telecommunication Standards ETS 300-421 and ETS 300-429**
- **Byte-Wide Input and Output, Clocked by a Single Symbol Rate Clock**
- **Ease of Integration**
  - Tapeout-Ready™ firm-IP targeted netlist
  - Simple core interface for easy integration into larger systems

KEY METRICS AND SPECIFICATIONS

- **Size:** 15.5k Gates
- **Maximum Frequency:** 200 MHz[1]
- **8 Bits per Symbol Yields 1.6 Gbits per Second Throughput**
- **CS3110 (DVB compliant)**
  - Generator Polynomial: $g(x)=(x+1)(x+a)(x+a^2)\ldots(x+a^{(2t-1)})$[2]
  - Field Polynomial: $f(x)=x^8+x^4+x^3+x^2+1$
- **CS3112 (Intelsat compliant)**
  - Generator Polynomial: $g(x)=(x+a^{120})(x+a^{121})\ldots(x+a^{120+(2t-1)})$
  - Field Polynomial: $f(x)=x^8+x^7+x^2+x+1$

APPLICATIONS

- **Digital Video and Audio Broadcast**
- **Digital Satellite Broadcast**
- **Data Storage and Retrieval Systems (e.g. Hard Disk Drives, CD-ROM, DVD, etc.**

1. Performance is dependent on the silicon process and libraries selected. 200MHz operation is representative of 180nm silicon using standard cell libraries.
2. "t" represents the number of correctable symbol errors (excluding erasures) and equals one-half the number of parity symbols "T".

CS3110/CS3112 FUNCTIONAL DESCRIPTION

BLOCK CODES FOR ERROR CORRECTION

In digital communications systems, channel coding is used to introduce controlled redundancy into a data sequence on the transmission (encode) side of a communications channel. The redundant information is then exploited by the receiver (decoder) to overcome the effects of data corrupting channel distortions and noise. Block codes are a type of channel coding scheme characterized by the independent coding of successive discrete blocks or groups of information bits with no dependencies between successive blocks of data. Binary codes operate on sequences of bits, whereas non-binary codes encode data as multi-bit symbols – 8 bits per symbol for most applications. Reed-Solomon codes are a particularly powerful type of non-binary, linear block code.

The CS3110 and CS3112 are designed to provide high-performance forward error correction (FEC) compliant with digital video broadcast (DVB) standards and other applications using Reed-Solomon. The cores are capable of processing both burst and continuous data streams and input and output will be symbol wide, clocked by a single symbol rate clock. The implementation is low latency (2 symbol clock cycles) and the simple core interface allows easy integration into larger systems.

The encoder accepts an input data block and outputs the unaltered input data block followed by parity symbols at the end of the code block; i.e., the encoders produce systematic codes. As shown in Figure 1, the length of the input data stream "K" ranges between 30 and 255 symbols with the output data stream "N" a function of the input stream and the number of parity symbols "T". N ranges between 50 to 255 symbols.

CS3110/CS3112 OPERATION

The encoders consist of 3 primary blocks as shown in Figure 2. A section of storage is reserved for the generator polynomial coefficients, the total number of symbols in the codeword (codeword length), and the number of appended check symbols (parity length). The codeword length and parity length registers are written and read via standard processor interface signals, as are the generator polynomial coefficients, a series of stored constants covering the range of 0 to 20 appended parity symbols. The parity symbol calculation block is responsible for producing the parity values from the input data sequence and the generator polynomial coefficients. The count and control circuitry performs internal control operations and switches the output data stream between the input information data stream and the generated parity values.

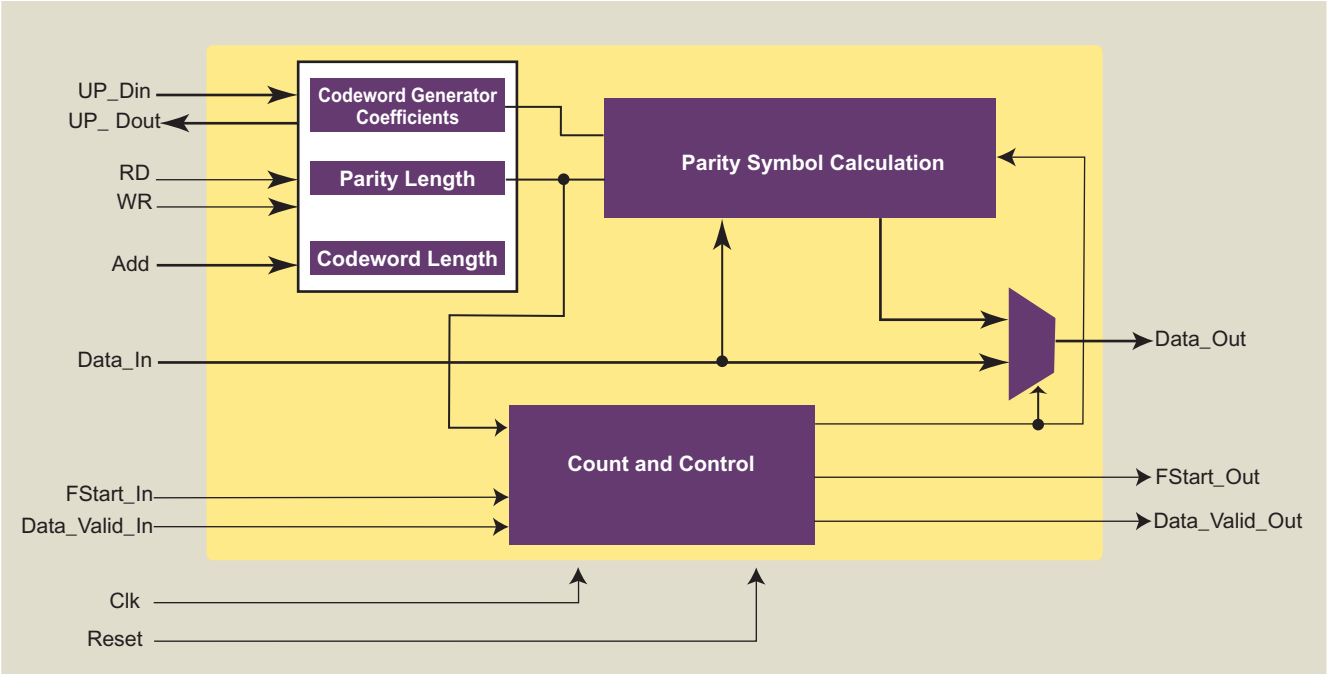

Figure 2: CS3110/CS3112 Block Diagram

PIN/PORT DESCRIPTION

Table 1 gives the descriptions of the input and output ports of the CS3110 and CS3112 Reed Solomon encoders. Unless otherwise stated, all signals are active high and bit (0) is the least significant bit.

Table 1: Input and Output Descriptions

SIGNAL	I/O	WIDTH (Bits)	Description
CLK	I	1	Symbol rate clock, rising edge active
Reset	I	1	Asynchronous Master Reset, active high
Data Stream Input Port			
Data_In [7:0]	I	8	Input data symbol, 8 bits wide
FStart_In	I	1	When high, indicates the data on Data_In is the first symbol in a new information sequence
Data_Valid_In	I	1	When high signifies that the signals at the Data_In and FStart_In ports contain valid information
Data Stream Output Port			
Data_Out [7:0]	O	8	Output data symbol, 8 bits wide
FStart_Out	O	1	When high, indicates the data on Data_Out is the first symbol in a new coded block
Data_Valid_Out	O	1	When high, signifies that the signals at the Data_Out and FStart_Out ports contain valid information
Control and Configuration			
UP_Din [7:0]	I	18	Data Bus input from microprocessor
Add [4:0]	I	5	Address Bus from microprocessor
RD	I	1	Read Enable for Data Bus
WR	I	1	Write Enable for Data Bus
UP_Dout [7:0]	O	8	Data Bus output to microprocessor

PROCESSOR INTERFACE

Before operation of the encoder can commence, the code generator polynomial coefficients, the codeword length and the parity length must be loaded into their appropriate registers via the processor interface. The addresses of the respective registers are given in Table 2.

Table 2: Register Address Contents for Microprocessor Interface

ADDRESS (HEX)	CONTENT	CONTENT WIDTH (bits)	ADDRESS (HEX)	CONTENT	CONTENT WIDTH (bits)
00	Generator Coefficient (0)	8	OC	Generator Coefficient (12)	8
01	Generator Coefficient (1)	8	OD	Generator Coefficient (13)	8
02	Generator Coefficient (2)	8	OE	Generator Coefficient (14)	8
03	Generator Coefficient (3)	8	OF	Generator Coefficient (15)	8
04	Generator Coefficient (4)	8	10	Generator Coefficient (16)	8
05	Generator Coefficient (5)	8	11	Generator Coefficient (17)	8
06	Generator Coefficient (6)	8	12	Generator Coefficient (18)	8
07	Generator Coefficient (7)	8	13	Generator Coefficient (19)	8
08	Generator Coefficient (8)	8	14-1D	Reserved	x
09	Generator Coefficient (9)	8	1E	Codeword Length (symbols)	8
0A	Generator Coefficient (10)	8	1F	Parity Length (symbols)	5
0B	Generator Coefficient (11)	8			

Addresses 00_{HEX} – 13_{HEX} contain the code generator polynomial coefficients, while address $1F_{HEX}$ contains the codeword length value (in symbols) and address $1F_{HEX}$ contains the parity length value. Every time the parity length changes, its value and the values of the appropriate generator coefficients must be loaded into their registers before error-free encoding can commence. Values are loaded into their respective registers by applying the correct address signal to *Add*, the parameter values to *UP_Din* and then asserting the write enable signal. The inputs *Add* and *UP_Din* are sampled on the write signal *WR* rising edge. The contents of the registers can be read by applying the correct address signal to Add and asserting the read enable signal *RD*. The contents are loaded to *UP_Dout* on the read signal *RD* rising edge.

RESET AND CLOCKING STRATEGY

All synchronous elements in the encoders are clocked using the rising edge of the *Clk* signal. The exceptions to this are the registers holding the generator polynomial coefficients, codeword length and parity length. These are written and read using strobe signals present in the processor interface. Additionally, all I/O signals are registered on the rising edge of Clk, with the exception of Reset. When the reset signal Reset is asserted, all registers will be set to zero value. The codeword length register will be loaded with the value FF_{HEX} (255_{10}) and the parity length register will be loaded with the value 10_{HEX} (16_{10}). The code generator polynomial registers are loaded with the corresponding coefficients for the given parity length. The default code rate is therefore (255, 239).

INPUT DATA INTERFACE

The *Data_Valid_In* signal should be asserted whenever valid data is present on *Data_In* and *FStart_In*. *Data_Valid_In* acts as a clock enable and if de-asserted, the encoder will not sample the signals at *FStart_In* and *Data_In*. Therefore, there is no requirement for the information sequence to be input in a continuous stream. If *Data_Valid_In* is de-asserted after a complete information sequence has been input, the encoder will continue to clock out the output parity values, despite the fact that the input data flow has stalled.

FStart_In should be asserted for one clock cycle at the same time as the first information symbol in a new sequence is applied to *Data_In*, allowing the appropriate parameters to be read. After *k* information symbols have been applied to the encoder, *Data_In* will not be sampled for a further N – K clock cycle, to allow the parity symbols to be output. The only exception to this scheme occurs if *FStart_In* signal is asserted at any time before a complete codeword has been output. In this case the encoder will restart the encoding process with the current value on *Data_In* as the start of a new information sequence; and, output data values for the previous coded block that have not yet emerged from the encoder will be lost. If the values held in the generator polynomial coefficients, codeword length and parity length registers are updated, the updated register values are not applied until the next assertion of *FStart_In*. Therefore, the programmable registers can be updated while the encoder is still processing the previous block. All programmable parameters must be stable one clock cycle before the beginning of the new information sequence to which the updated parameters should be applied.

OUTPUT DATA INTERFACE

FStart_Out is asserted high for one clock cycle at the same time as the first codeword symbol appears on *Data_Out*. When valid information symbols are present on *Data_Out*, the output *Data_Valid_Out* signal is asserted high.

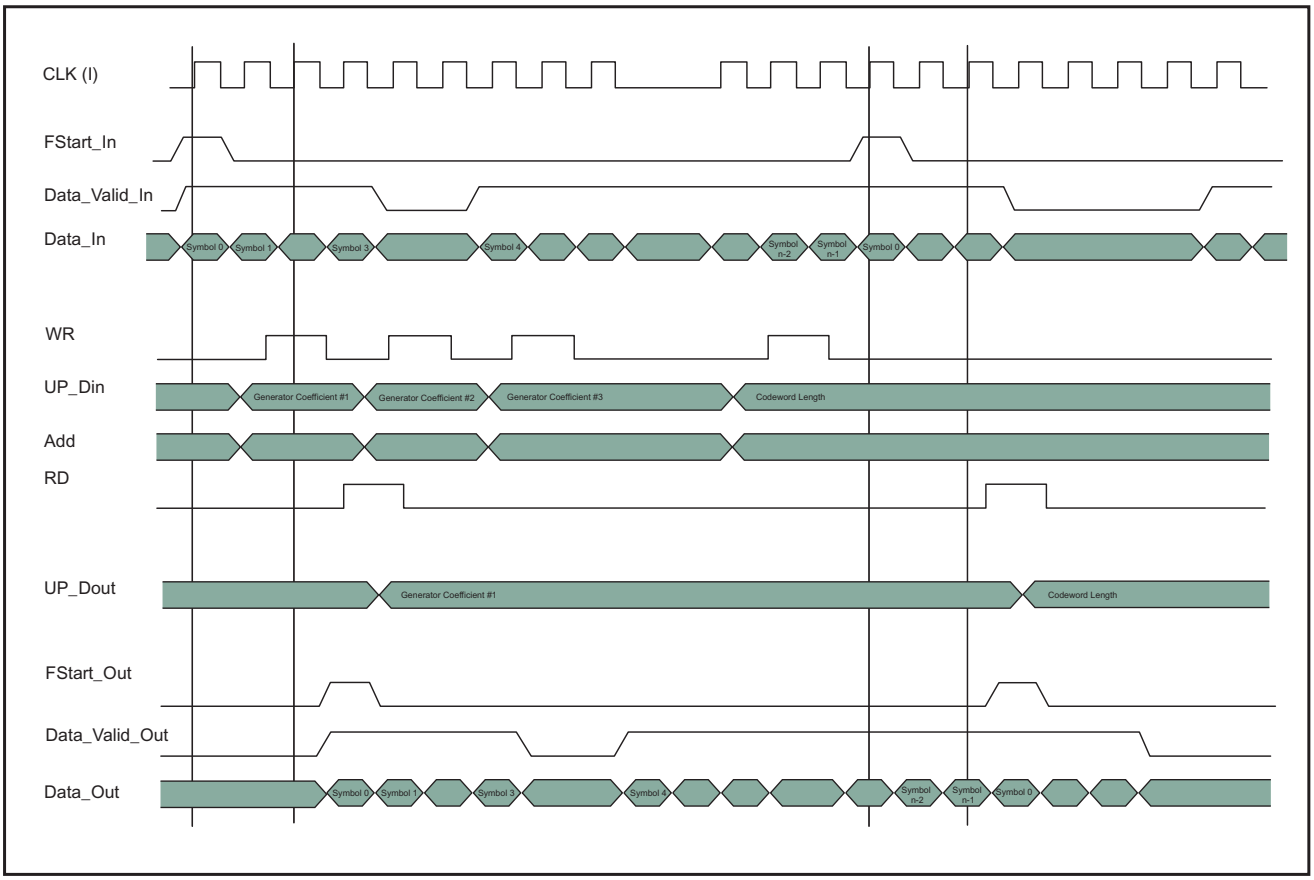

Figure 3: Functional Timing Characteristics of the CS3110 and CS3112

DEFINITION OF RS CODE IMPLEMENTED IN THE CS3110/CS3112

The CS3110 and CS3112 encoders support a wide range of applications and are fully compliant with the European DVB Standards ETS 300-421 and ETS 300-429 (CS3110) or Intelsat IESS 308/309 (CS3112). The Reed-Solomon Generator polynomial for the European DVB standards is:

$g(x)=(x+1)(x+a)(x+a^2)\ldots(x+a^{(2t-1)})$, where a is 02_{HEX} and the Reed-Solomon primitive polynomial is:

$f(x)=x^8+x^4+x^3+x^2+1$.

Equivalently, for Intelsat the Reed-Solomon Generator polynomial is:

$g(x)=(x+a^{120})(x+a^{121})\ldots(x+a^{120+(2t-1)})$

with a Reed-Solomon primitive polynomial of

$f(x)=x^8+x^7+x^2+x+1$

The core is designed for high performance applications and is configurable for any valid block length (n = 50-255) and parity length ((N – K) = 0–20). For ETS 300-421 and ETS 300-429, the coding parameters are:

(204,188,8)

where the rate is in the format (N, K, t)- n is the codeword length, k is the message length, t is the error correction capability and is (N – K)/2.

TIMING CHARACTERISTICS

Most inputs and outputs to the encoders are registered and fully synchronous. Full pin descriptions and conditional timing behavior for non-registered pins are given in the CS3110/CS3112 databook. Functional timing characteristics are given in Figure 3 with example characteristics in Table 3. Timing characteristics are technology dependent and will vary by instantiation as signal loading in the target system determines final timing.

Table 3: Encoder Timing Characteristics

SYMBOL	DESCRIPTION	CONDITION	VALUE	COMMENT
t_{cyc}	Clock Cycle Rate	min	5ns	Positive edge triggered
t_{su}	Input port set-up time	Worst case	2.99ns	
t_h	Input port hold time	Worst case	0ns	
t_{co}	Output port clock to output timing		0.7ns	
t_{skew}	Clock skew	max	200ps	Synthesis Value

CS6190TK: All values reflect pre-layout estimated timing. Wireloading conditions use “Conservative” model supplied by model supplied by library vendor and worst case commercial operating conditions.

AVAILABILITY AND IMPLEMENTATION INFORMATION

ASIC CORES

For applications that require the high performance, low cost and high integration of an ASIC, Amphion delivers a series of multimedia cores that are pre-optimized by Amphion experts to a targeted silicon technology. Choose from off-the-shelf versions of the CS3110 or CS3112 available for many popular ASIC and foundry silicon supplier technologies or Amphion can port the encoders to a technology of your choice.

Table 4: ASIC Cores

PRODUCT ID#	SILICON VENDOR	PRODUCT NAME/PROCESS	PERFORMANCE[a]	LOGIC GATES[b]	AVAILABILITY
CS3110		Programmable Reed-Solomon Encoder			
CS3110TK	TMSC	180nm using Artisan standard cell libraries	1.6 Gbps throughput at 200MHz	15k	Now
CS3112TK	TMSC	180nm using Artisan standard cell libraries	1.6 Gbps throughput at 200MHz	15.6k	Now

a. Performance figures based on silicon vendor design kit information. ASIC performance is pre-layout using vendor-provided statistical wire loading information, under the following conditions: $T_J = 125^oC$, V_{CC} -10%)
b. Logic gates do not include clock circuitry

Consult your local Amphion representative for product specific performance information, current availability of individual products, and for lead times for ASIC core porting.

PROGRAMMABLE LOGIC CORES

For ASIC prototyping or for projects requiring the fast time-to-market of a programmable logic solution, Amphion has a range of core solutions that offer the silicon-aware performance tuning found in all Amphion products, combined with the rapid design times offered by today's leading programmable logic solutions.

Table 5: Programmable Logic Cores

PRODUCT ID#	SILICON VENDOR	PROGRAMMABLE LOGIC PRODUCT	PERFORMANCE[a] (Data Rate)	PERFORMANCE[a] (Clock Speed)	DEVICE RESOURCE USED	AVAILABILITY
CS3110AA	Altera	Apex 20K FPGA	592 Mbps	79 MHz	2079 LEs	Now
CS3110XE	Xilinx	Virtex-E FPGA	720 Mbps	85 MHz	904 Slices	Now
CS3110X2	Xilinx	Virtex-2 FPGA		117 MHz	826 Slices	Now
CS3112AA	Altera	Apex 20K FPGA	456 Mbps	68 MHz	2358 LEs	Now
CS3112XE	Xilinx	Virtex-E FPGA	680 Mbps	80 MHz	923 Slices	Now

a. Performance represents core only under worst case commercial conditions. Does not include timing effect of external logic and I/O circuitry.

ABOUT AMPHION

Amphion (formerly Integrated Silicon Systems) is the leading supplier of speech coding, video/image processing and channel coding application specific silicon cores for system-on-a-chip (SoC) solutions in the broadband, wireless, and mulitmedia markets

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