

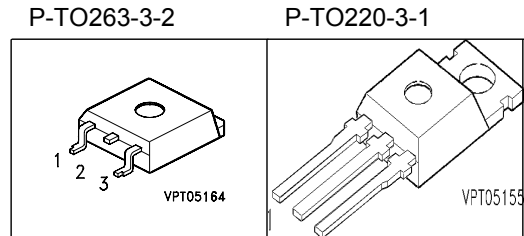
## OptiMOS™ Power-Transistor

### Feature

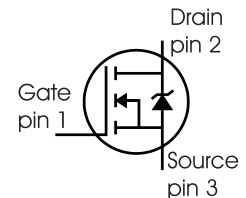
- N-Channel
- Enhancement mode
- Logic Level
- Low on-resistance  $R_{DS(on)}$
- Excellent Gate Charge x  $R_{DS(on)}$  product (FOM)
- Superior thermal resistance
- 175°C operating temperature
- Avalanche rated
- dv/dt rated

### Product Summary

$V_{DS}$	30	V
$R_{DS(on)}$	5.2	mΩ
$I_D$	80	A



Type	Package	Ordering Code	Marking
SPP80N03S2L-05	P-TO220-3-1	Q67042-S4033	2N03L05
SPB80N03S2L-05	P-TO263-3-2	Q67042-S4032	2N03L05



**Maximum Ratings**, at  $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current $T_C = 25\text{ °C}^1)$ $T_C = 100\text{ °C}$	$I_D$	80 80	A
Pulsed drain current $T_C = 25\text{ °C}$	$I_D \text{ puls}$	320	
Avalanche energy, single pulse $I_D = 80\text{ A}$ , $V_{DD} = 25\text{ V}$ , $R_{GS} = 25\text{ Ω}$	$E_{AS}$	325	mJ
Reverse diode dv/dt $I_S = 80\text{ A}$ , $V_{DS} = 24\text{ V}$ , $di/dt = 200\text{ A/μs}$ , $T_{jmax} = 175\text{ °C}$	dv/dt	6	kV/μs
Gate source voltage	$V_{GS}$	±20	V
Power dissipation $T_C = 25\text{ °C}$	$P_{tot}$	154	W
Operating and storage temperature	$T_j, T_{stg}$	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

**Thermal Characteristics**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Characteristics</b>					
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.97	K/W
SMD version, device on PCB:	$R_{thJA}$				
@ min. footprint		-	-	62	
@ 6 cm <sup>2</sup> cooling area <sup>2)</sup>		-	-	40	

**Electrical Characteristics, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Static Characteristics</b>					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	30	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=110\mu A$	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current $V_{DS}=30V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=30V, V_{GS}=0V, T_j=125^\circ C$	$I_{DSS}$	-	0.01	1	$\mu A$
		-	10	100	
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	$I_{GSS}$	-	1	100	nA
Drain-source on-state resistance $V_{GS}=4.5V, I_D=55A$ $V_{GS}=4.5V, I_D=55A, \text{SMD version}$	$R_{DS(on)}$	-	5.5	7.5	m $\Omega$
		-	5.2	7.2	
Drain-source on-state resistance <sup>3)</sup> $V_{GS}=10V, I_D=55A$ $V_{GS}=10V, I_D=55A, \text{SMD version}$	$R_{DS(on)}$	-	3.9	5.2	
		-	3.6	4.9	

<sup>1</sup>Current limited by bondwire; with a  $R_{thJC} = 0.97\text{ K/W}$  the chip is able to carry  $I_D = 135A$  and calculated with max. source pin temperature of  $85^\circ C$ .

<sup>2</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70  $\mu m$  thick) copper area for drain connection. PCB is vertical without blown air.

<sup>3</sup>Diagrams are related to straight lead versions

Electrical Characteristics, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Dynamic Characteristics</b>						
Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 80\text{A}$	55	110	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$	-	2590	3885	pF
Output capacitance	$C_{oss}$		-	1025	1540	
Reverse transfer capacitance	$C_{rss}$		-	205	308	
Gate resistance	$R_G$		-	1.75	-	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{V}$ , $V_{GS} = 10\text{V}$ , $I_D = 20\text{A}$ , $R_G = 2.7\Omega$	-	10	15	ns
Rise time	$t_r$		-	50	75	
Turn-off delay time	$t_{d(off)}$		-	44	66	
Fall time	$t_f$		-	20	30	

**Gate Charge Characteristics**

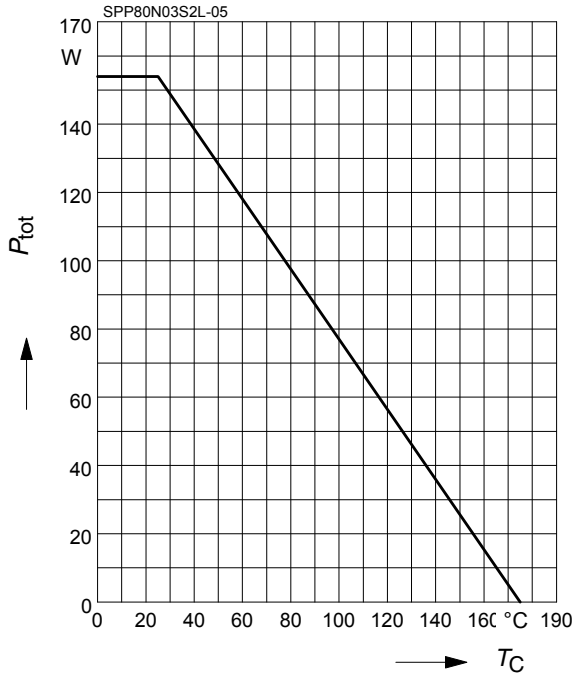
Gate to source charge	$Q_{gs}$	$V_{DD} = 24\text{V}$ , $I_D = 40\text{A}$	-	7.9	9.9	nC
Gate to drain charge	$Q_{gd}$		-	20.3	30	
Gate charge total	$Q_g$	$V_{DD} = 24\text{V}$ , $I_D = 40\text{A}$ , $V_{GS} = 0$ to $10\text{V}$	-	64.8	81	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 24\text{V}$ , $I_D = 40\text{A}$	-	3.2	-	V

**Reverse Diode**

Inverse diode continuous forward current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	80	A
Inverse diode direct current, pulsed	$I_{SM}$		-	-	320	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{V}$ , $f = 80\text{A}$	-	0.95	1.26	V
Reverse recovery time	$t_{rr}$	$V_R = 15\text{V}$ , $f = 5$ , $di_f/dt = 100\text{A}/\mu\text{s}$	-	38.6	58	ns
Reverse recovery charge	$Q_{rr}$		-	44.8	76.2	

### 1 Power dissipation

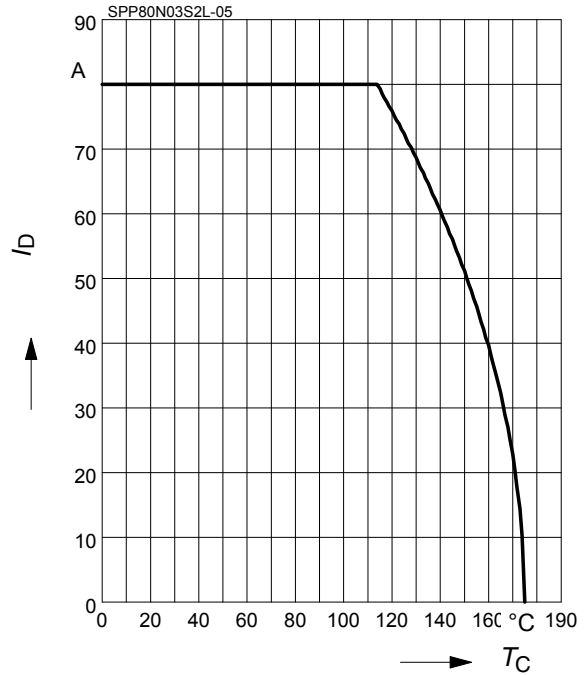
$$P_{tot} = f(T_C)$$



### 2 Drain current

$$I_D = f(T_C)$$

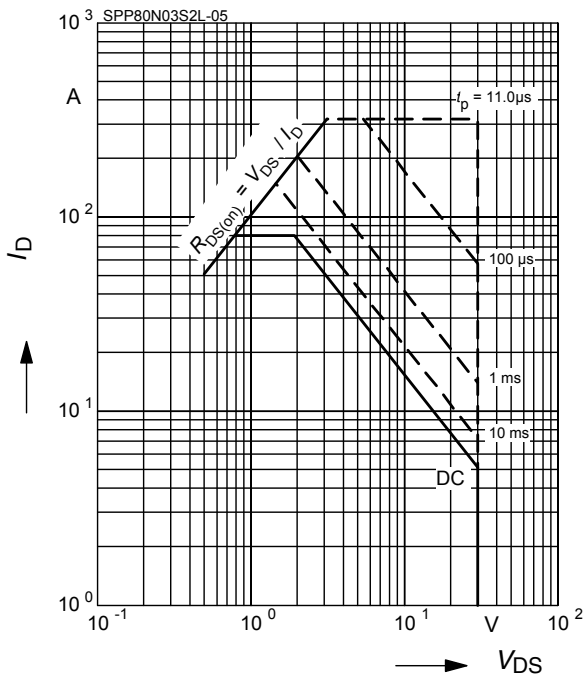
parameter:  $V_{GS} \geq 10\text{ V}$



### 3 Safe operating area

$$I_D = f(V_{DS})$$

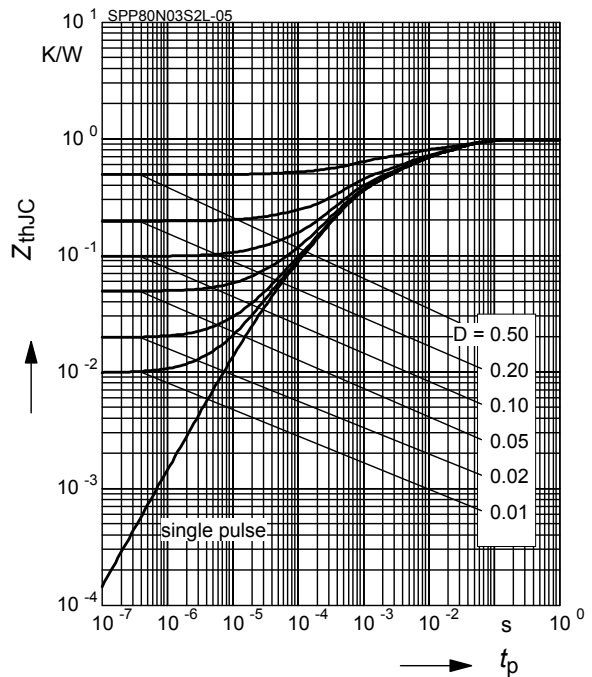
parameter:  $D = 0$ ,  $T_C = 25\text{ °C}$



### 4 Transient thermal impedance

$$Z_{thJC} = f(t_p)$$

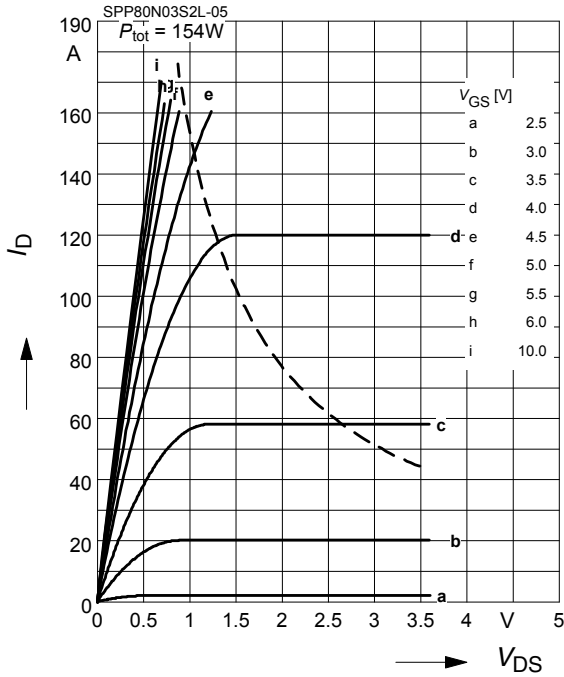
parameter:  $D = t_p/T$



**5 Typ. output characteristic**

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

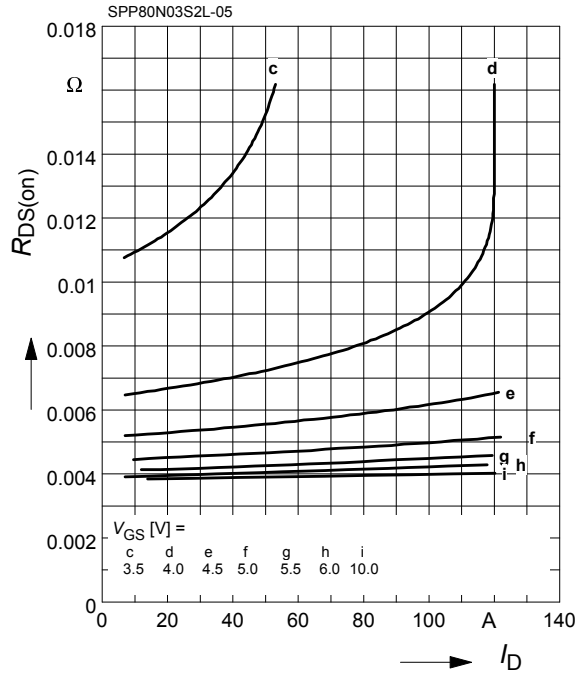
parameter:  $t_p = 80 \mu\text{s}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D)$

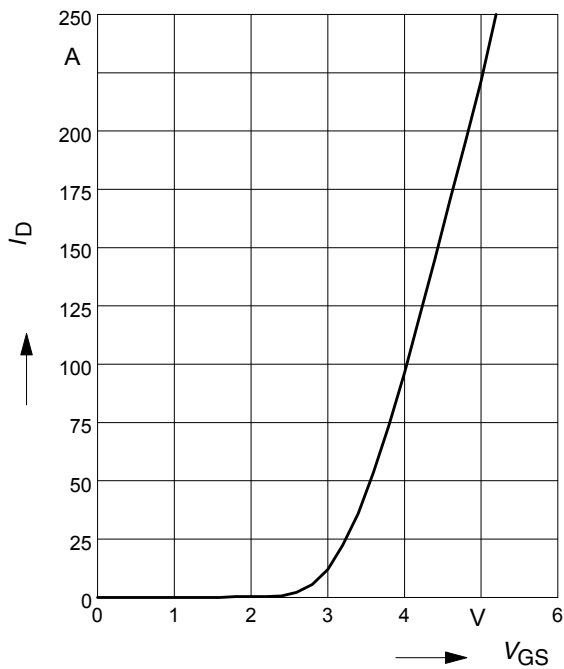
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

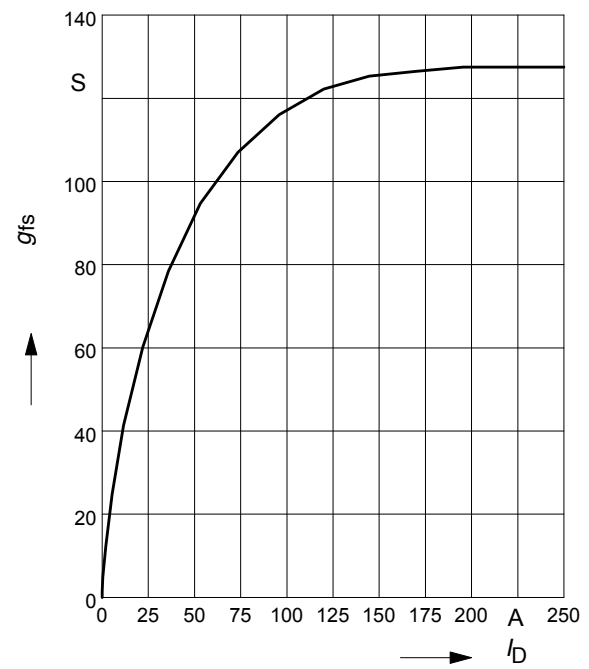
parameter:  $t_p = 80 \mu\text{s}$



**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

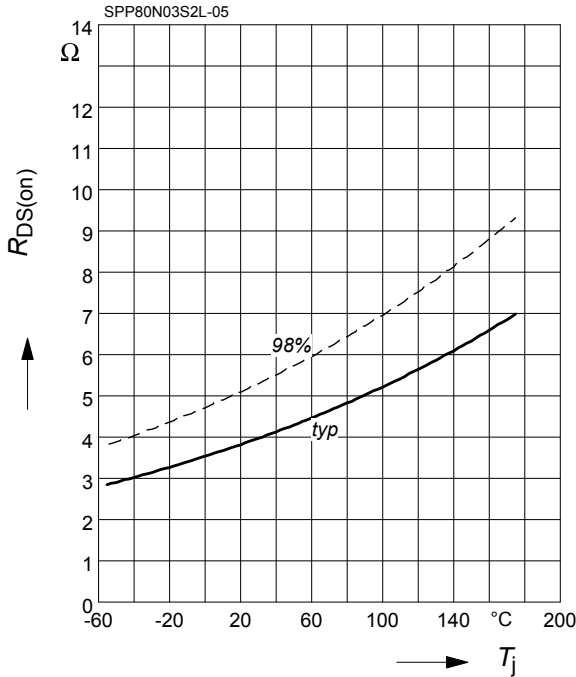
parameter:  $g_{fs}$



**9 Drain-source on-state resistance**

$$R_{DS(on)} = f(T_j)$$

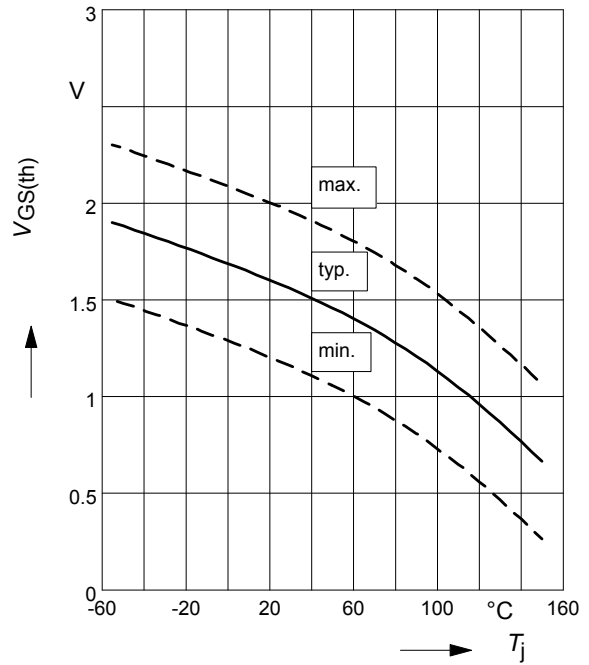
parameter:  $I_D = 55 \text{ A}$ ,  $V_{GS} = 10 \text{ V}$



**10 Gate threshold voltage**

$$V_{GS(th)} = f(T_j)$$

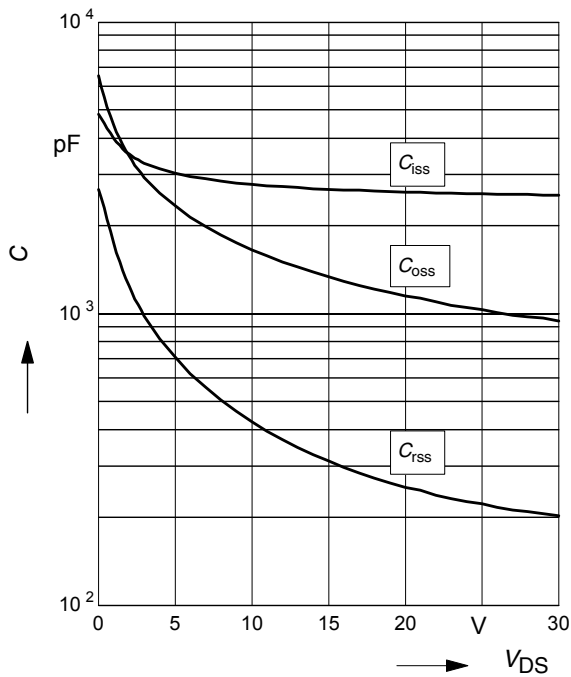
parameter:  $V_{GS} = V_{DS}$ ,  $I_D = 110 \mu\text{A}$



**11 Typ. capacitances**

$$C = f(V_{DS})$$

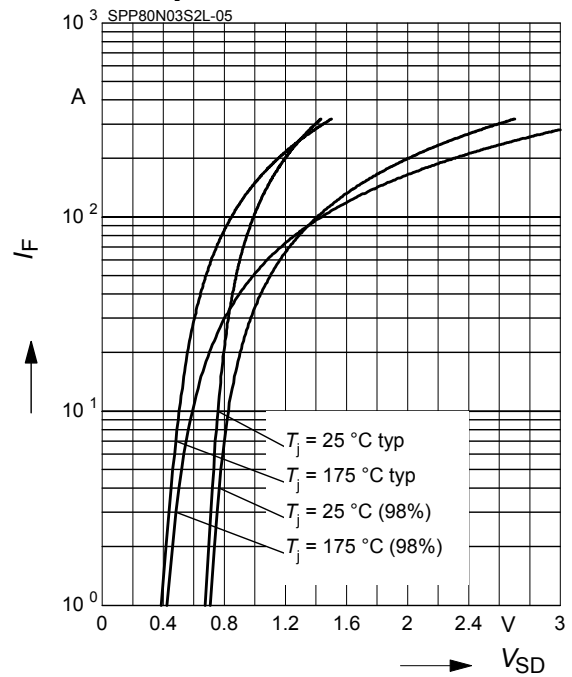
parameter:  $V_{GS}=0\text{V}$ ,  $f=1 \text{ MHz}$



**12 Forward character. of reverse diode**

$$I_F = f(V_{SD})$$

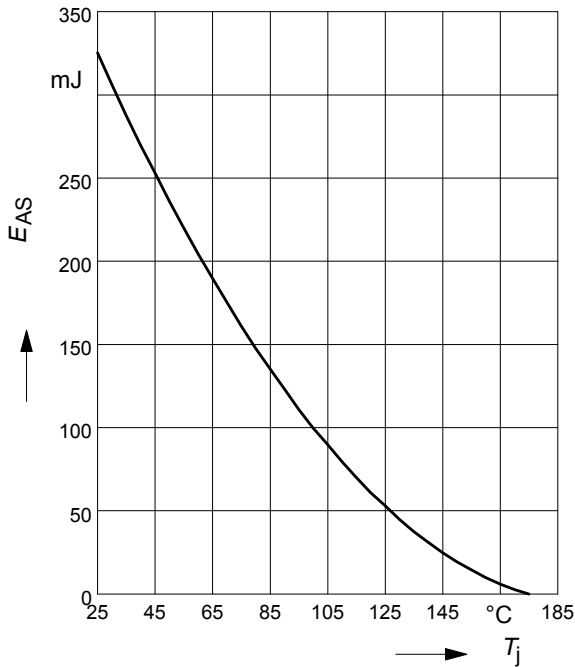
parameter:  $T_j$ ,  $t_p = 80 \mu\text{s}$



**13 Typ. avalanche energy**

$$E_{AS} = f(T_j)$$

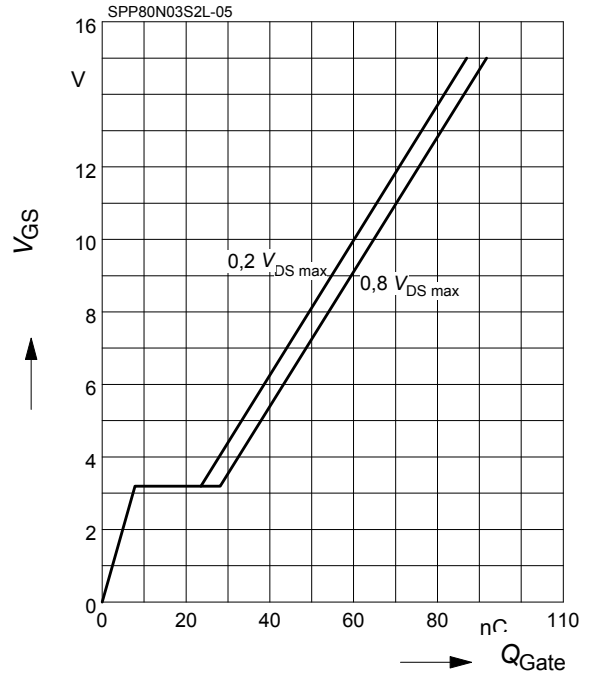
par.:  $I_D = 80 \text{ A}$  ,  $V_{DD} = 25 \text{ V}$  ,  $R_{GS} = 25 \Omega$



**14 Typ. gate charge**

$$V_{GS} = f(Q_{Gate})$$

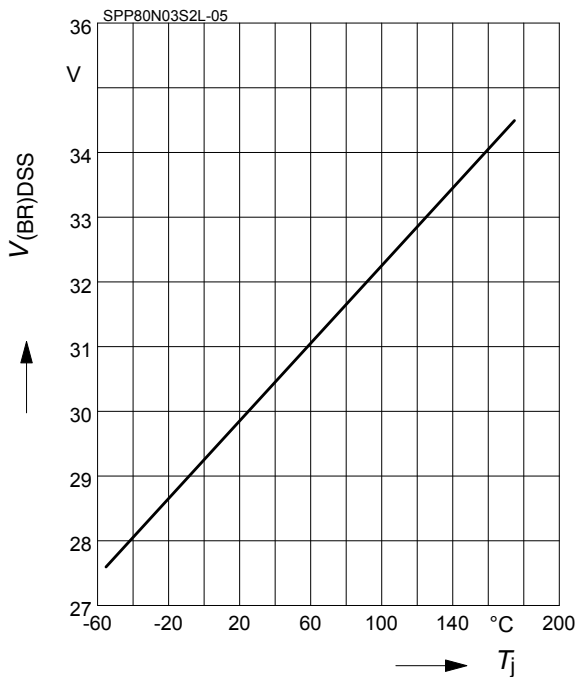
parameter:  $I_D = 40 \text{ A}$  pulsed



**15 Drain-source breakdown voltage**

$$V_{(BR)DSS} = f(T_j)$$

parameter:  $I_D = 10 \text{ mA}$



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