RIMM® Module SPD Specification based on 256Mb RDRAM®(E-die, 32s banks)

Version 1.0
March 2003

Change History

Version 0.1 (Dec. '03) -Preliminary
First Copy
Based on the SAMSUNG 256Mb D-die RIMM Module SPD

Version 1.0 (Mar. '04)
Eliminate "Preliminary"

MR16R1624(8)EG0-CT9/CM8/CK8

- Feature: Single Sided Module & 1,250mil height(CM8/CK8)
  Single Sided Module & 1,375mil height(CT9)
- Composition : 16Mx16 *4(8) pcs
- Used component type & part number :
  K4R571669E-GCT9/GCM8/GCK8
- # of banks in component : 32s banks (Doubled with Split Banks)
- Refresh : 16K/32ms

MR16R162GEG0-CT9/CM8/CK8

- Feature: Double Sided Module & 1,250mil height(CM8/CK8)
  Double Sided Module & 1,375mil height(CT9)
- Composition : 16Mx16 *16 pcs
- Used component type & part number :
  K4R571669E-GCT9/GCM8/GCK8
- # of banks in component : 32s banks (Doubled with Split Banks)
- Refresh : 16K/32ms

• Contents ;

Byte # (Dec)	Described Function	Option	Field Width	Units	Supported Function			Hex Value			Note
					T9	M8	K8	T9	M8	K8	
0	SPD Revision Level		8	LUT	SPD Revision 1.3			02h			1
1	Total Number of Bytes in the SPD		8	LUT	256 Bytes			08h			1
2	Device Type		8	LUT	RDRAM®			01h			1
3	Module Type		8	LUT	RIMM® Module			01h			1
4	Row Address Bits[3:0], Column Address Bits[3:0]		4,4	bits	9 bits, 7 bits			97h			
5	Bank Address Bits and Type		8	LUT	32s banks			C5h			1
6	Refresh Bank Bits		3	bits	32 Refresh Bank Sets			05h			
7	Refresh Period(=t_{REF})		8	ms	32ms			20h			
8	Protocol Version		8	LUT	Protocol Version 3			04h			1
9	Misc. Device Configuration Field		8	n/a	DQS=1.5, no -LP, S28, S3			05h			3
10	Minimum Precharge to RAS time(=$t_{RP-R,Min}$)		5	1/f_{RAS}	8cycles	8cycles	8cycles	08h			
11	Minimum RAS to Precharge time(=$t_{RAS-R,Min}$)		6	1/f_{RAS}	20cycles	20cycles	20cycles	14h			
12	Minimum RAS to CAS time(=$t_{RCD-R,Min}$)		5	1/f_{RAS}	10cycles	8cycles	10cycles	0Ah	08h	0Ah	
13	Minimum RAS to RAS time(=$t_{RR-R,Min}$)		5	1/f_{RAS}	8cycles	8cycles	8cycles	08h			
14	Minimum Precharge to Precharge time(=$t_{PP-R,Min}$)		5	1/f_{RAS}	8cycles	8cycles	8cycles	08h			
15	Min t_{CYCLE} for Range A		8	128ps	1.875ns	2.50ns	2.50ns	0Eh	13h	13h	
16	Max t_{CYCLE} for Range A		8	128ps	2.3ns	3.83ns	3.83ns	12h	1Eh	1Eh	
17	t_{CDLY} Range for Range A		8	t_{CYCLE}	$5t_{CYCLE}$ ~ $9t_{CYCLE}$			59h			
18	t_{CLS} and t_{CAS} Range for Range A		8	t_{CYCLE}	$2t_{CYCLE}$ for t_{CLS} & t_{CAS}			AAh			
19	Min t_{CYCLE} for Range B		8	128ps	2.18ns	RFU		11h	00h		
20	Max t_{CYCLE} for Range B		8	128ps	2.56ns	RFU		14h	00h		
21	t_{CDLY} Range for Range B		8	t_{CYCLE}	$5t_{CYCLE}$ ~ $9t_{CYCLE}$	RFU		59h	00h		
22	t_{CLS} and t_{CAS} Range for Range B		8	t_{CYCLE}	$2t_{CYCLE}$ for t_{CLS} & t_{CAS}	RFU		AAh	00h		
23	Min t_{CYCLE} for Range C		8	128ps	RFU			00h			
24	Max t_{CYCLE} for Range C		8	128ps	RFU			00h			
25	t_{CDLY} Range for Range C		8	t_{CYCLE}	RFU			00h			
26	t_{CLS} and t_{CAS} Range for Range C		8	t_{CYCLE}	RFU			00h			
27	Min t_{CYCLE} for Range D		8	128ps	RFU			00h			2
28	Max t_{CYCLE} for Range D		8	128ps	RFU			00h			2
29	t_{CDLY} Range for Range D		8	t_{CYCLE}	RFU			00h			2
30	t_{CLS} and t_{CAS} Range for Range D		8	t_{CYCLE}	RFU			00h			2
31	Power Down Exit Max.time, Phase A(=$t_{PDNXA,Max}$)		8	us	4us			04h			
32	Power Down Exit Max.time, Phase B(=$t_{PDNXB,Max}$)		8	64t_{CYCLE}	$9000t_{CYCLE}$			8Dh			
33	Nap Exit Max.time, Phase A(=$t_{NAPXA,Max}$)		8	ns	50ns			32h			
34	Nap Exit Max.time, Phase B(=$t_{NAPXB,Max}$)		8	ns	40ns			28h			

Byte # (Dec)	Described Function	Option	Field Width	Units	Supported Function			Hex Value			Note
					T9	M8	K8	T9	M8	K8	
35	f_{IMIN}[11:8] f_{IMAX}[11:8]		4 4	MHz	400MHz 533MHz	261MHz 400MHz	261MHz 400MHz	12h	11h	11h	
36	f_{IMIN}[7:0]		8	MHz	400MHz	261MHz	261MHz	90h	05h	05h	
37	f_{IMAX}[7:0]		8	MHz	533MHz	400MHz	400MHz	15h	90h	90h	
38	ODF mapping		-	-	-			00h			
39	Max. time between Current Control(=$t_{CCTRL,Max}$)		8	ms	100ms			64h			
40	Max. time between Temp. Calibration(=$t_{TEMP,Max}$)		8	ms	100ms			64h			
41	Min. time between Temp. Calibration Enable and Command(=$t_{TCEN,Min}$)		8	t_{CYCLE}	$150t_{CYCLE}$			96h			
42	Maximum RAS to Precharge time(=$t_{RAS-R,Max}$)		8	us	64us			40h			
43	Maximum time that a Device can stay in Nap Mode(=$t_{NLIMIT,Max}$)		8	us	10us			0Ah			
44	ACTREFPT[3:0], PCHREFPT[3:0]		4,4	t_{CYCLE}	$6t_{CYCLE}$, $6t_{CYCLE}$			66h			
45	CPCHREFPT_DC[3:0], RDREFPT_DC[3:0]		4,4	t_{CYCLE}	$5t_{CYCLE}$, $5t_{CYCLE}$			55h			
46	RETREFPT_DC[3:0], WRREFPT_DC[3:0]		4,4	t_{CYCLE}	$5t_{CYCLE}$, $13t_{CYCLE}$			5Dh			
47~49	Reserved		-	-	-			00h			
50	f_{RAS}[11:8]		4	MHz	533MHz	400MHz	400MHz	02h	01h	01h	
51	f_{RAS}[7:0]		8	MHz				15h	90h	90h	
52	PMAX,HI, PMAX,LO, Tj		1,1	°C	0,0,100°C			24h			
53	HeatSpreader, thermal sensor, Tplate		1,1	°C	1,0,92°C			9Ch			
54	PSTBY,HI		8	1mA	105mA	95mA	95mA	69h	5Fh	5Fh	
55	PACTI,HI		8	2mA	160mA	135mA	135mA	50h	43h	43h	
56	PACTRW,HI		8	8mA	700mA	560mA	560mA	57h	46h	46h	
57	PSTBY,LO		8	1mA	95mA	85mA	85mA	5Fh	55h	55h	
58	PACTI,LO		8	2mA	135mA	115mA	115mA	43h	39h	39h	
59	PACTRW,LO		8	8mA	560mA	440mA	440mA	46h	37h	37h	
60	PNAP		8	128uA	4.0mA			20h			
61	PRESA (Reserved for a future thermal parameter)		-	-	-			00h			
62	PRESB (Reserved for a future thermal parameter)		-	-	-			00h			
63	Checksum for bytes 0 ~ 62		8	n/a	n/a			68h	6Dh	6Fh	3
64	Module Manufacturer ID Code		8	n/a	Samsung			CEh			3, 5
65~71	..... Module Manufacturer ID Code		56	n/a	Samsung			00h			3, 5
72	Module Manufacturer Location		8	n/a	Onyang Korea			01h			3, 5
73	Module Part Number(Memory module)		8	n/a	M			4Dh			3, 5
74	Module Part Number(Module Configuration)		8	n/a	R			52h			3, 5
75	Module Part Number(Data Bits)		8	n/a	1			31h			3, 5
76	..... Module Part Number(Data Bits)		8	n/a	6			36h			3, 5
77	Module Part Number(Feature)		8	n/a	R			52h			3, 5
78	Module Part Number(Module Density)		8	n/a	Blank			20h			3, 5
79	Module Part Number(Module Density)		8	n/a	1			31h			3, 5
80	..... Module Part Number(Module Density)		8	n/a	6			36h			3, 5
81	Module Part Number (Refresh, # of banks in comp. & interface)		8	n/a	2			32h			3, 5
82	Module Part Number (# of component)	4d	8	n/a	4			34h			3, 5
		8d	8	n/a	8			38h			3, 5
		16d	8	n/a	G			47h			3, 5
83	Module Part Number(Component Revision)		8	n/a	E			45h			3, 5
84	Module Part Number(Package Type)		8	n/a	G			47h			3, 5
85	Module Part Number(PCB Revision)		8	n/a	0			30h			3, 5
86	Module Part Number(Hyphen)		8	n/a	- (Hyphen)			2Dh			3, 5

Byte # (Dec)	Described Function	Option	Field Width	Units	Supported Function			Hex Value			Note
					T9	M8	K8	T9	M8	K8	
87	Module Part Number(Power)		8	n/a	C	C	C	43h	43h	43h	3, 5
88	Module Part Number(t_{RAC} & Speed)		8	n/a	T	M	K	54h	4Dh	4Bh	3, 5
89	Module Part Number(t_{RAC} & Speed)		8	n/a	9	8	8	39h	38h	38h	3, 5
90	Module Part Number(RFU)		8	n/a	-			00h			3, 5
91	Module Manufacturer Revision Code (PCB)		8	n/a	0			30h			3, 5
92	..... Component Manufacturer Revision Code		8	n/a	E(E-die)			45h			3, 5
93	Module Manufacturing Year		8	n/a	-			-			3, 4
94	Module Manufacturing Week		8	n/a	-			-			3, 4
95~98	Module Serial Number		32	n/a	-			-			3, 5
99	Number of Devices on Module	4d	6	devices	4			04h			
		8d	6	devices	8			08h			
		16d	6	devices	16			10h			
100	Module Data Width		8	bits	16bits			10h			
101	Devices Enables	4d	8	bits	All 4devices are enabled			0Fh			
		8d	8	bits	All 8devices are enabled			FFh			
		16d	8	bits	All 16devices are enabled			FFh			
102	..... Devices Enables	4d	8	bits	All 4devices are enabled			00h			
		8d	8	bits	All 8devices are enabled			00h			
		16d	8	bits	All 16devices are enabled			FFh			
103~104	..... Devices Enables		16	bits	-			00h			
105	Module Vdd[3:0], Module Voltage Interface Level[3:0]		4,4	LUT	2.5V, 1.8V Vterm			10h			1
106	Module Vdd Tolerance		8	LUT	5% DC, 2% AC			52h			1
107~113	Reserved		56	-	-			00h			
114	CDLY0/1 for tCDLY=3		8	t_{CYCLE}	-			00h			
115	CDLY0/1 for tCDLY=4		8	t_{CYCLE}	-			00h			
116	CDLY0/1 for tCDLY=5		8	t_{CYCLE}	3 / 0			30h			
117	CDLY0/1 for tCDLY=6		8	t_{CYCLE}	4 / 0	3 / 1	3 / 1	40h	31h	31h	
118	CDLY0/1 for tCDLY=7		8	t_{CYCLE}	4 / 1	3 / 2	3 / 2	41h	32h	32h	
119	CDLY0/1 for tCDLY=8		8	t_{CYCLE}	4 / 2			42h			
120	CDLY0/1 for tCDLY=9		8	t_{CYCLE}	5 / 2			52h			
121	CDLY0/1 for tCDLY=10		8	t_{CYCLE}	-			00h			
122	CDLY0/1 for tCDLY=11		8	t_{CYCLE}	-			00h			
123	CDLY0/1 for tCDLY=12		8	t_{CYCLE}	-			00h			
124	CDLY0/1 for tCDLY=13		8	t_{CYCLE}	-			00h			
125	CDLY0/1 for tCDLY=14		8	t_{CYCLE}	-			00h			
126	CDLY0/1 for tCDLY=15		8	t_{CYCLE}	-			00h			
127	Checksum for Bytes 99 ~ 126	4d	8	n/a	-			CAh	ACh	ACh	3
		8d	8	n/a	-			BEh	A0h	A0h	3
		16d	8	n/a	-			C5h	A7h	A7h	3
128 +	Open for Customer Use		-	-	-			Undefined			

<Notes>

1. Please refer to Look-Up Table (LUT) in the Direct Rambus™ SPD specification 1.3
2. It is reserved to future use (RFU).
3. Unit is not available (n/a).
4. These bytes are programmed by code of Date Week & Date Year with binary format.
5. These bytes are programmed by Samsung' s own Module Assembly Serial # system. All modules may have unique serial #.