This version: Apr. 8. 1999

OKI Semiconductor

MSC23CV26457D-xxBS8

2,097,152-word x 64-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSC23CV26457D-xxBS8 is a 2,097,152-word x 64-bit CMOS dynamic random access memory module which is composed of eight 16Mb(2Mx8) DRAMs in TSOP packages mounted with eight decoupling capacitors. This is an 144-pin small outline dual in-line memory module. This module supports any application where high density and large capacity of storage memory are required.

FEATURES

· 2,097,152-word x 64-bit organization
· 144-pin Small Outline Dual In-line Memory Module
· Gold tab
· Single 3.3V power supply, ±0.3V tolerance
· Input : LVTTL compatible
· Output : LVTTL compatible, 3-state
· Refresh : 2048cycles/32ms
· /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
· Fast page mode with EDO, read modify write capability
· Multi-bit test mode capability

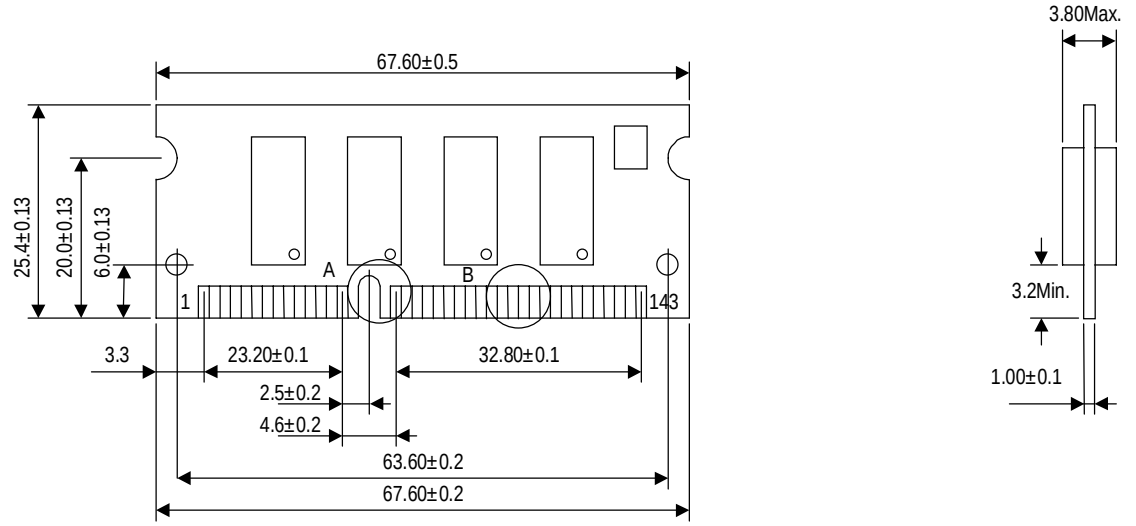
PRODUCT FAMILY

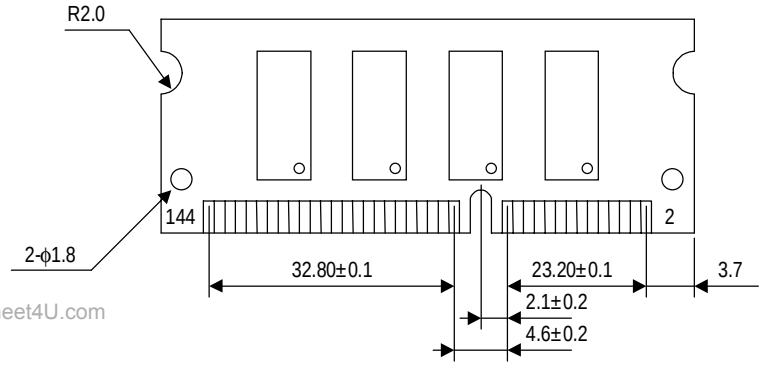
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation (Max.)	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating	Standby
MSC23CV26457D-50BS8	50ns	25ns	13ns	13ns	84ns	2880mW	14.4mW
MSC23CV26457D-60BS8	60ns	30ns	15ns	15ns	104ns	2592mW	
MSC23CV26457D-70BS8	70ns	35ns	20ns	20ns	124ns	2304mW	

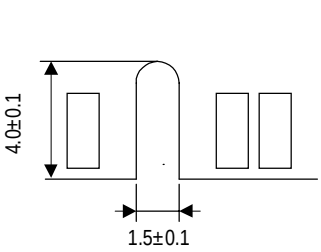
MODULE OUTLINE

MSC23CV26457D-xxBS8

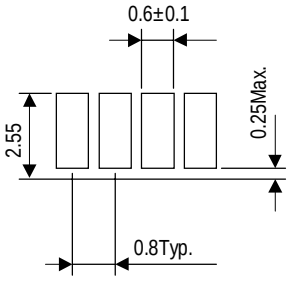
(Unit : mm)







Detail A



Detail B

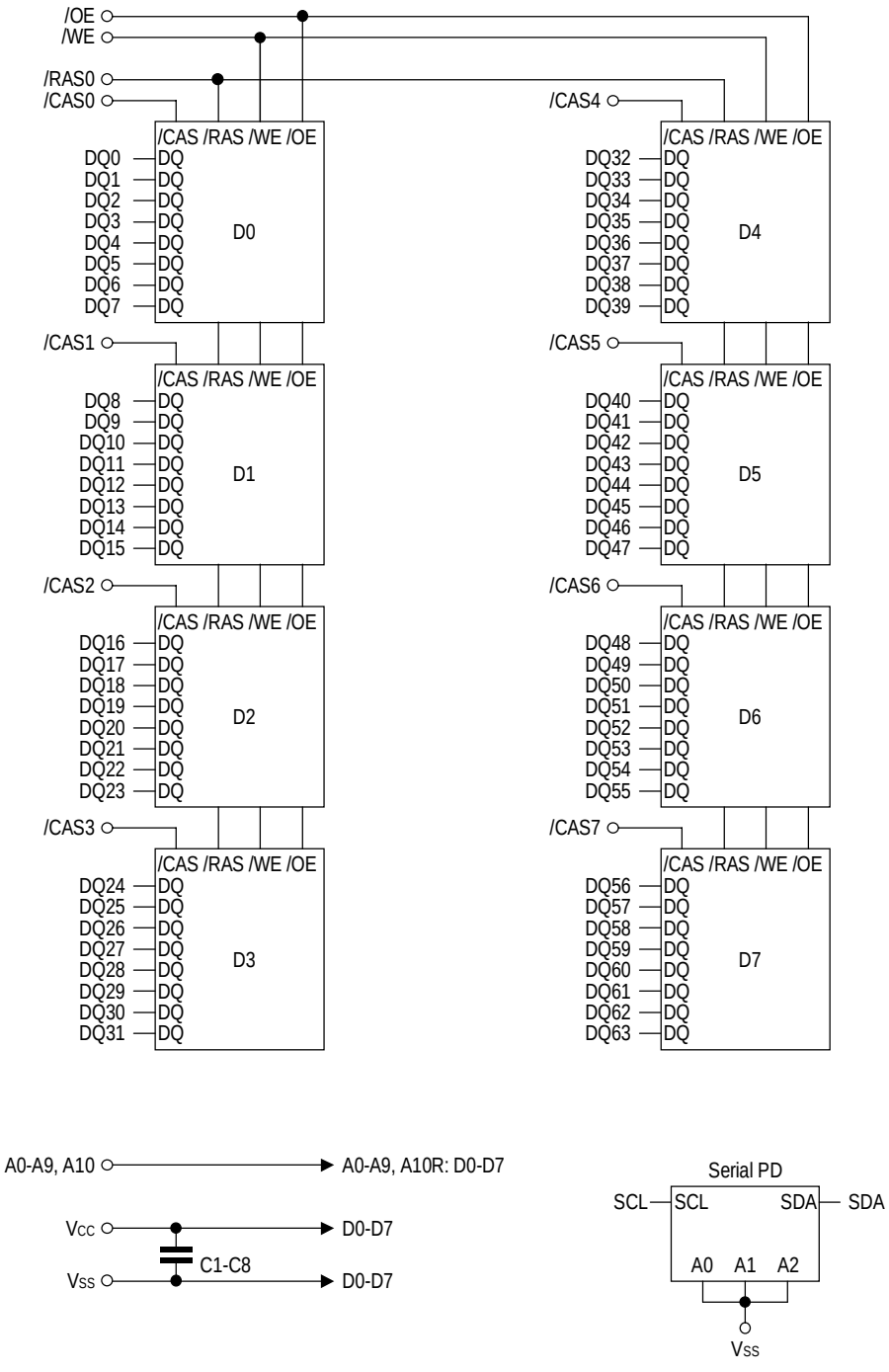
PIN CONFIGURATION

Front Side		Back Side		Front Side		Back Side	
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	2	V_{SS}	73	/OE	74	NC
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V_{CC}	82	V_{CC}
11	V_{CC}	12	V_{CC}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	/CAS0	24	/CAS4	95	DQ21	96	DQ53
25	/CAS1	26	/CAS5	97	DQ22	98	DQ54
27	V_{CC}	28	V_{CC}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{CC}	102	V_{CC}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	NC
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	NC
39	DQ9	40	DQ41	111	A10	112	NC
41	DQ10	42	DQ42	113	V_{CC}	114	V_{CC}
43	DQ11	44	DQ43	115	/CAS2	116	/CAS6
45	V_{CC}	46	V_{CC}	117	/CAS3	118	/CAS7
47	DQ12	48	DQ44	119	V_{SS}	120	V_{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V_{SS}	56	V_{SS}	127	DQ27	128	DQ59
57	NC	58	NC	129	V_{CC}	130	V_{CC}
59	NC	60	NC	131	DQ28	132	DQ60
61	NC	62	NC	133	DQ29	134	DQ61
63	V_{CC}	64	V_{CC}	135	DQ30	136	DQ62
65	NC	66	NC	137	DQ31	138	DQ63
67	/WE	68	NC	139	V_{SS}	140	V_{SS}
69	/RAS0	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	V_{CC}	144	V_{CC}

Serial PD Matrix

Byte No.		Function described	SPD Value (Hex)	Note
0		Number of Byte used	80	128 Bytes
1		Total SPD Memory size	08	256 Bytes
2		Memory type	02	EDO
3		Number of Rows	0B	11
4		Number of Columns	0A	10
5		Number of Banks	01	1
6		Module Data Width	40	64
7		Module Data Width Continued	00	0
8		Supply Voltage	01	LVTTL
9	-50	/RAS Access Time	32	50ns
	-60		3C	60ns
	-70		46	70ns
10	-50	/CAS Access Time	0D	13ns
	-60		0F	15ns
	-70		14	20ns
11		DIMM Configuration type	00	Non-parity
12		Refresh Rate/Type	00	Normal Refresh
13		Primary DRAM Width	08	x8
14		Error Checking DRAM Width	00	
15-61		Superset Information	00	Reserved
62		SPD Data Revision Code	01	1
63	-50	Checksum for Byte 0-62	29	
	-60		35	
	-70		44	
64-127		Reserved	00	
128-255		Unused Storage Location (Reserved)	FF	

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D *	8	W
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature	T_{STG}	-40 to 125	°C

* Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

Capacitance

(V_{CC} = 3.3V ±0.3V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 – A10)	C_{IN1}	-	49	pF
Input Capacitance (/RAS0)	C_{IN2}	-	65	pF
Input Capacitance (/CAS0 - /CAS7)	C_{IN3}	-	13	pF
Input Capacitance (/WE)	C_{IN4}	-	65	pF
Input Capacitance (/OE)	C_{IN5}	-	65	pF
I/O Capacitance (DQ0 - DQ63)	$C_{I/O}$	-	13	pF

DC Characteristics

(V_{CC} = 3.3V ±0.3V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	-50		-60		-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = -2.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ V_{CC}+0.3V; All other pins not under test = 0V	-80	80	-80	80	-80	80	µA	
Output Leakage Current	I_{LO}	DQ disable 0V ≤ V_{OUT} ≤ V_{CC}	-10	10	-10	10	-10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	/RAS, /CAS cycling, t_{RC} = Min.	-	800	-	720	-	640	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	/RAS, /CAS = V_{IH}	-	16	-	16	-	16	mA	1
		/RAS, /CAS ≥ V_{CC} -0.2V	-	4	-	4	-	4	mA	
Average Power Supply Current (/RAS only refresh)	I_{CC3}	/RAS cycling, /CAS = V_{IH}, t_{RC} = Min.	-	800	-	720	-	640	mA	1, 2
Average Power Supply Current (/CAS before /RAS refresh)	I_{CC6}	/RAS cycling, /CAS before /RAS	-	800	-	720	-	640	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	/RAS = V_{IL}, /CAS cycling, t_{HPC} = Min.	-	800	-	720	-	640	mA	1, 3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.

2. The address can be changed once or less while /RAS = V_{IL}.
3. The address can be changed once or less while /CAS = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 3.3V ±0.3V, Ta = 0°C to 70°C) Note: 1, 2, 3, 12, 13

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	84	-	104	-	124	-	ns	
Read Modify Write Cycle Time	t_{RWC}	110	-	135	-	160	-	ns	
Fast Page Mode Cycle Time	t_{HPC}	20	-	25	-	30	-	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{HPRWC}	58	-	68	-	78	-	ns	
Access Time from /RAS	t_{RAC}	-	50	-	60	-	70	ns	4, 5, 6
Access Time from /CAS	t_{CAC}	-	13	-	15	-	20	ns	4, 5
Access Time from Column Address	t_{AA}	-	25	-	30	-	35	ns	4, 6
Access Time from /CAS Precharge	t_{CPA}	-	30	-	35	-	40	ns	4
Access Time from /OE	t_{OEA}	-	13	-	15	-	20	ns	4
Output Low Impedance Time from /CAS	t_{CLZ}	0	-	0	-	0	-	ns	4
Data Output Hold After /CAS Low	t_{DOH}	5	-	5	-	5	-	ns	
/CAS to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	13	0	15	0	20	ns	7, 8
/RAS to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	13	0	15	0	20	ns	7, 8
/OE to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	13	0	15	0	20	ns	7
/WE to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t_T	1	50	1	50	1	50	ns	3
Refresh Period	t_{REF}	-	32	-	32	-	32	ms	
/RAS Precharge Time	t_{RP}	30	-	40	-	50	-	ns	
/RAS Pulse Width	t_{RAS}	50	10K	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode with EDO)	t_{RASP}	50	100K	60	100K	70	100K	ns	
/RAS Hold Time	t_{RSH}	7	-	10	-	13	-	ns	
/RAS Hold Time referenced to /OE	t_{ROH}	7	-	10	-	13	-	ns	
/CAS Precharge Time (Fast Page Mode with EDO)	t_{CP}	7	-	10	-	10	-	ns	
/CAS Pulse Width	t_{CAS}	7	10K	10	10K	13	10K	ns	
/CAS Hold Time	t_{CSH}	35	-	40	-	45	-	ns	
/CAS to /RAS Precharge Time	t_{CRP}	5	-	5	-	5	-	ns	
/RAS Hold Time from /CAS Precharge	t_{RHCP}	30	-	35	-	40	-	ns	
/OE Hold Time from /CAS (DQ Disable)	t_{CHO}	5	-	5	-	5	-	ns	
/RAS to /CAS Delay Time	t_{RCD}	11	37	14	45	14	50	ns	5
/RAS to Column Address Delay Time	t_{RAD}	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	7	-	10	-	10	-	ns	
Column Address Set-up Time	t_{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	7	-	10	-	13	-	ns	
Column Address to /RAS Lead Time	t_{RAL}	25	-	30	-	35	-	ns	

AC Characteristics (2/2)

(V_{CC} = 3.3V ±0.3V, Ta = 0°C to 70°C) Note: 1, 2, 3, 12, 13

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time	t_{RCH}	0	-	0	-	0	-	ns	9
Read Command Hold Time referenced to /RAS	t_{RRH}	0	-	0	-	0	-	ns	9
Write Command Set-up Time	t_{WCS}	0	-	0	-	0	-	ns	10
Write Command Hold Time	t_{WCH}	7	-	10	-	13	-	ns	
Write Command Pulse Width	t_{WP}	7	-	10	-	10	-	ns	
/WE Pulse Width (DQ Disable)	t_{WPE}	7	-	10	-	10	-	ns	
/OE Command Hold Time	t_{OEH}	7	-	10	-	13	-	ns	
/OE Precharge Time	t_{OEP}	7	-	10	-	10	-	ns	
/OE Command Hold Time	t_{OCH}	7	-	10	-	10	-	ns	
Write Command to /RAS Lead Time	t_{RWL}	7	-	10	-	13	-	ns	
Write Command to /CAS Lead Time	t_{CWL}	7	-	10	-	13	-	ns	
Data-in Set-up Time	t_{DS}	0	-	0	-	0	-	ns	11
Data-in Hold Time	t_{DH}	7	-	10	-	13	-	ns	11
/OE to Data-in Delay Time	t_{OED}	13	-	15	-	20	-	ns	
/CAS to /WE Delay Time	t_{CWD}	30	-	34	-	44	-	ns	10
Column Address to /WE Delay Time	t_{AWD}	42	-	49	-	59	-	ns	10
/RAS to /WE Delay Time	t_{RWD}	67	-	79	-	94	-	ns	10
/CAS Precharge /WE Delay Time	t_{CPWD}	47	-	54	-	64	-	ns	10
/CAS Active Delay Time from /RAS Precharge	t_{RPC}	5	-	5	-	5	-	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	t_{CSR}	5	-	5	-	5	-	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	t_{CHR}	10	-	10	-	10	-	ns	
/WE to /RAS Precharge Time (/CAS before /RAS)	t_{WRP}	10	-	10	-	10	-	ns	
/WE Hold Time from /RAS (/CAS before /RAS)	t_{WRH}	10	-	10	-	10	-	ns	
/RAS to /WE Set-up Time (Test Mode)	t_{WTS}	10	-	10	-	10	-	ns	
/RAS to /WE Hold Time (Test Mode)	t_{WTH}	10	-	10	-	10	-	ns	

Notes: 1. A start-up delay of 200µs is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 2ns.

3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF.
The output timing reference levels are V_{OH} = 2.0V and V_{OL} = 0.8V.

5. Operation within the t_{RCD}(Max.) limit ensures that t_{RAC}(Max.) can be met.
t_{RCD}(Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(Max.) limit, then the access time is controlled by t_{CAC}.

6. Operation within the t_{RAD}(Max.) limit ensures that t_{RAC}(Max.) can be met.
t_{RAD}(Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(Max.) limit, then the access time is controlled by t_{AA}.

7. t_{CEZ}(Max.), t_{REZ}(Max.), t_{WEZ}(Max.) and t_{OEZ}(Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{CEZ} or t_{REZ} must be satisfied for open circuit condition.

9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(Min.), $t_{RWD} \geq t_{RWD}$(Min.), $t_{AWD} \geq t_{AWD}$(Min.) and $t_{CPWD} \geq t_{CPWD}$(Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

11. These parameters are referenced to the /CAS leading edge in an early write cycle, and to the /WE leading edge in an /OE control write cycle, or a read modify write cycle.

12. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA9 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low levels. The test mode is cleared and the memory device returned to its normal operating state by performing a /RAS only refresh cycle or a /CAS before /RAS refresh cycle.

13. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.