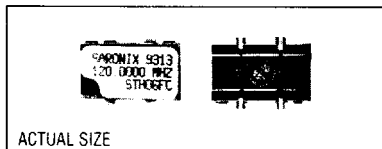
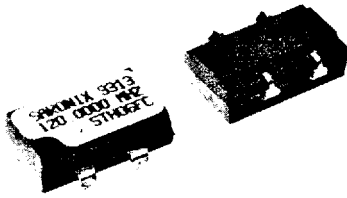
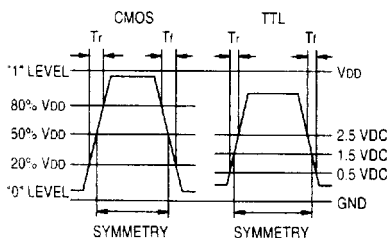


Technical Data**STA / STH / STT Series, Type F****Description**

A crystal controlled, low current oscillator to drive HCMOS and NMOS microprocessors. This ACMOS device is capable of driving both HCMOS and TTL loads at high frequencies. The tri-state function enables the output to go high impedance. The surface mountable J-leaded plastic package is ideal for automated assembly.

Applications & Features

- Ideally suited for high speed graphics, CISC and RISC processors, and custom ASIC's
- Compact Surface Mountable package
- Matches EIA standard SO-J-20 footprint
- High frequency up to 135 MHz
- HCMOS, HCMOS and TTL compatible
- Tri-state output
- Output is short-circuit protected

Output Waveform

Frequency Range: 70 MHz to 135 MHz

Frequency Stability: $\pm 50, \pm 100$ or ± 500 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.

Temperature Range:

Operating: 0°C to $+70^{\circ}\text{C}$
Storage: -55°C to $+125^{\circ}\text{C}$

Supply Voltage:

Operating: $+5\text{ VDC} \pm 10\%$
Absolute Maximum: $+7\text{ VDC}$

Supply Current:

70 MHz to 80 MHz: 30mA typical, 35mA max @ 25°C
40mA max over operating temperature range
Above 80 MHz: 45mA typical, 55mA max @ 25°C
65mA max over temperature range

Output Drive:

ACMOS

Symmetry: @ 0.5 VDD , see Part Numbering Guide on Page 2
Rise & Fall Times: 20% to 80% VDD, see Part Numbering Guide
Logic 0: 10% VDD max
Logic 1: 90% VDD min
Output Load: 50 pF in parallel with 500Ω , max

TTL

Symmetry: @ 1.5V level, see Part Numbering Guide on Page 2
Rise & Fall Times: 0.5 to 2.5V, see Part Numbering Guide
Logic 0: 0.5V max
Logic 1: 2.5V min
Sink & Source Current: 50mA max

Mechanical:

Shock: MIL-STD-883, Method 2002, Condition B
Solderability: MIL-STD-883, Method 2003
Terminal Strength: MIL-STD-202, Method 211, Conditions A and C
Vibration: MIL-STD-883, Method 2007, Condition A
Solvent Resistance: MIL-STD-202, Method 215
Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition B

Environmental:

Thermal Shock: MIL-STD-883, Method 1011, Condition A
Moisture Resistance: MIL-STD-883, Method 1004

Technical Data

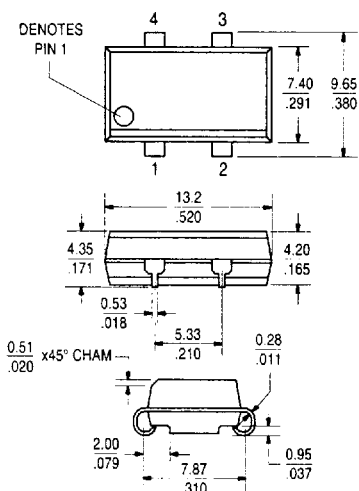
STA / STH / STT Series, Type F

Tri-State Logic Table

Pin 1 Input	Pin 3 Output
Logic "1" or NC	Oscillation
Logic "0" or GND	High Impedance

Required Input Levels on Pin 1:
 Logic "1" = 3.0V min
 Logic "0" = 0.5V max

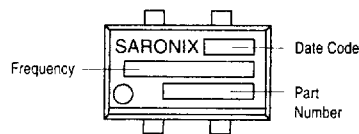
Package



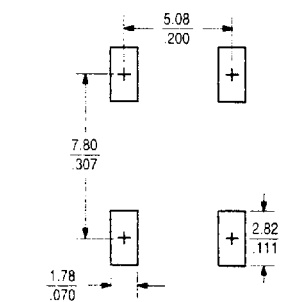
Pin Function:

Pin 1: Tri-State Control Pin 3: Output
 Pin 2: GND Pin 4: +5 VDC

Standard Marking Format



Recommended Land Pattern

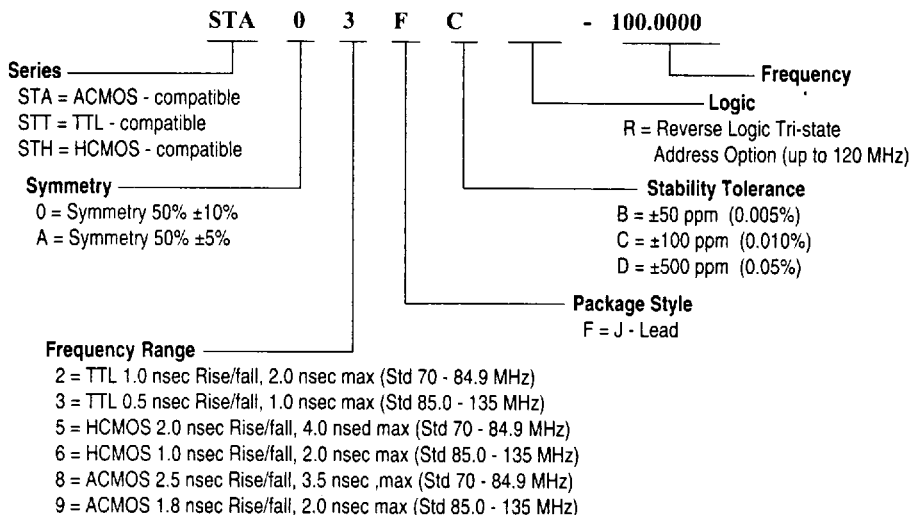


Tolerance: ± 13
 $\pm .005$

* Good external high frequency power supply decoupling required.

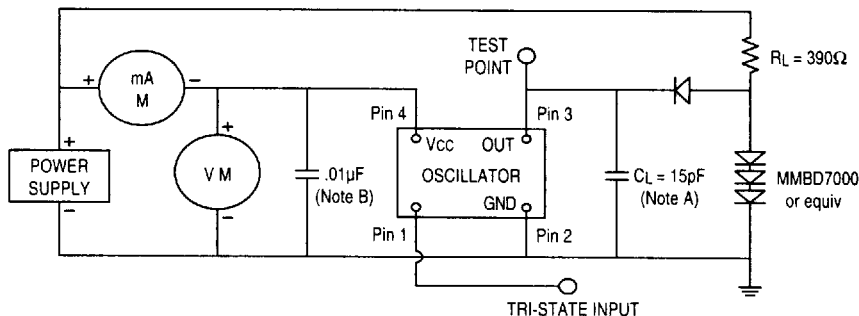
Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide



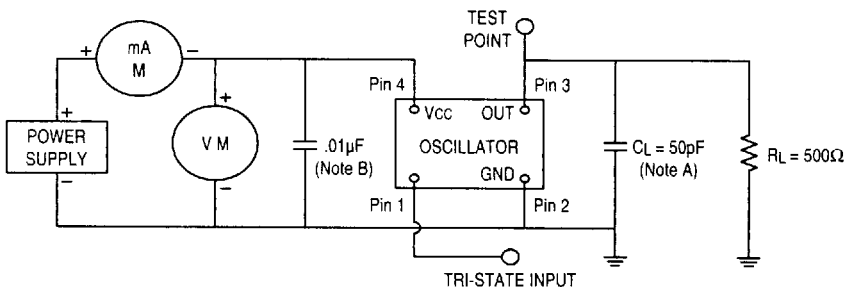
Example P/N: STA08FC - 80.0000

Test Circuits



NOTE: A. C_L includes probe and fixture capacitance.
 NOTE: B. An external $.01\mu\text{F}$ bypass capacitor close to package ground and Vcc pin is recommended.

FIGURE 1 - TTL TEST CIRCUIT



NOTE: A. C_L includes probe and fixture capacitance.
 NOTE: B. An external $.01\mu\text{F}$ bypass capacitor close to package ground and Vcc pin is recommended.

FIGURE 2 - HCMOS TEST CIRCUIT

All specifications are subject to change without notice.