Octal 16-/14-/12-Bit Rail-to-Rail DACs in 16-Lead SSOP

FEATURES

- **Smallest Pin-Compatible Octal DACs:**
  LTC2605: 16 Bits
  LTC2615: 14 Bits
  LTC2625: 12 Bits
- **Guaranteed Monotonic Over Temperature**
- 400kHz I^2C Interface
- Wide 2.7V to 5.5V Supply Range
- Low Power Operation: 250µA per DAC at 3V
- Individual Channel Power-Down to 1µA, Max
- Ultralow Crosstalk Between DACs (<10µV)
- High Rail-to-Rail Output Drive (±15mA, Min)
- Double-Buffered Digital Inputs
- 27 Selectable Addresses
- LTC2605/LTC2615/LTC2625: Power-On Reset to Zero Scale
- LTC2605-1/LTC2615-1/LTC2625-1: Power-On Reset to Midscale
- Tiny 16-Lead Narrow SSOP Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

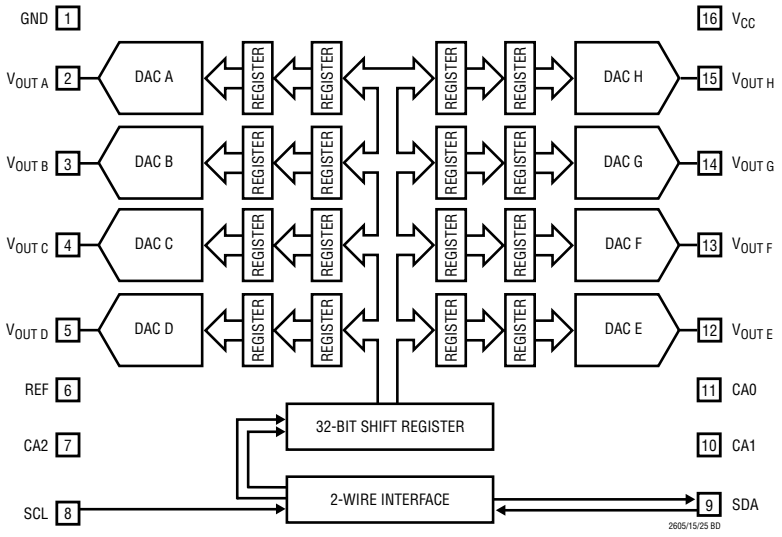
The LTC®2605/LTC2615/LTC2625 are octal 16-, 14- and 12-bit, 2.7V to 5.5V rail-to-rail voltage-output DACs in 16-lead narrow SSOP packages. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish new board-density benchmarks for 16- and 14-bit DACs and advance performance standards for output drive, crosstalk and load regulation in single-supply, voltage-output multiples.

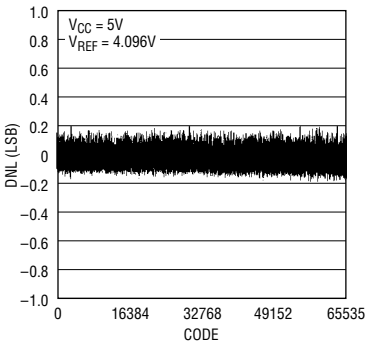
The parts use the 2-wire I^2C compatible serial interface. The LTC2605/LTC2615/LTC2625 operate in both the standard mode (maximum clock rate of 100kHz) and the fast mode (maximum clock rate of 400kHz).

The LTC2605/LTC2615/LTC2625 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale; and after power-up, they stay at zero scale until a valid write and update take place. The power-on reset circuit resets the LTC2605-1/LTC2615-1/LTC2625-1 to midscale. The voltage output stays at midscale until a valid write and update takes place.

BLOCK DIAGRAM



Differential Nonlinearity (LTC2605)

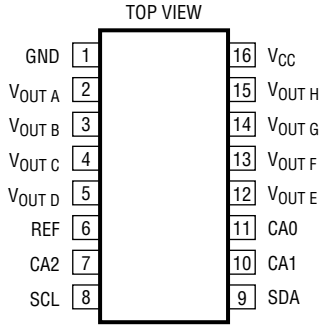


ABSOLUTE MAXIMUM RATINGS (Note 1)

Any Pin to GND ..... –0.3V to 6V
Any Pin to V_{CC} ..... –6V to 0.3V
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Temperature Range
LTC2605C/LTC2615C/LTC2625C ..... 0°C to 70°C
LTC2605C-1/LTC2615C-1/LTC2625C-1 ... 0°C to 70°C
LTC2605I/LTC2615I/LTC2625I ..... –40°C to 85°C
LTC2605I-1/LTC2615I-1/LTC2625I-1 .. –40°C to 85°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER	GN PART MARKING
LTC2605CGN	2605
LTC2605CGN-1	26051
LTC2605IGN	2605I
LTC2605IGN-1	2605I1
LTC2615CGN	2615
LTC2615CGN-1	26151
LTC2615IGN	2615I
LTC2615IGN-1	2615I1
LTC2625CGN	2625
LTC2625CGN-1	26251
LTC2625IGN	2625I
LTC2625IGN-1	2625I1

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2625/-1 MIN	LTC2625/-1 TYP	LTC2625/-1 MAX	LTC2615/-1 MIN	LTC2615/-1 TYP	LTC2615/-1 MAX	LTC2605/-1 MIN	LTC2605/-1 TYP	LTC2605/-1 MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	(Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	(Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	(Note 2)	●		±1	±4		±4	±16		±18	±64	LSB
	Load Regulation	V_{REF} = V_{CC} = 5V, Midscale											
		I_{OUT} = 0mA to 15mA Sourcing	●		0.02	0.125		0.07	0.5		0.3	2	LSB/mA
		I_{OUT} = 0mA to 15mA Sinking	●		0.03	0.125		0.10	0.5		0.4	2	LSB/mA
		V_{REF} = V_{CC} = 2.7V, Midscale											
		I_{OUT} = 0mA to 7.5mA Sourcing	●		0.04	0.25		0.15	1		0.6	4	LSB/mA
		I_{OUT} = 0mA to 7.5mA Sinking	●		0.07	0.25		0.20	1		0.8	4	LSB/mA
ZSE	Zero-Scale Error	Code = 0	●		1.7	9		1.7	9		1.7	9	mV
V_{OS}	Offset Error	(Note 4)	●		±1	±9		±1	±9		±1	±9	mV
	V_{OS} Temperature Coefficient				±5			±5			±5		µV/°C
GE	Gain Error		●		±0.1	±0.7		±0.1	±0.7		±0.1	±0.7	%FSR
	Gain Temperature Coefficient				±8			±8			±8		ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), V_{OUT} unloaded, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSR	Power Supply Rejection	V_{CC} ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{REF} = V_{CC} = 5V, Midscale; –15mA ≤ I_{OUT} ≤ 15mA	●		0.02	0.15	Ω
		V_{REF} = V_{CC} = 2.7V, Midscale; –7.5mA ≤ I_{OUT} ≤ 7.5mA	●		0.03	0.15	Ω
	DC Crosstalk (Note 10)	Due to Full Scale Output Change (Note 11)			±10		µV
		Due to Load Current Change			±3.5		µV/mA
		Due to Powering Down (per Channel)			±7		µV
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.5V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	15	34	60	mA
		Code: Full Scale; Forcing Output to GND	●	15	34	60	mA
		V_{CC} = 2.7V, V_{REF} = 2.7V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	7.5	20	50	mA
		Code: Full Scale; Forcing Output to GND	●	7.5	27	50	mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	11	16	20	kΩ
	Capacitance				90		pF
I_{REF}	Reference Current, Power Down Mode	DAC Powered Down	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3)	●		2.50	4.0	mA
		V_{CC} = 3V (Note 3)	●		2.00	3.2	mA
		DAC Powered Down (Note 3) V_{CC} = 5V	●		0.38	1.0	µA
		DAC Powered Down (Note 3) V_{CC} = 3V	●		0.16	1.0	µA
Digital I/O (Note 9)							
V_{IL}	Low Level Input Voltage (SDA and SCL)		●			0.3V_{CC}	V
V_{IH}	High Level Input Voltage (SDA and SCL)		●	0.7V_{CC}			V
$V_{IL(CA)}$	Low Level Input Voltage (CA0 to CA2)	See Test Circuit 1	●			0.15V_{CC}	V
$V_{IH(CA)}$	High Level Input Voltage (CA0 to CA2)	See Test Circuit 1	●	0.85V_{CC}			V
R_{INH}	Resistance from CA_n (n = 0,1,2) to V_{CC} to Set CA_n = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA_n (n = 0,1,2) to GND to Set CA_n = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA_n (n = 0,1,2) to V_{CC} or GND to Set CA_n = FLOAT	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	V_O = $V_{IH(MIN)}$ to V_O = $V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 7)	●	20 + 0.1C_B		250	ns
t_{SP}	Pulse Width of Spikes Surpassed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	0.1V_{CC} ≤ V_{IN} ≤ 0.9V_{CC}	●			1	µA
C_{IN}	I/O Pin Capacitance	(Note 12)	●			10	pF
C_B	Capacitance Load for Each Bus Line		●			400	pF
C_{CAn}	External Capacitive Load on Address Pins CA0, CA1 and CA2		●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC2625/-1 MIN	LTC2625/-1 TYP	LTC2625/-1 MAX	LTC2615/-1 MIN	LTC2615/-1 TYP	LTC2615/-1 MAX	LTC2605/-1 MIN	LTC2605/-1 TYP	LTC2605/-1 MAX	UNITS
AC Performance												
t_S	Settling Time (Note 5)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		7			7 9			7 9 10		µs µs µs
	Settling Time for 1LSB Step (Note 6)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		2.7			2.7 4.8			2.7 4.8 5.2		µs µs µs
	Voltage Output Slew Rate			0.80			0.80			0.80		V/µs
	Capacitive Load Driving			1000			1000			1000		pF
	Glitch Impulse	At Midscale Transition		12			12			12		nV • s
	Multiplying Bandwidth			180			180			180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz		120 100			120 100			120 100		nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz		15			15			15		μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1) (Notes 8, 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 2.7V to 5.5V							
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Program		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time of Both SDA and SCL Signals	(Note 7)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time of Both SDA and SCL Signals	(Note 7)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Linearity and monotonicity are defined from code k_L to code $2^N - 1$, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256 and linearity is defined from code 256 to code 65,535.

Note 3: SDA, SCL at 0V or V_{CC}, CA0, CA1 and CA2 floating.

Note 4: Inferred from measurement at code 256 (LTC2605/LTC2605-1), code 64 (LTC2615/LTC2615-1) or code 16 (LTC2625/LTC2625-1) and at full scale.

Note 5: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 200pF to GND.

Note 6: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped ±1LSB between half scale and half scale – 1. Load is 2kΩ in parallel with 200pF to GND.

Note 7: C_B = capacitance of one bus line in pF.

Note 8: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 9: These specifications apply to LTC2605/LTC2605-1, LTC2615/LTC2615-1 and LTC2625/LTC2625-1.

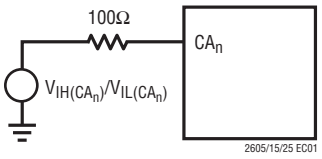
Note 10: DC Crosstalk is measured with V_{CC} = 5V and V_{REF} = 4096V, with the measured DAC at midscale, unless otherwise noted.

Note 11: R_L = 2kΩ to GND or V_{CC}.

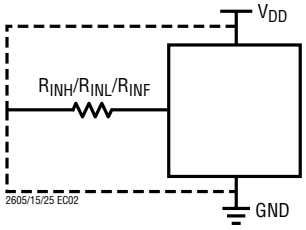
Note 12: Guaranteed by design and not production tested.

ELECTRICAL CHARACTERISTICS

Test Circuit 1



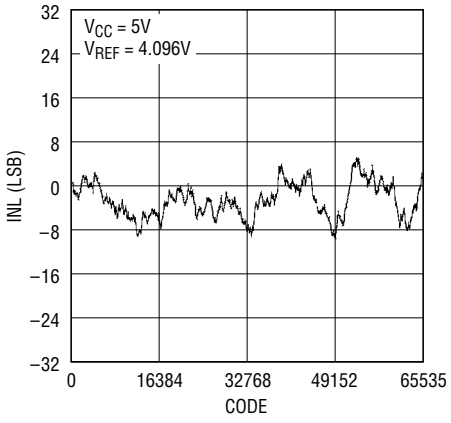
Test Circuit 2



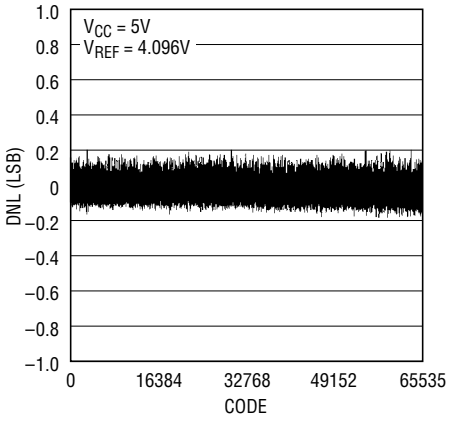
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2605

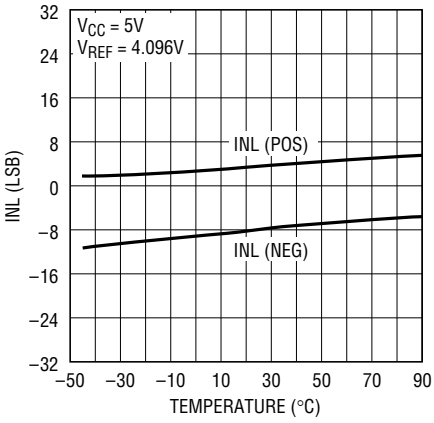
Integal Nonlinearity (INL)



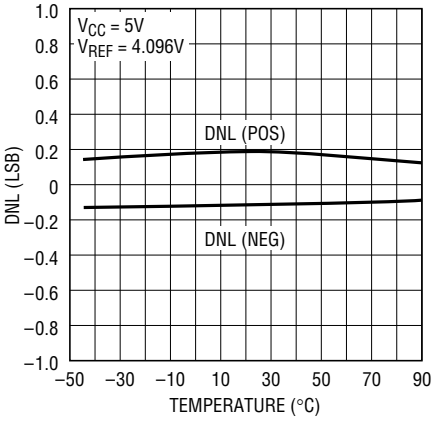
Differential Nonlinearity (DNL)



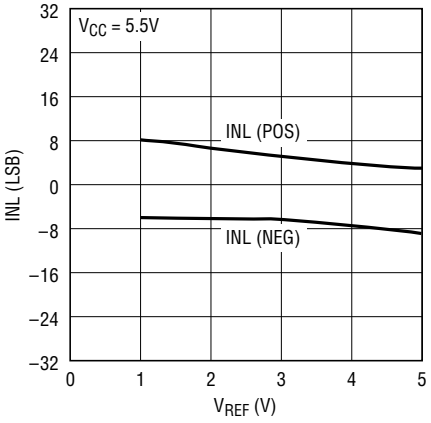
INL vs Temperature



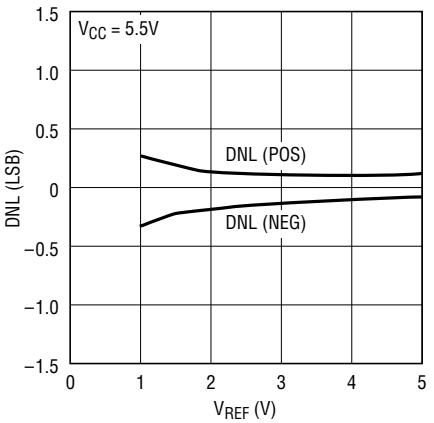
DNL vs Temperature



INL vs V_{REF}



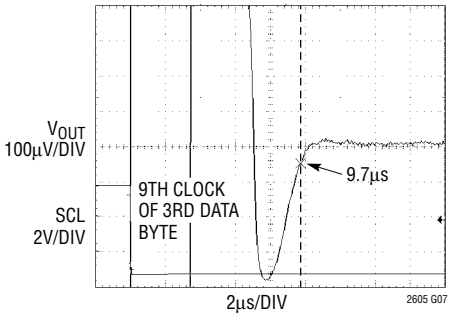
DNL vs V_{REF}



TYPICAL PERFORMANCE CHARACTERISTICS

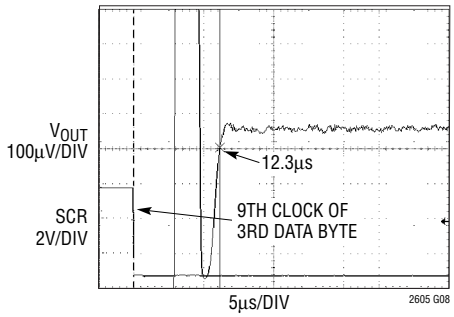
LTC2605

Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

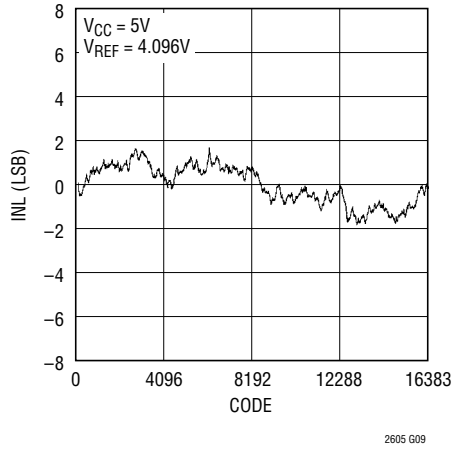
Settling of Full-Scale Step



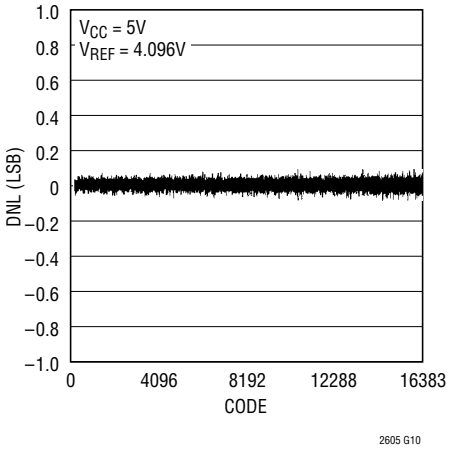
SETTLING TO ±1LSB
V_{CC} = 5V, V_{REF} = 4.096V
CODE 512 TO 65535 STEP
AVERAGE OF 2048 EVENTS

LTC2615

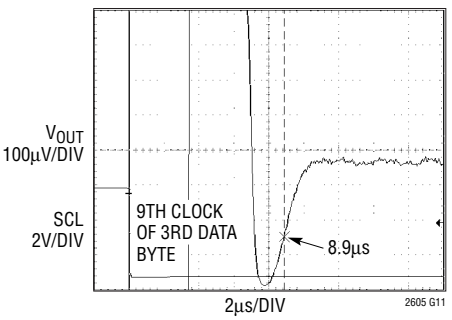
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



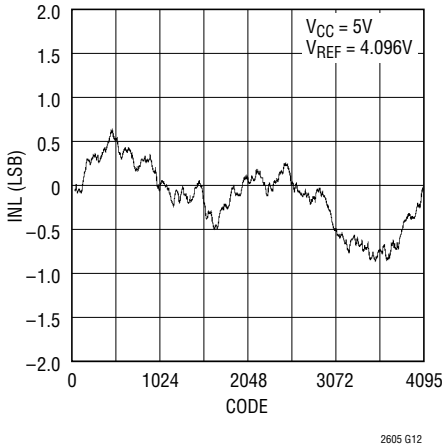
Settling to ±1LSB



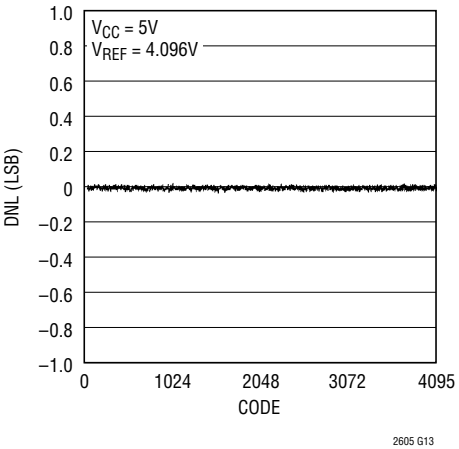
V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

LTC2625

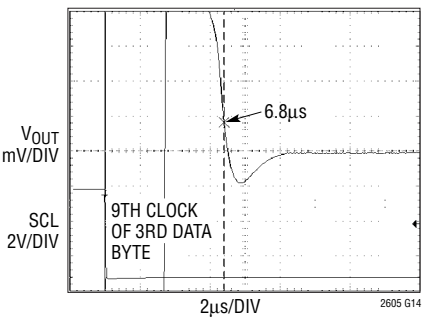
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



Settling to ±1LSB

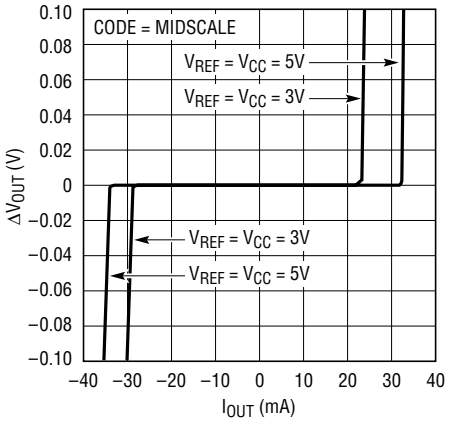


V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

TYPICAL PERFORMANCE CHARACTERISTICS

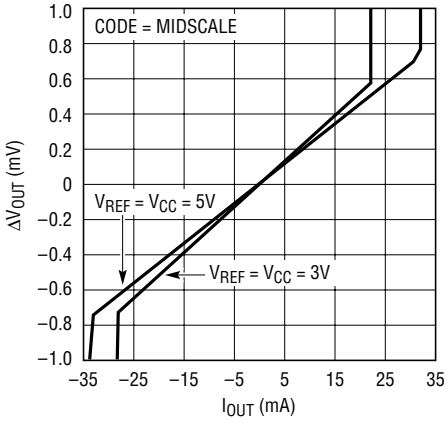
LTC2605/LTC2615/LTC2625

Current Limiting



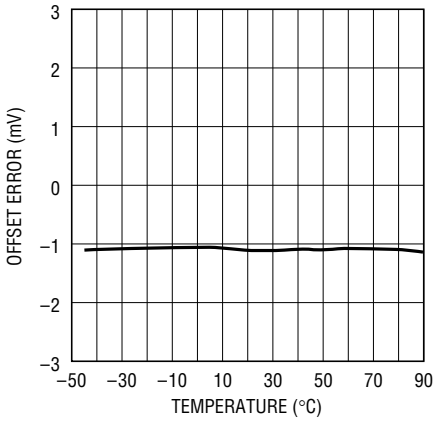
2605 G15

Load Regulation



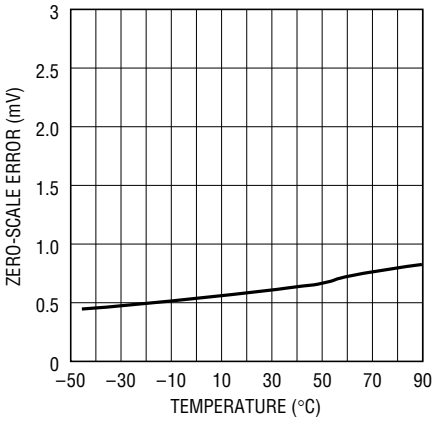
2606 G16

Offset Error vs Temperature



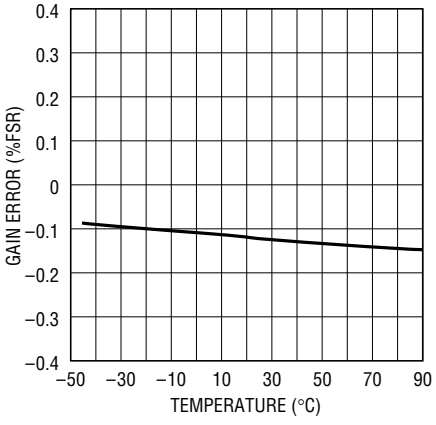
2605 G17

Zero-Scale Error vs Temperature



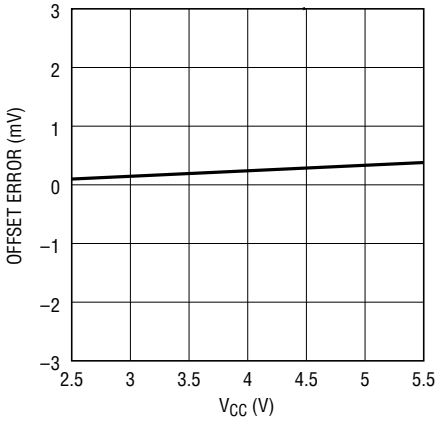
2605 G18

Gain Error vs Temperature



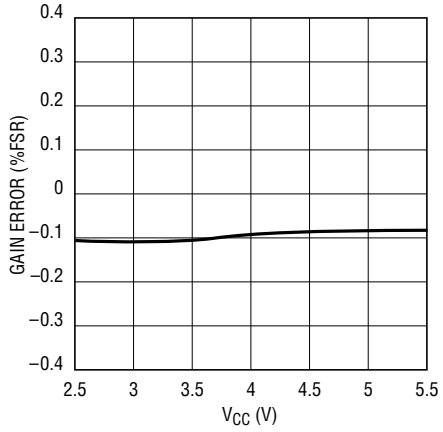
2605 G19

Offset Error vs V_{CC}



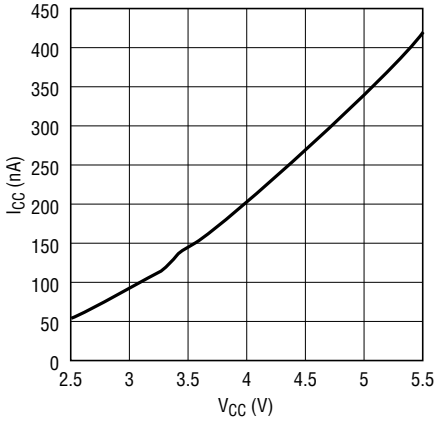
2605 G20

Gain Error vs V_{CC}



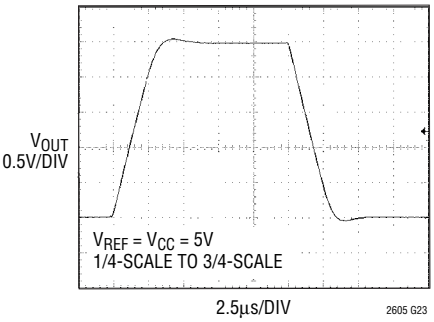
2605 G21

I_{CC} Shutdown vs V_{CC}



2605 G22

Large-Signal Response

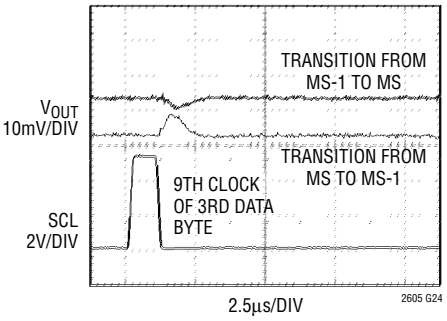


2605 G23

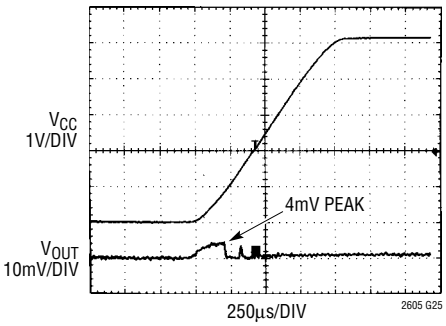
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2605/LTC2615/LTC2625

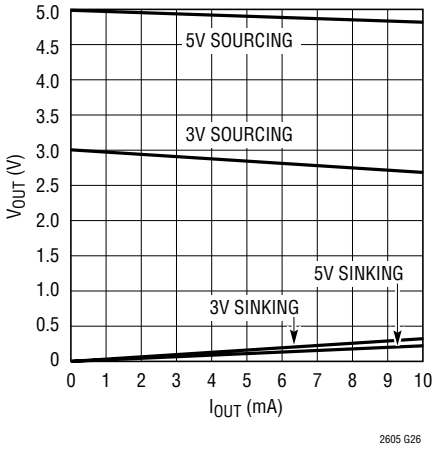
Midscale Glitch Impulse



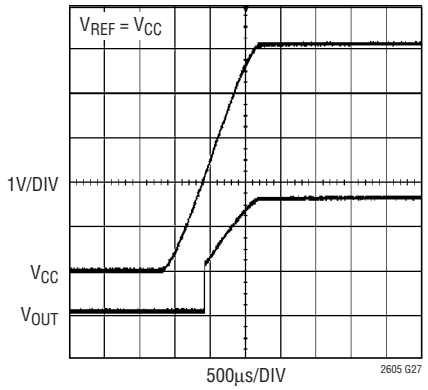
Power-On Reset Glitch



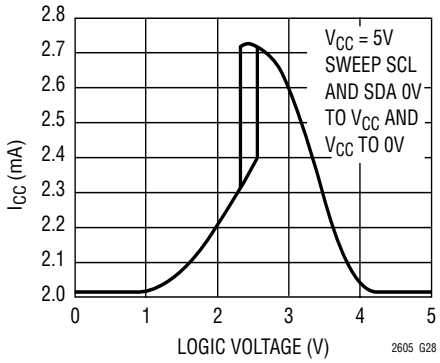
Headroom at Rails vs Output Current



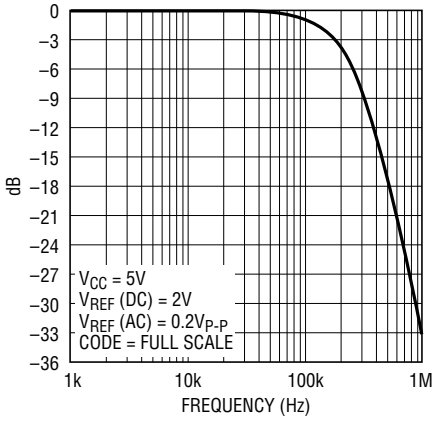
Power-On Reset to Midscale



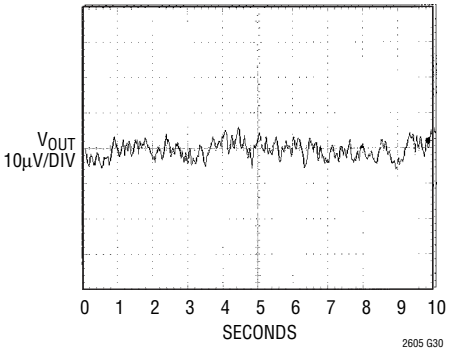
Supply Current vs Logic Voltage



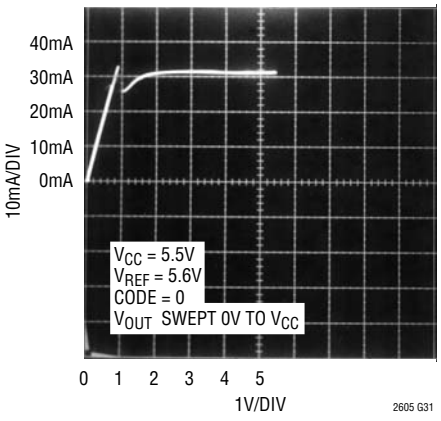
Multiplying Bandwidth



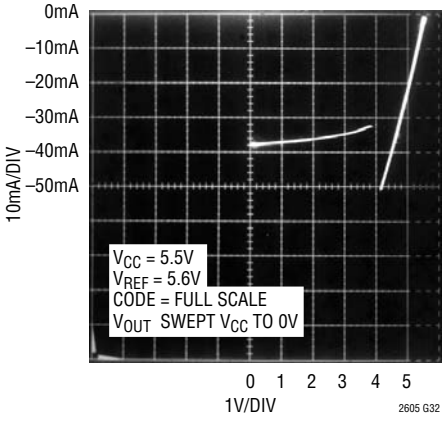
Output Voltage Noise, 0.1Hz to 10Hz



Short-Circuit Output Current vs VOUT (Sinking)



Short-Circuit Output Current vs VOUT (Sourcing)



PIN FUNCTIONS

GND (Pin 1): Analog Ground.

$V_{OUT\ A}$ to $V_{OUT\ H}$ (Pins 2-5 and 12-15): DAC Analog Voltage Output. The output range is 0V to V_{REF}.

REF (Pin 6): Reference Voltage Input. $0V \le V_{REF} \le V_{CC}$.

CA2 (Pin 7): Chip Address Bit 2. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 2).

SCL (Pin 8): Serial Clock Input Pin. Data is shifted into the SDA pin at the rising edges of the clock. This high impedance pin requires a pull-up resistor or current source to V_{CC}.

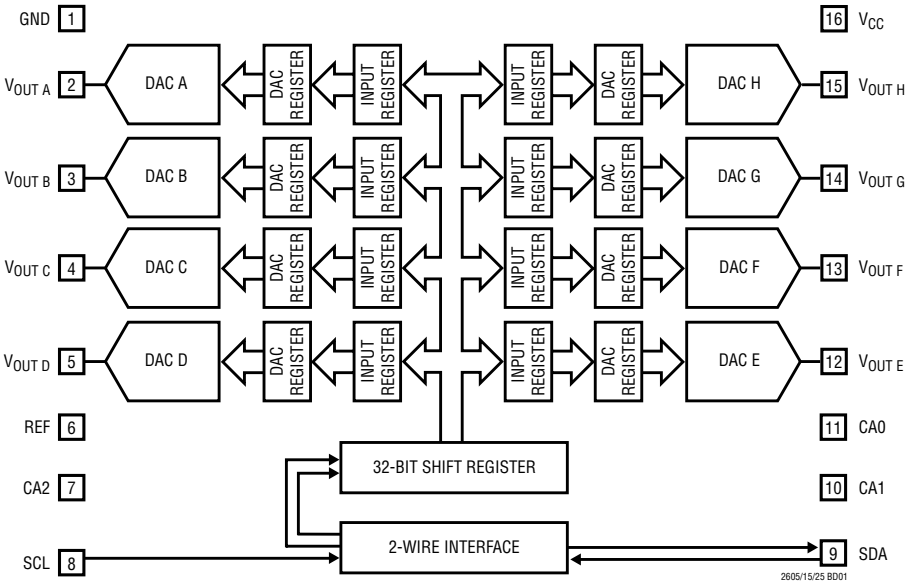
SDA (Pin 9): Serial Data Bidirectional Pin. Data is shifted into the SDA pin and acknowledged by the SDA pin. This is a high impedance pin while data is shifted in. It is an open-drain N-channel output during acknowledgment. This pin requires a pull-up resistor or current source to V_{CC}.

CA1 (Pin 10): Chip Address Bit 1. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 2).

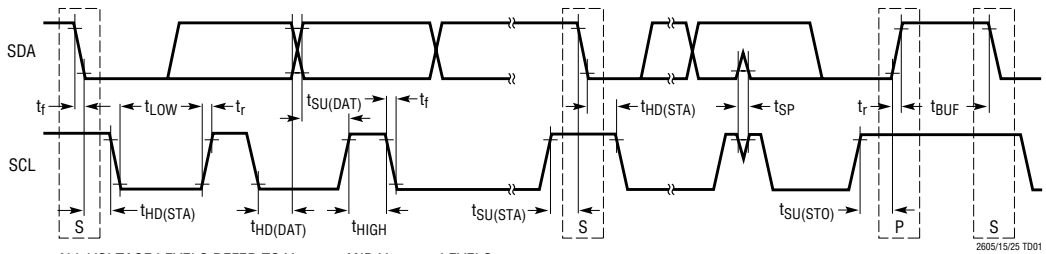
CA0 (Pin 11): Chip Address Bit 0. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 2).

V_{CC} (Pin 16): Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$.

BLOCK DIAGRAM



TIMING DIAGRAM



ALL VOLTAGE LEVELS REFER TO $V_{IH(MIN)}$ AND $V_{IL(MAX)}$ LEVELS

Figure 1

OPERATION

Power-On Reset

The LTC2605/LTC2615/LTC2625 clear the outputs to zero scale when power is first applied, making system initialization consistent and repeatable. The LTC2605-1/LTC2615-1/LTC2625-1 set the voltage outputs to midscale when power is first applied.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2605/LTC2615/LTC2625 contain circuitry to reduce the power-on glitch: the analog outputs typically rise less than 10mV above zero scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 16) is in transition.

Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is the voltage at REF (Pin 6).

Serial Digital Interface

The LTC2605/LTC2615/LTC2625 communicate with a host using the standard 2-wire digital interface. The Timing Diagram (Figure 1) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The value of these pull-up resistors is dependent on the power supply and can be obtained from the I^2C specifications. For an I^2C bus operating in the fast mode, an active pull-up will be necessary if the bus capacitance is greater than 200pF.

The LTC2605/LTC2615/LTC2625 are receive-only (slave) devices. The master can write to the LTC2605/LTC2615/LTC2625. The LTC2605/LTC2615/LTC2625 do not respond to a read from the master.

The START (S) and STOP (P) Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high.

When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Table 1.

COMMAND*				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power Up) All n
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
1	1	1	1	No Operation

*Address and command codes not shown are reserved and should not be used.

ADDRESS (n)*				
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

OPERATION

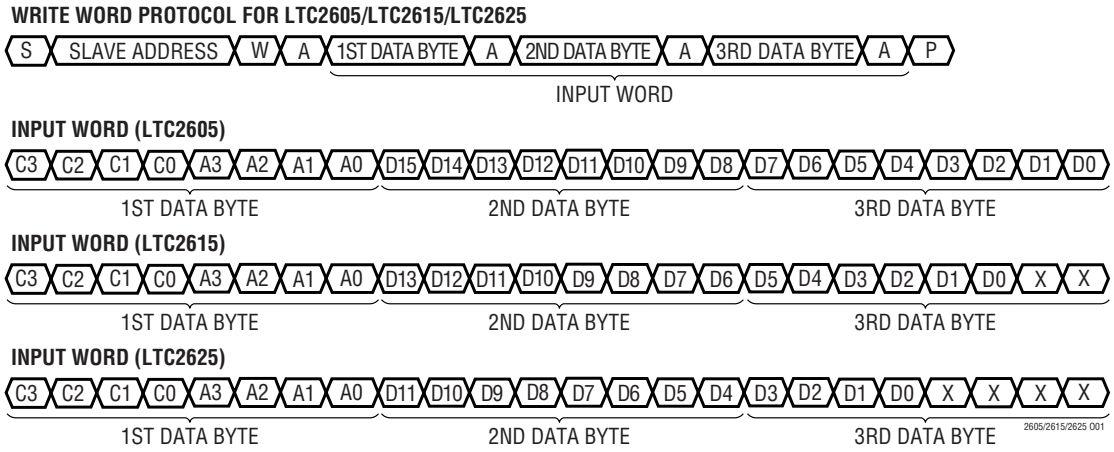


Figure 2

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave-receiver must pull down the SDA during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse. The LTC2605/LTC2615/LTC2625 respond to a write by a master in this manner. The LTC2605/LTC2615/LTC2625 do not acknowledge a read (it retains SDA HIGH during the period of the Acknowledge clock pulse).

Chip Address

The state of CA0, CA1 and CA2 decides the slave address of the part. The pins CA0, CA1 and CA2 can be each set to any one of three states: V_{CC}, GND or FLOAT. This results in 27 selectable addresses for the part. The addresses corresponding to the states of CA0, CA1 and CA2 and the global address are shown in Table 2.

In addition to the address selected by the address pins, the parts also respond to a global address. This address allows a common write to all LTC2605, LTC2615 and LTC2625 parts to be accomplished with one 3-byte write transaction on the I^2C bus. The global address is a 7-bit hardwired address and is not selectable by CA0, CA1 and CA2. The maximum capacitive load allowed on the address pins (CA0, CA1 and CA2) is 10pF.

Write Word Protocol

The master initiates communication with the LTC2605/LTC2615/LTC2625 with a START condition and a 7-bit slave address followed by the Write bit (W) = 0. The LTC2605/LTC2615/LTC2625 acknowledges by pulling the SDA pin low at the 9th clock if the 7-bit slave address matches the address of the parts (set by CA0, CA1 and CA2) or the global address. The master then transmits three bytes of data. The LTC2605/LTC2615/LTC2625 acknowledges each byte of data by pulling the SDA line low at the 9th clock of each data byte transmission. After receiving three complete bytes of data, the LTC2605/LTC2615/LTC2625 executes the command specified in the 24-bit input word.

If more than three data bytes are transmitted after a valid 7-bit slave address, the LTC2605/LTC2615/LTC2625 do not acknowledge the extra bytes of data (SDA is high during the 9th clock).

The format of the three data bytes is shown in Figure 2. The first byte of the input word consists of the 4-bit command and 4-bit DAC address. The next two bytes consist of the 16-bit data word. The 16-bit data word consists of the 16-, 14- or 12-bit input code, MSB to LSB, followed by 0, 2 or 4 don't care bits (LTC2605, LTC2615 and LTC2625 respectively). A typical I^2C write transaction is shown in Figure 3.

OPERATION

The command (C3-C0) and address (A3-A0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads the 16-bit data word from the 32-bit shift register into the input register of the selected DAC, n. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 16-, 14- or 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the block diagram.

Table 2. Slave Address Map

CA2	CA1	CA0	SA6	SA5	SA4	SA3	SA2	SA1	SA0
GND	GND	GND	0	0	1	0	0	0	0
GND	GND	FLOAT	0	0	1	0	0	0	1
GND	GND	V_{CC}	0	0	1	0	0	1	0
GND	FLOAT	GND	0	0	1	0	0	1	1
GND	FLOAT	FLOAT	0	1	0	0	0	0	0
GND	FLOAT	V_{CC}	0	1	0	0	0	0	1
GND	V_{CC}	GND	0	1	0	0	0	1	0
GND	V_{CC}	FLOAT	0	1	0	0	0	1	1
GND	V_{CC}	V_{CC}	0	1	1	0	0	0	0
FLOAT	GND	GND	0	1	1	0	0	0	1
FLOAT	GND	FLOAT	0	1	1	0	0	1	0
FLOAT	GND	V_{CC}	0	1	1	0	0	1	1
FLOAT	FLOAT	GND	1	0	0	0	0	0	0
FLOAT	FLOAT	FLOAT	1	0	0	0	0	0	1
FLOAT	FLOAT	V_{CC}	1	0	0	0	0	1	0
FLOAT	V_{CC}	GND	1	0	0	0	0	1	1
FLOAT	V_{CC}	FLOAT	1	0	1	0	0	0	0
FLOAT	V_{CC}	V_{CC}	1	0	1	0	0	0	1
V_{CC}	GND	GND	1	0	1	0	0	1	0
V_{CC}	GND	FLOAT	1	0	1	0	0	1	1
V_{CC}	GND	V_{CC}	1	1	0	0	0	0	0
V_{CC}	FLOAT	GND	1	1	0	0	0	0	1
V_{CC}	FLOAT	FLOAT	1	1	0	0	0	1	0
V_{CC}	FLOAT	V_{CC}	1	1	0	0	0	1	1
V_{CC}	V_{CC}	GND	1	1	1	0	0	0	0
V_{CC}	V_{CC}	FLOAT	1	1	1	0	0	0	1
V_{CC}	V_{CC}	V_{CC}	1	1	1	0	0	1	0
GLOBAL ADDRESS			1	1	1	0	0	1	1

Power Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than eight outputs are needed. When in power-down, the buffer amplifiers and reference inputs are disabled and draw essentially zero current. The DAC outputs are put into a high-impedance state, and the output pins are passively pulled to ground through individual 90k resistors. When all eight DACs are powered down, the bias generation circuit is also disabled. Input- and DAC- registers are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100_b in combination with the appropriate DAC address, (n). The 16-bit data word is ignored. The supply and reference currents are reduced by approximately 1/8 for each DAC powered down; the effective resistance at REF (Pin 6) rises accordingly, becoming a high-impedance input (typically >1GΩ) when all eight DACs are powered down.

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 1. The selected DAC is powered up as its voltage output is updated.

There is an initial delay as the DAC powers up before it begins its usual settling behavior. If less than eight DACs are in a powered-down state prior to the updated command, the power-up delay is 5µs. If, on the other hand, all eight DACs are powered down, then the bias generation circuit is also disabled and must be restarted. In this case, the power-up delay is greater: 12µs for V_{CC} = 5V, 30µs for V_{CC} = 3V.

Voltage Outputs

Each of the eight rail-to-rail amplifiers contained in these parts has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

OPERATION

DC output impedance is equivalent to load regulation and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifier's DC output impedance is 0.020Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 30Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 30Ω • 1mA = 30mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping "signal" and "power" grounds separated internally and by reducing shared internal resistance to just 0.005Ω.

The GND pin functions both as the node to which the reference and output voltages are referred and as a return path for power currents in the device. Because of this, careful thought should be given to the grounding scheme and board layout in order to ensure rated performance.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin of the part should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.020Ω), and will degrade DC crosstalk. Note that the LTC2605/LTC2615/LTC2625 are no more susceptible to these effects than other parts of their type; on the contrary, they allow layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit for the lowest codes as shown in Figure 4b. Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 4c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

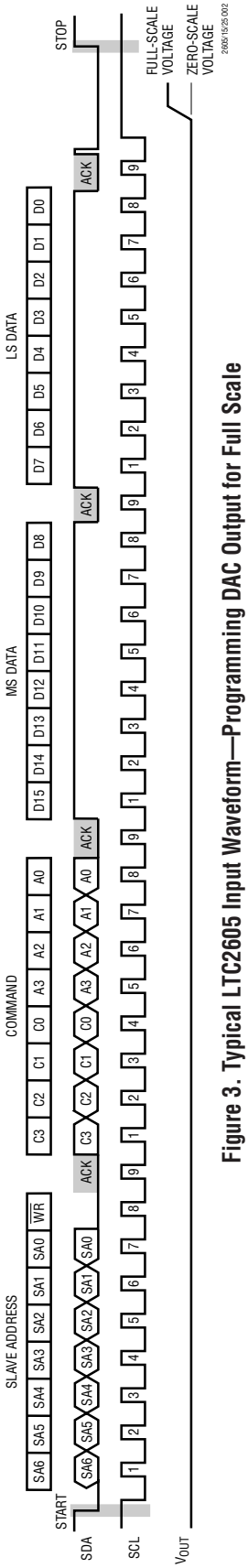


Figure 3. Typical LTC2605 Input Waveform—Programming DAC Output for Full Scale

OPERATION

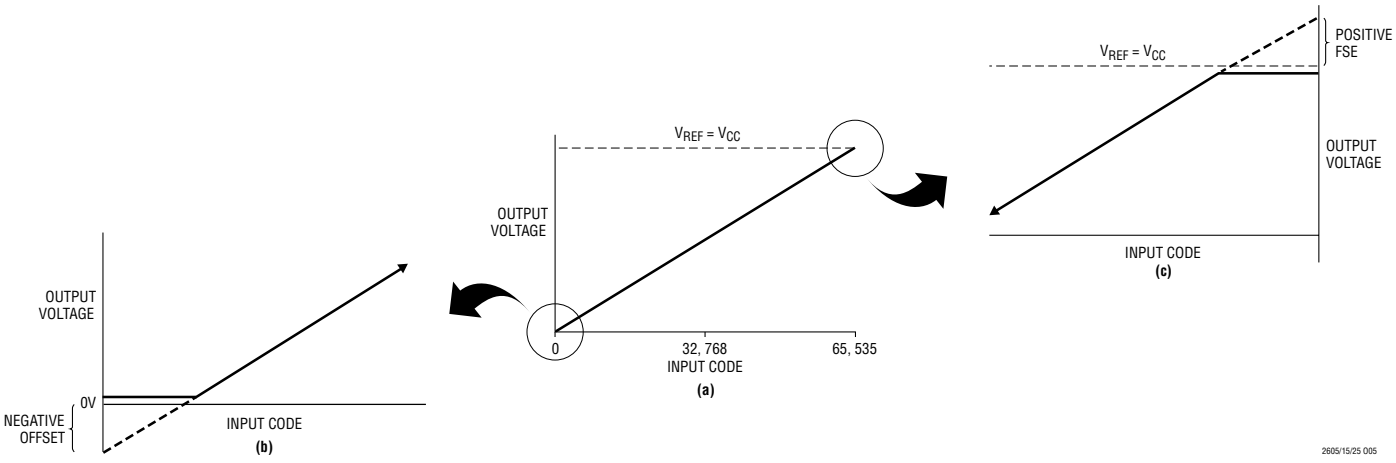
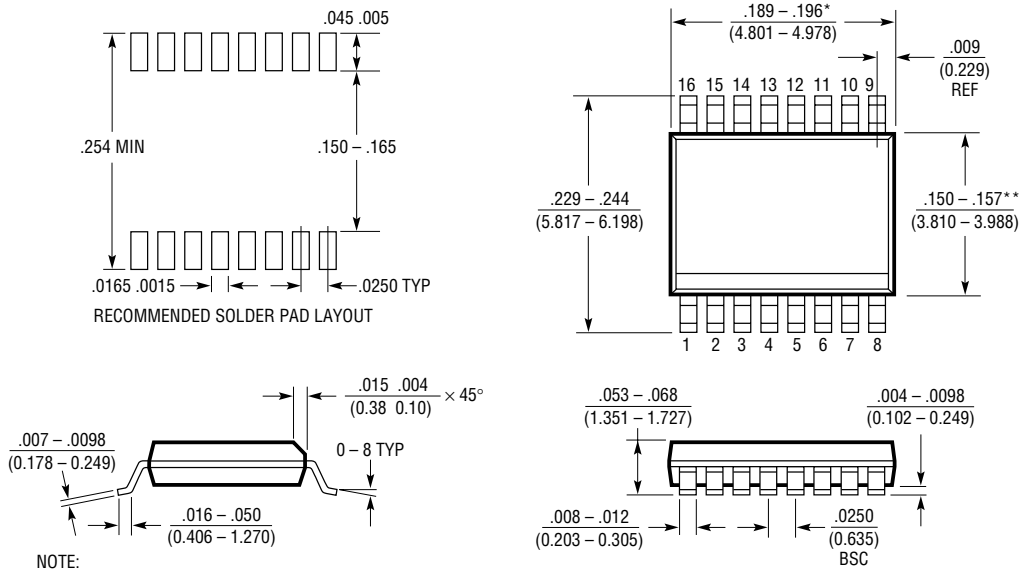


Figure 4. Effects of Rail-to-Rail Operation on a DAC Transfer Curve. (a) Overall Transfer Function, (b) Effect of Negative Offset for Codes Near Zero Scale, (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



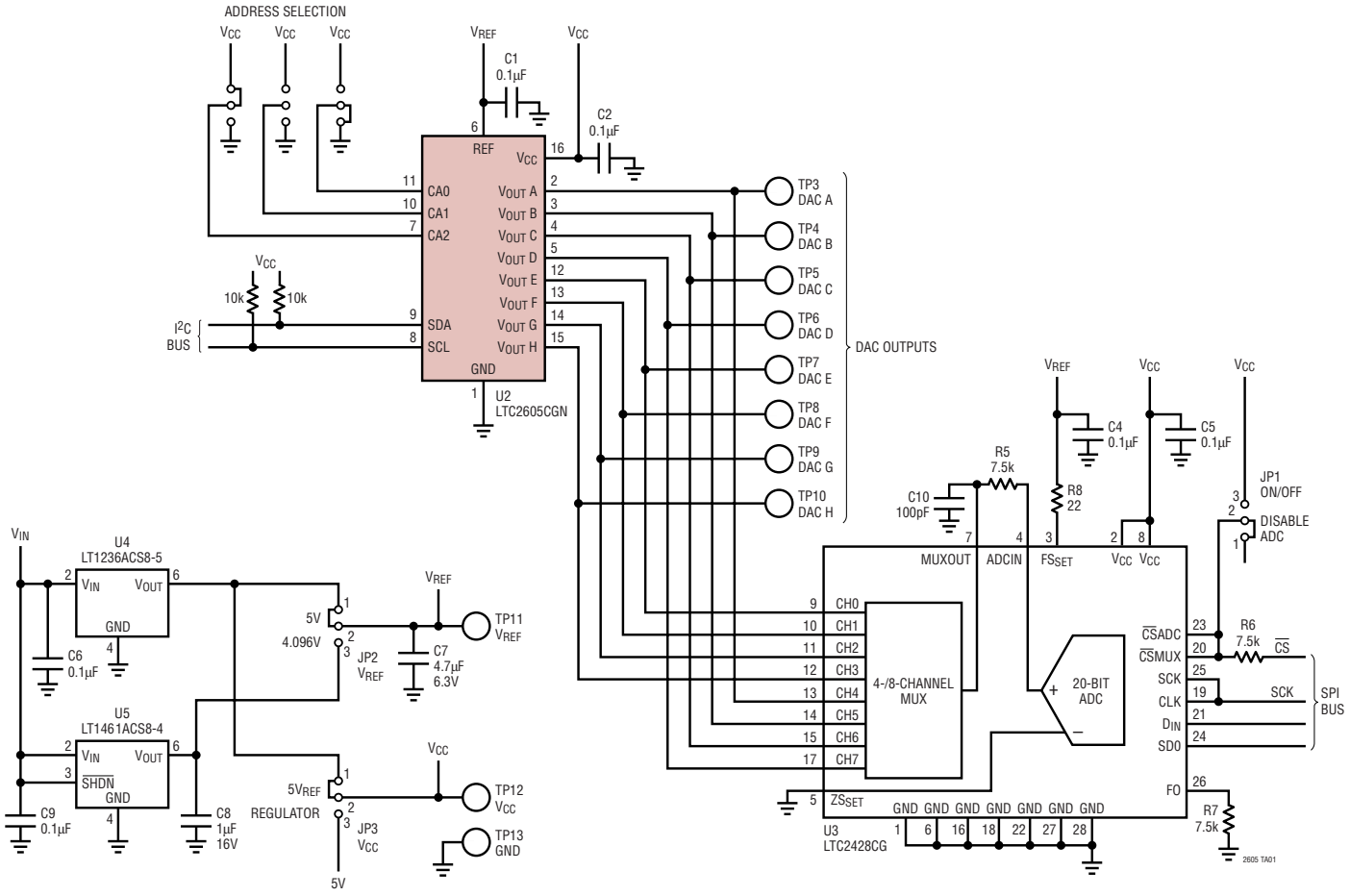
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Demonstration Circuit—LTC2428 20-Bit ADC Measures Key Performance Parameters



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5µs/750µA, 8µs/450µA
LTC1655/LTC1655L	Single 16-Bit V_{OUT} DAC with Serial Interface in SO-8	V_{CC} = 5V(3V), Low Power, Deglitched
LTC1657/LTC1657L	Parrallel 5V/3V 16-Bit V_{OUT} DAC	Low Power, Deglitched, Rail-to-Rail V_{OUT}
LTC1660/LTC1665	Octal 10-/8-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2µs for 10V Step
LTC2600/LTC2610/ LTC2620	Octal 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V–5.5V Supply Range, Rail-to-Rail Output, SPI Interface
LTC2601/LTC2611/ LTC2621	Single 16-/14-/12-Bit V_{OUT} DACs in 10-Lead DFN	300µA per DAC, 2.5V–5.5V Supply Range, Rail-to-Rail Output, SPI Interface
LTC2602/LTC2612/ LTC2622	Dual 16-/14-/12-Bit V_{OUT} DACs in 8-Lead MSOP	300µA per DAC, 2.5V–5.5V Supply Range, Rail-to-Rail Output, SPI Interface
LTC2604/LTC2614/ LTC2624	Quad 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V–5.5V Supply Range, Rail-to-Rail Output, SPI Interface
LTC2606/LTC2616/ LTC2626	Single 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface in 10-Lead DFN	270µA per DAC, 2.7V–5.5V Supply Range, Rail-to-Rail Output, I^2C Interface

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