16-/14-/12-Bit Rail-to-Rail DACs in 10-Lead DFN

FEATURES

- **Smallest Pin-Compatible Single DACs:**
  LTC2601: 16 Bits
  LTC2611: 14 Bits
  LTC2621: 12 Bits
- **Guaranteed Monotonic Over Temperature**
- Wide 2.5V to 5.5V Supply Range
- Low Power Operation: 300µA at 3V
- Power Down to 1µA, Max
- High Rail-to-Rail Output Drive (±15mA, Min)
- Double-Buffered Data Latches
- Asynchronous DAC Update Pin
- LTC2601-1/LTC2611-1/LTC2621-1: Power-On Reset to Midscale
- Tiny (3mm × 3mm) 10-Lead DFN Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

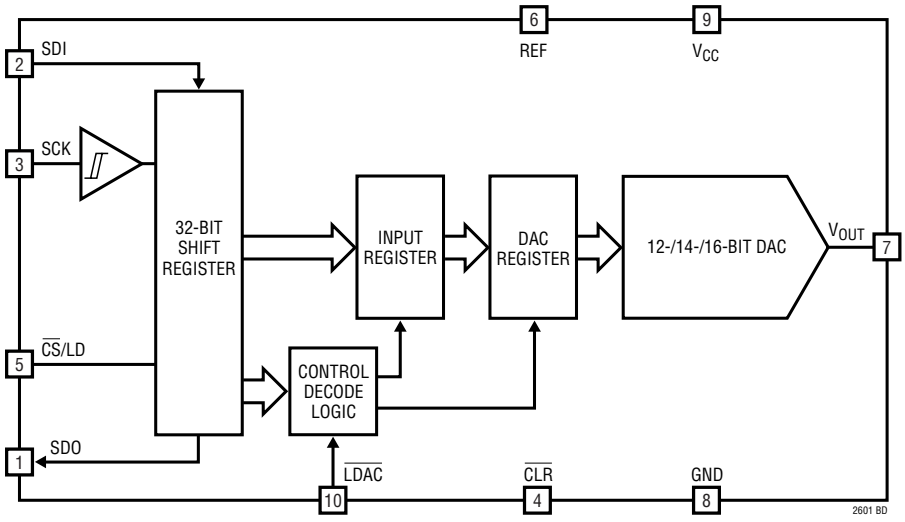
The LTC®2601/LTC2611/LTC2621 are single 16-, 14- and 12-bit, 2.5V-to-5.5V rail-to-rail voltage output DACs in a 10-lead DFN package. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish new board-density benchmarks for 16- and 14-bit DACs and advance performance standards for output drive and load regulation in single-supply, voltage-output DACs.

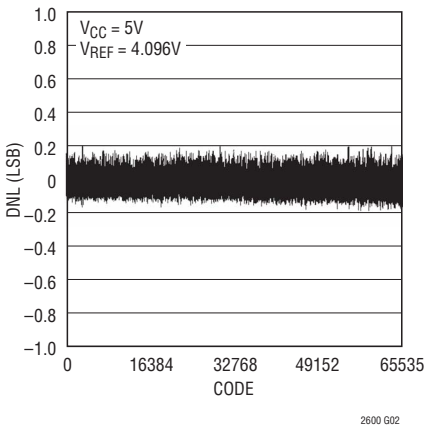
The parts use a simple SPI/MICROWIRE compatible 3-wire serial interface which can be operated at clock rates up to 50MHz. Daisy-chain capability, hardware $\overline{CLR}$ and asynchronous DAC update (LDAC) pins are included.

The LTC2601/LTC2611/LTC2621 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale until a valid write and update take place. The power-on reset circuit resets the LTC2601-1/LTC2611-1/LTC2621-1 to midscale. The voltage outputs stay at midscale until a valid write and update take place.

BLOCK DIAGRAM



Differential Nonlinearity (LTC2601)

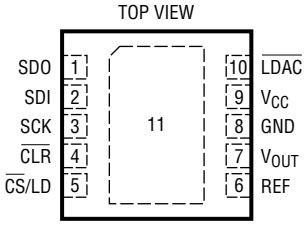


ABSOLUTE MAXIMUM RATINGS (Note 1)

Any Pin to GND ..... –0.3V to 6V
Any Pin to V_{CC} ..... –6V to 0.3V
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Temperature Range:
LTC2601C/LTC2611C/LTC2621C
LTC2601C-1/LTC2611C-1/LTC2621C-1 ... 0°C to 70°C
LTC2601I/LTC2611I/LTC2621I
LTC2601I-1/LTC2611I-1/LTC2621I-1 .. –40°C to 85°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DD PART MARKING
LTC2601CDD	LAGT
LTC2601IDD	LAGT
LTC2611CDD	LBFQ
LTC2611IDD	LBFQ
LTC2621CDD	LBFS
LTC2621IDD	LBFS
LTC2601CDD-1	LBZH
LTC2601IDD-1	LBZH
LTC2611CDD-1	LBZJ
LTC2611IDD-1	LBZJ
LTC2621CDD-1	LBZK
LTC2621IDD-1	LBZK

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.5V), V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2621/LTC2621-1 MIN	TYP	MAX	LTC2611/LTC2611-1 MIN	TYP	MAX	LTC2601/LTC2601-1 MIN	TYP	MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	(Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	(Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	(Note 2)	●		±0.8	±4		±3	±16		±13	±64	LSB
	Load Regulation	V_{REF} = V_{CC} = 5V, Midscale											
		I_{OUT} = 0mA to 15mA Sourcing	●		0.03	0.125		0.10	0.5		0.45	2	LSB/mA
		I_{OUT} = 0mA to 15mA Sinking	●		0.04	0.125		0.15	0.5		0.60	2	LSB/mA
		V_{REF} = V_{CC} = 2.5V, Midscale											
		I_{OUT} = 0mA to 7.5mA Sourcing	●		0.06	0.25		0.2	1		0.9	4	LSB/mA
		I_{OUT} = 0mA to 7.5mA Sinking	●		0.08	0.25		0.3	1		1.2	4	LSB/mA
ZSE	Zero-Scale Error	Code = 0	●		1	9		1	9		1	9	mV
V_{OS}	Offset Error	(Note 5)	●		±1.5	±9		±1.5	±9		±1.5	±9	mV
	V_{OS} Temperature Coefficient				±5			±5			±5		µV/°C

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.5V), V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2621/LTC2621-1 MIN	LTC2621/LTC2621-1 TYP	LTC2621/LTC2621-1 MAX	LTC2611/LTC2611-1 MIN	LTC2611/LTC2611-1 TYP	LTC2611/LTC2611-1 MAX	LTC2601/LTC2601-1 MIN	LTC2601/LTC2601-1 TYP	LTC2601/LTC2601-1 MAX	UNITS
GE	Gain Error		●		±0.03	±0.7		±0.1	±0.7		±0.05	±0.7	%FSR
	Gain Temperature Coefficient				±2			±2			±2		ppm/°C

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.5V), V_{OUT} unloaded, unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSR	Power Supply Rejection	V_{CC} = 5V ±10%			–80		dB
		V_{CC} = 3V ±10%	●		–80		dB
R_{OUT}	DC Output Impedance	V_{REF} = V_{CC} = 5V, Midscale; –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.15	Ω
		V_{REF} = V_{CC} = 2.5V, Midscale; –7.5mA ≤ I_{OUT} ≤ 7.5mA	●		0.05	0.15	Ω
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.5V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	15	35	60	mA
		Code: Full Scale; Forcing Output to GND	●	15	39	60	mA
		V_{CC} = 2.5V, V_{REF} = 2.5V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	7.5	20	50	mA
		Code: Full Scale; Forcing Output to GND	●	7.5	27	50	mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	88	124	160	kΩ
	Capacitance				15		pF
I_{REF}	Reference Current, Power Down Mode	DAC Powered Down	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3)	●		0.375	0.55	mA
		V_{CC} = 3V (Note 3)	●		0.30	0.45	mA
		DAC Powered Down (Note 3) V_{CC} = 5V	●		0.40	1	µA
		DAC Powered Down (Note 3) V_{CC} = 3V	●		0.10	1	µA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.5V to 5.5V	●	2.4			V
		V_{CC} = 2.5V to 3.6V	●	2.0			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V	●			0.8	V
		V_{CC} = 2.5V to 5.5V	●			0.6	V
V_{OH}	Digital Output High Voltage	Load Current = –100µA	●	V_{CC} – 0.4			V
V_{OL}	Digital Output Low Voltage	Load Current = +100µA	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 4)	●			8	pF

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.5V), V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC2621/LTC2621-1 MIN	LTC2621/LTC2621-1 TYP	LTC2621/LTC2621-1 MAX	LTC2611/LTC2611-1 MIN	LTC2611/LTC2611-1 TYP	LTC2611/LTC2611-1 MAX	LTC2601/LTC2601-1 MIN	LTC2601/LTC2601-1 TYP	LTC2601/LTC2601-1 MAX	UNITS
AC Performance												
t_S	Settling Time (Note 6)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		7			7 9			7 9 10		µs µs µs
	Settling Time for 1LSB Step (Note 7)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		2.7			2.7 4.8			2.7 4.8 5.2		µs µs µs
	Voltage Output Slew Rate			0.80			0.80			0.80		V/µs
	Capacitive Load Driving			1000			1000			1000		pF
	Glitch Impulse	At Midscale Transition		12			12			12		nV • s
	Multiplying Bandwidth			180			180			180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz		120 100			120 100			120 100		nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz		15			15			15		μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1) (Notes 4, 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 2.5V to 5.5V							
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse Width		●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_8	SDO Propagation Delay from SCK Falling Edge	C_{LOAD} = 10pF V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V	 ● ●			 20 45	 ns ns
t_9	$\overline{CLR}$ Pulse Width		●	20			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
t_{12}	$\overline{LDAC}$ Pulse Width		●	15			ns
t_{13}	$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition		●	200			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Linearity and monotonicity are defined from code k_L to code $2^N - 1$, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256 and linearity is defined from code 256 to code 65,535.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: Guaranteed by design and not production tested.

Note 5: Inferred from measurement at code $K_L = 0.016(2^N/V_{REF})$ and at full scale.

Note 6: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2k in parallel with 200pF to GND.

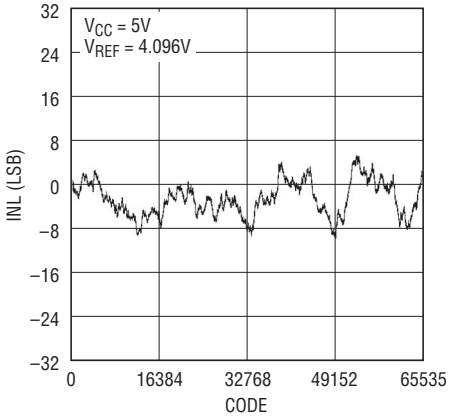
Note 7: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped ±1LSB between half scale and half scale – 1. Load is 2k in parallel with 200pF to GND.

Note 8: These specifications apply to LTC2601/LTC2601-1, LTC2611/LTC2611-1, LTC2621/LTC2621-1

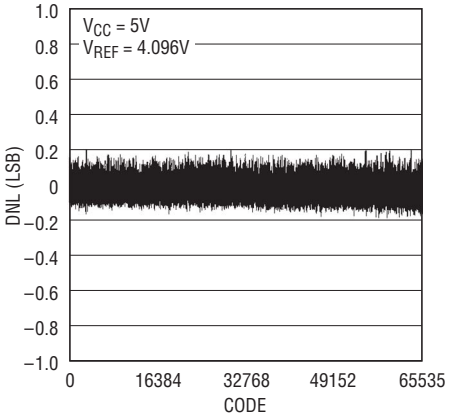
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2601

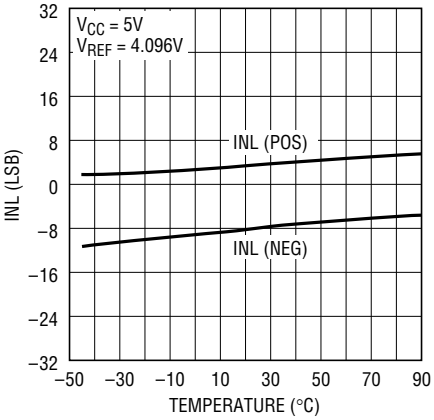
Integral Nonlinearity (INL)



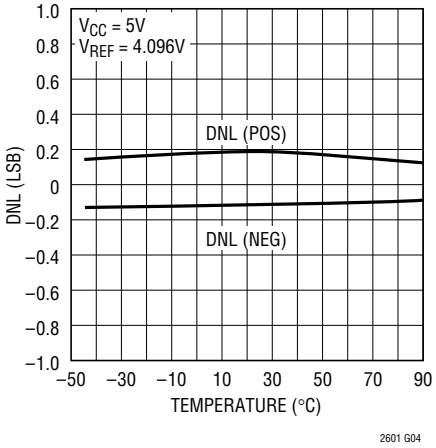
Differential Nonlinearity (DNL)



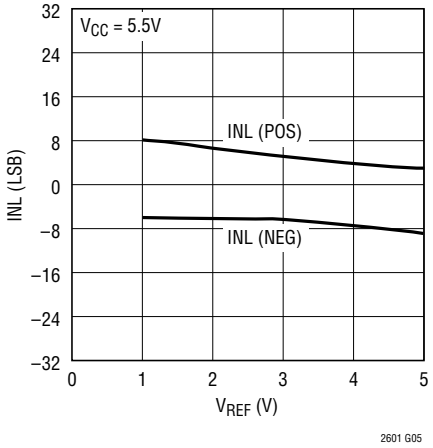
INL vs Temperature



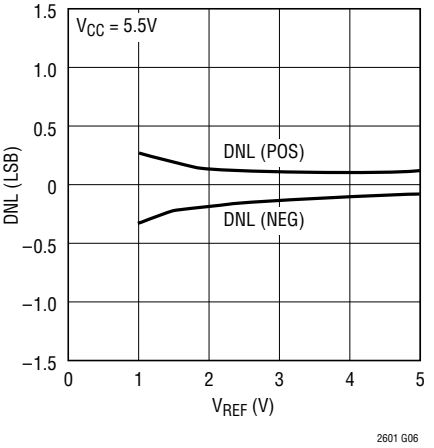
DNL vs Temperature



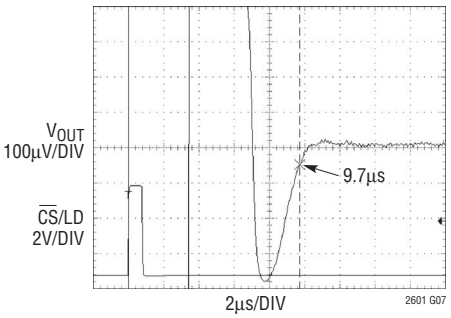
INL vs V_{REF}



DNL vs V_{REF}

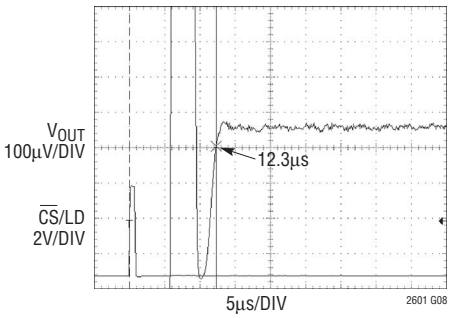


Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

Settling of Full-Scale Step

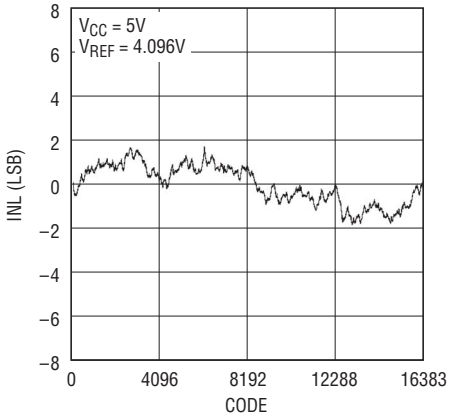


SETTLING TO ±1LSB
V_{CC} = 5V, V_{REF} = 4.096V
CODE 512 TO 65535 STEP
AVERAGE OF 2048 EVENTS

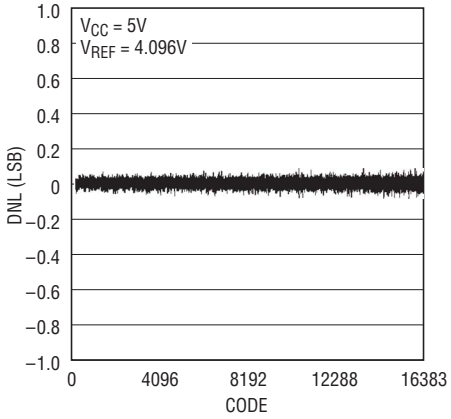
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2611

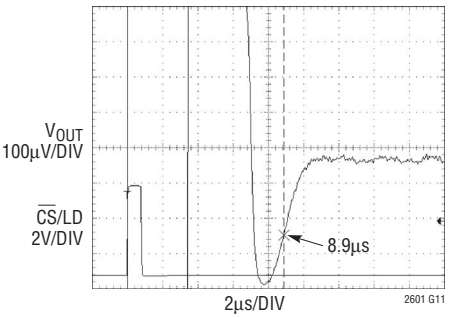
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



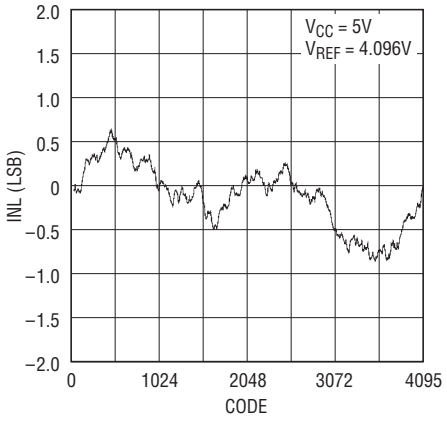
Settling to ±1LSB



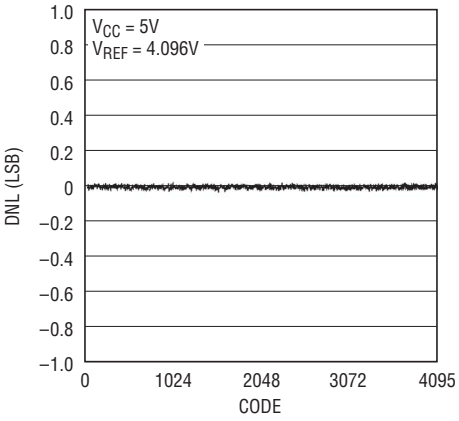
V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

LTC2621

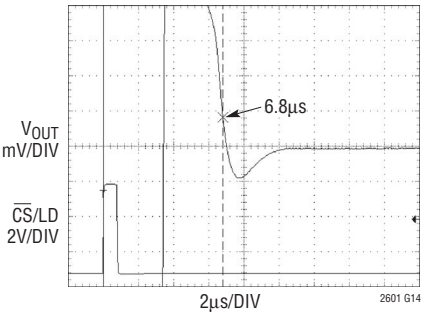
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



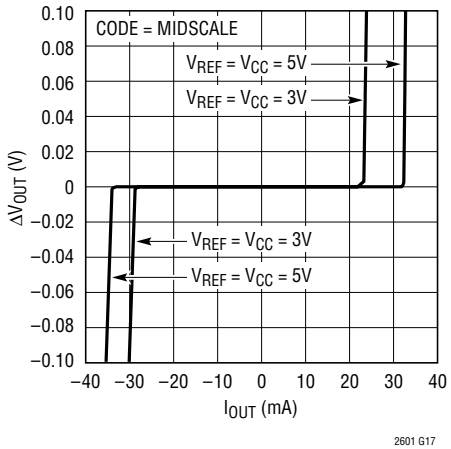
Settling to ±1LSB



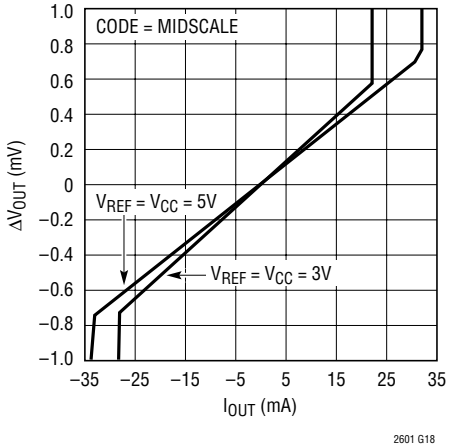
V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

LTC2601/LTC2611/LTC2621

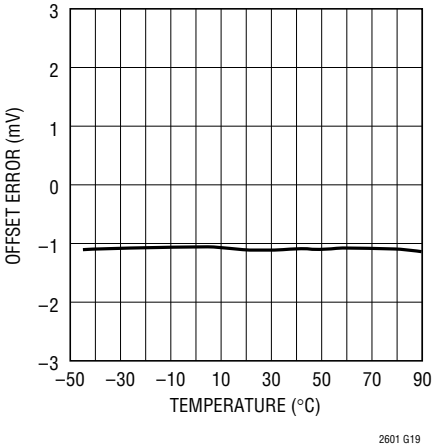
Current Limiting



Load Regulation



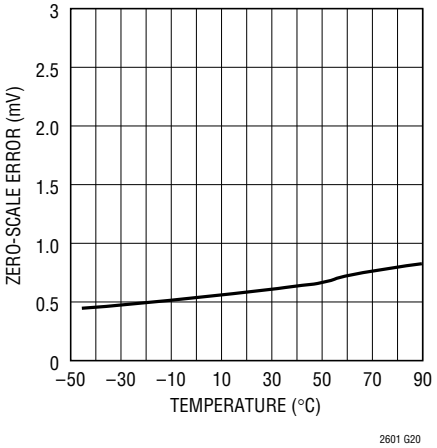
Offset Error vs Temperature



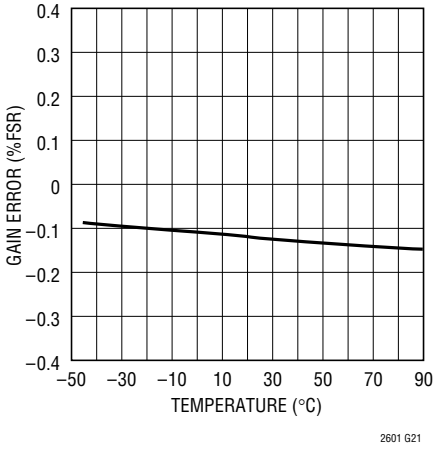
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2601/LTC2611/LTC2621

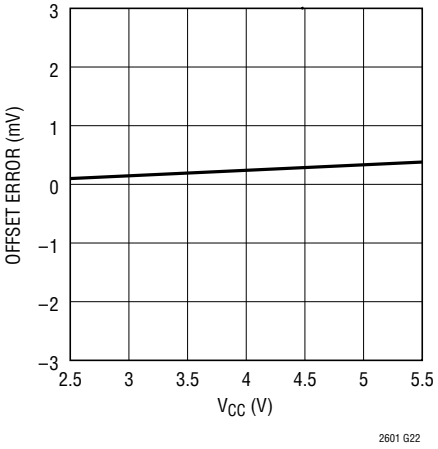
Zero-Scale Error vs Temperature



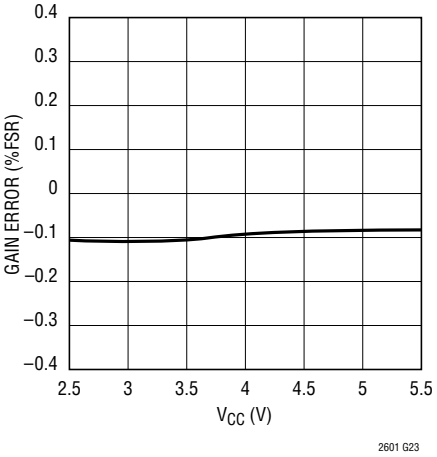
Gain Error vs Temperature



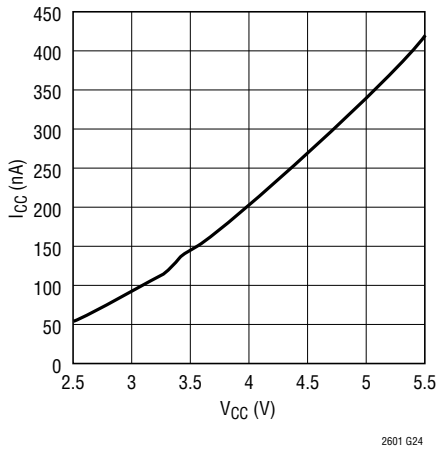
Offset Error vs V_{CC}



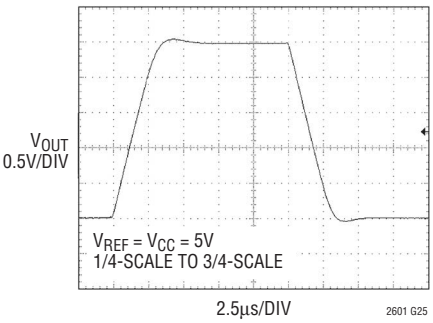
Gain Error vs V_{CC}



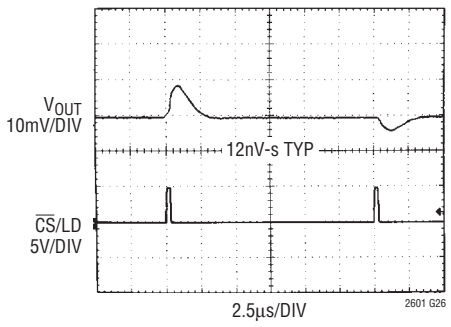
I_{CC} Shutdown vs V_{CC}



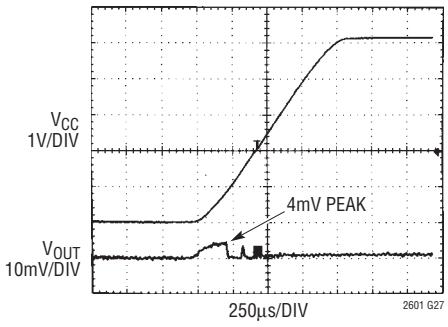
Large-Signal Response



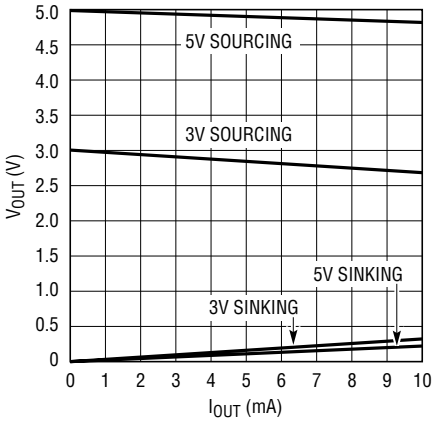
Midscale Glitch Impulse



Power-On Reset Glitch to Zero Scale



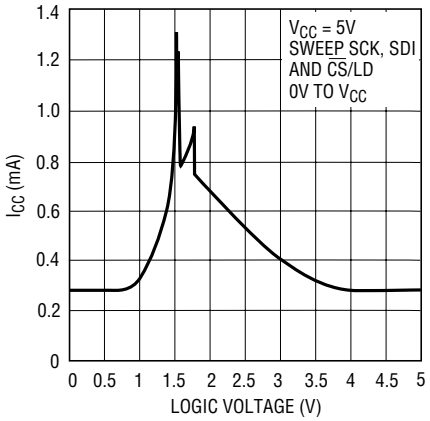
Headroom at Rails vs Output Current



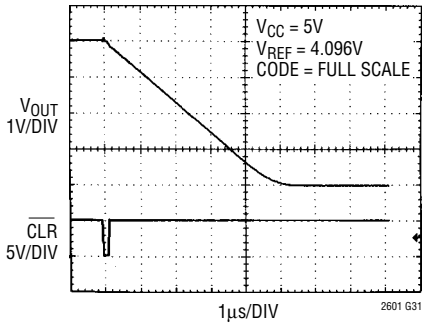
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2601/LTC2611/LTC2621

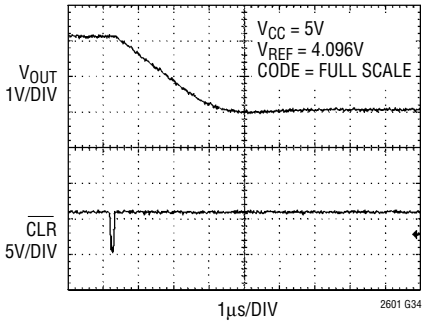
Supply Current vs Logic Voltage



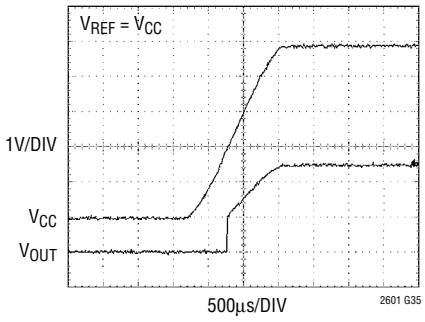
Hardware $\overline{CLR}$ to Zero Scale



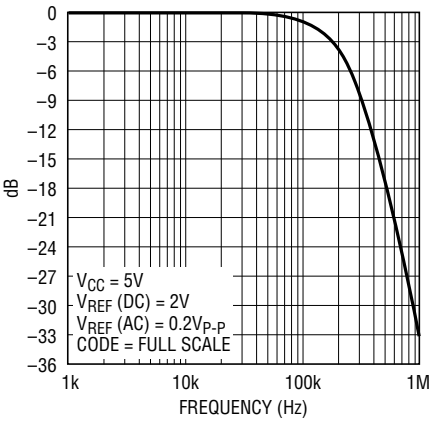
Hardware $\overline{CLR}$ to Midscale



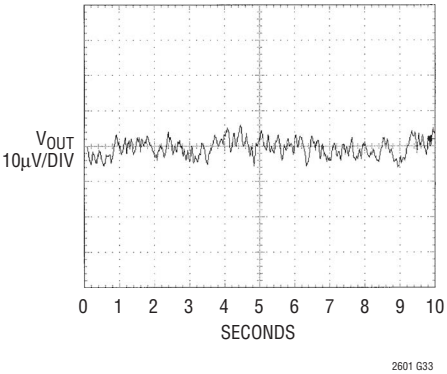
Power-On Reset to Midscale



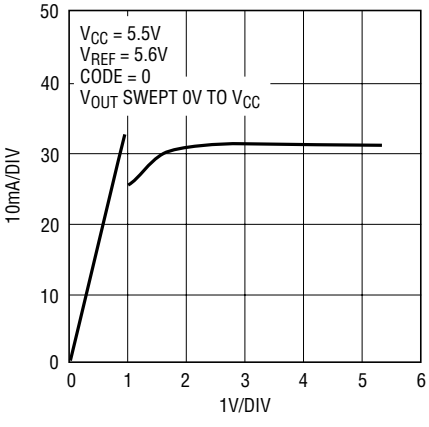
Multiplying Bandwidth



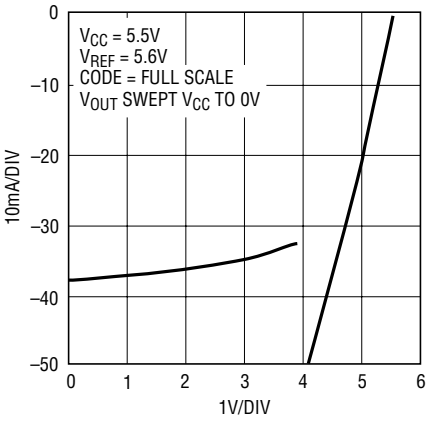
Output Voltage Noise, 0.1Hz to 10Hz



Short-Circuit Output Current vs V_{OUT} (Sinking)



Short-Circuit Output Current vs V_{OUT} (Sourcing)



PIN FUNCTIONS

SDO (Pin 1): Serial Interface Data Output. The serial output of the shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. This pin is used for daisy-chain operation.

SDI (Pin 2): Serial Interface Data Input. Data is applied to SDI for transfer to the device at the rising edge of SCK (Pin 3). The LTC2601 accepts input word lengths of either 24 or 32 bits.

SCK (Pin 3): Serial Interface Clock Input. CMOS and TTL compatible.

$\overline{\text{CLR}}$ (Pin 4): Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage outputs to drop to 0V for LTC2601/LTC2611/LTC2621. A logic low at this input sets all registers to midscale code and causes the DAC voltage outputs to go to midscale for LTC2601-1/LTC2611-1/LTC2621-1. CMOS and TTL compatible.

$\overline{\text{CS}}$/LD (Pin 5): Serial Interface Chip Select/Load Input. When $\overline{\text{CS}}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{\text{CS}}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

REF (Pin 6): Reference Voltage Input. $0V \leq V_{REF} \leq V_{CC}$.

V_{OUT} (Pin 7): DAC Analog Voltage Output. The output range is 0V to V_{REF}.

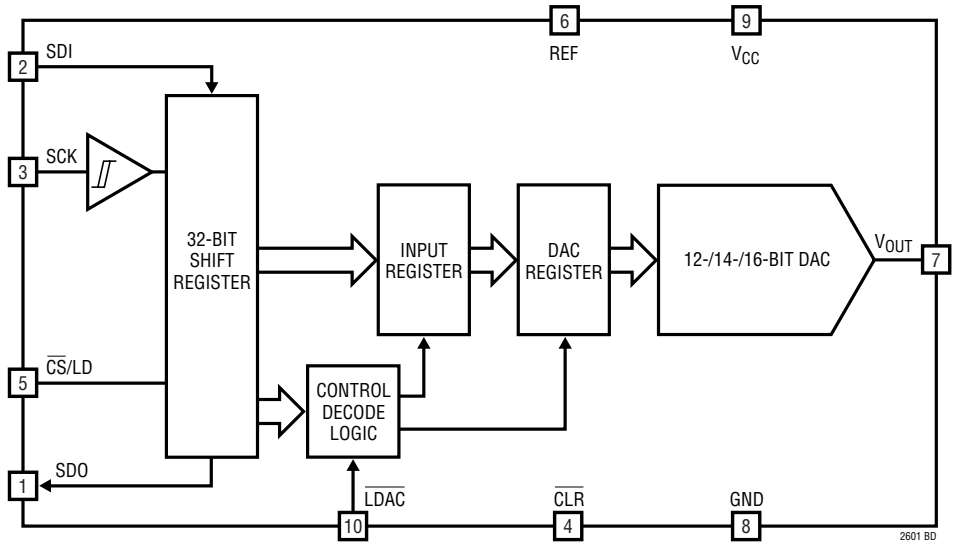
GND (Pin 8): Analog Ground.

V_{CC} (Pin 9): Supply Voltage Input. $2.5V \leq V_{CC} \leq 5.5V$.

$\overline{\text{LDAC}}$ (Pin 10): Asynchronous DAC Update Pin. If $\overline{\text{CS}}$/LD is high, a falling edge on $\overline{\text{LDAC}}$ immediately updates the DAC register with the contents of the input register (similar to a software update). If $\overline{\text{CS}}$/LD is low when $\overline{\text{LDAC}}$ goes low, the DAC register is updated after $\overline{\text{CS}}$/LD returns high. A low on the $\overline{\text{LDAC}}$ pin powers up the DAC. A software power down command is ignored if $\overline{\text{LDAC}}$ is low.

Exposed Pad (Pin 11): Ground. Must be soldered to PCB ground.

BLOCK DIAGRAM



TIMING DIAGRAMS

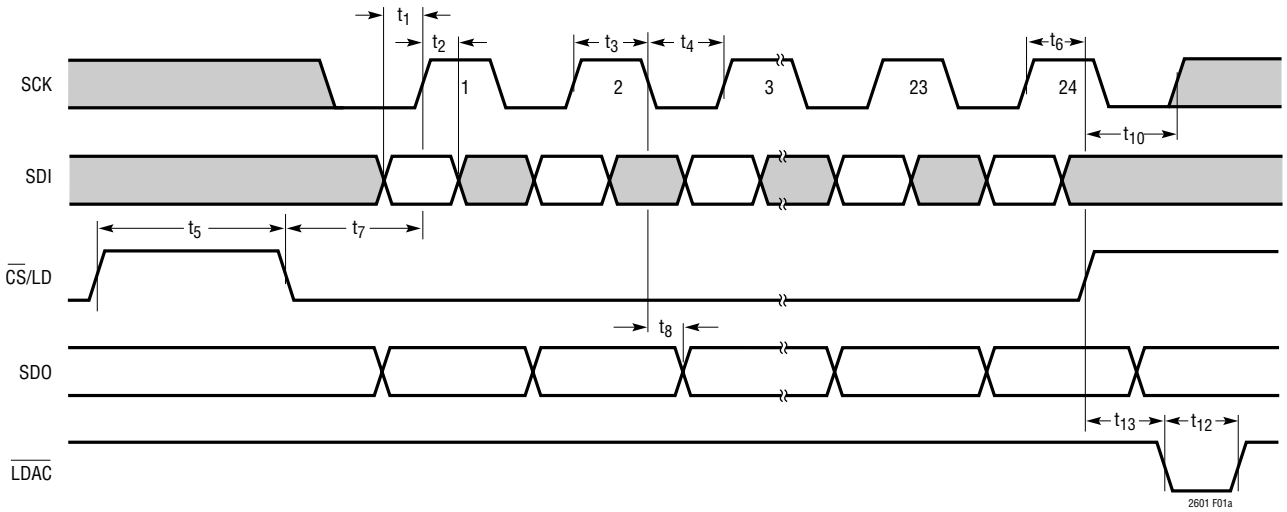


Figure 1a

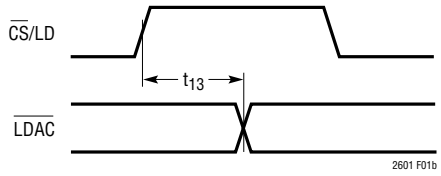


Figure 1b

OPERATION

Power-On Reset

The LTC2601/LTC2611/LTC2621 clear the outputs to zero scale when power is first applied, making system initialization consistent and repeatable. The LTC2601-1/LTC2611-1/LTC2621-1 set the voltage outputs to midscale when power is first applied.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2601/LTC2611/LTC2621 contain circuitry to reduce the power-on glitch; furthermore, the glitch amplitude can be made arbitrarily small by reducing the ramp rate of the power supply. For example, if the power supply is ramped to 5V in 1ms, the analog outputs rise less than 10mV above ground (typ) during power-on. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 16) is in transition.

Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is the voltage at REF (Pin 6).

Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, powering-on the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then 4 don't care bits; and finally the 16-bit data word. The data word comprises the 16-, 14- or 12-bit input code, ordered MSB-to-LSB, followed by 0, 2 or 4 don't care bits (LTC2601, LTC2611 and LTC2621 respectively). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to execute the command specified in the 24-bit input word. The complete sequence is shown in Figure 2a.

The command (C3-C0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the DAC. In an update operation, the data word is copied from the input register to the DAC register and converted to an analog voltage at the DAC output. The update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits are transferred to the device first, followed by the 24-bit word as just described. Figure 2b shows the 32-bit sequence. The 32-bit word is required for daisy-chain operation, and is also available to accommodate microprocessors which have a minimum word width of 16 bits (2 bytes).

Daisy-Chain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a "daisy chain" series is configured by connecting SDO of each upstream device to SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single

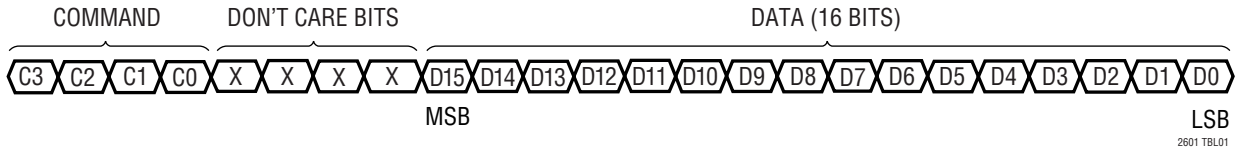
Table 1.

COMMAND*				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register
0	0	0	1	Update (Power Up) DAC Register
0	0	1	1	Write to and Update (Power Up)
0	1	0	0	Power Down
1	1	1	1	No Operation

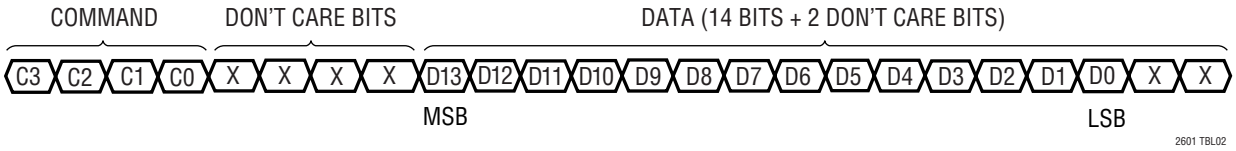
*Command codes not shown are reserved and should not be used.

OPERATION

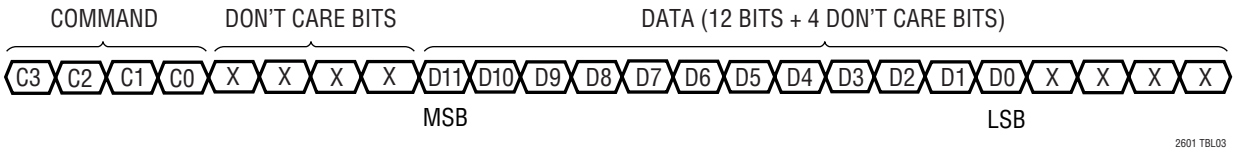
INPUT WORD (LTC2601)



INPUT WORD (LTC2611)



INPUT WORD (LTC2621)



input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then the concatenated input data is transferred to the chain, using SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, which executes the commands specified for each of the devices simultaneously. A single device can be controlled by using the no-operation command (1111) for the other devices in the chain.

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever the DAC output is not needed. When in power-down, the buffer amplifier, bias circuit and reference input is disabled and draws essentially zero current. The DAC output is put into a high impedance state, and the output pin is passively pulled to ground through 90k resistors. Input- and DAC-register contents are not disturbed during power-down.

The DAC can be put into power-down mode by using command 0100_b. The 16-bit data word is ignored. The supply and reference currents are reduced to almost zero when the DAC is powered down; the effective resistance at REF rises accordingly becoming a high impedance input (typically > 1GΩ).

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 1 or performing an asynchronous update ($\overline{LDAC}$) as described in the next section. The DAC is powered up as its voltage output is updated. When the DAC in powered-down state is powered up and updated, normal settling is delayed. The main bias generation circuit block has been automatically shut down in addition to the DAC amplifier and reference input and so the power up delay time is 12µs (for V_{CC} = 5V) or 30µs (for V_{CC} = 3V).

Asynchronous DAC Update Using $\overline{LDAC}$

In addition to the update commands shown in Table 1, the $\overline{LDAC}$ pin asynchronously updates the DAC register with the contents of the input register.

If $\overline{CS}$/LD is high, a low on the $\overline{LDAC}$ pin causes the DAC register to be updated with the contents of the input register.

If $\overline{CS}$/LD is low, a low going pulse on the $\overline{LDAC}$ pin before the rising edge of $\overline{CS}$/LD powers up the DAC but does not cause the output to be updated. If $\overline{LDAC}$ remains low after the rising edge of $\overline{CS}$/LD, then $\overline{LDAC}$ is recognized, the command specified in the 24-bit word just transferred is executed and the DAC output is updated.

OPERATION

The DAC is powered up when $\overline{LDAC}$ is taken low, independent of the state of $\overline{CS}$/LD.

If $\overline{LDAC}$ is low at the time $\overline{CS}$/LD goes high, it inhibits any software power-down command that was specified in the input word.

Voltage Outputs

The rail-to-rail amplifier contained in these parts has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifier's DC output impedance is 0.05Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 25Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 25Ω • 1mA = 25mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation of these devices is achieved in part by keeping "signal" and "power" grounds separated internally and by reducing shared internal resistance.

The GND pin functions both as the node to which the reference and output voltages are referred and as a return path for power currents in the device. Because of this, careful thought should be given to the grounding scheme and board layout in order to ensure rated performance.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin of the part should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.05Ω). Note that the LTC2601/LTC2611/LTC2621 are no more susceptible to these effects than other parts of their type; on the contrary, they allow layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the device cannot go below ground, it may limit for the lowest codes as shown in Figure 3b. Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

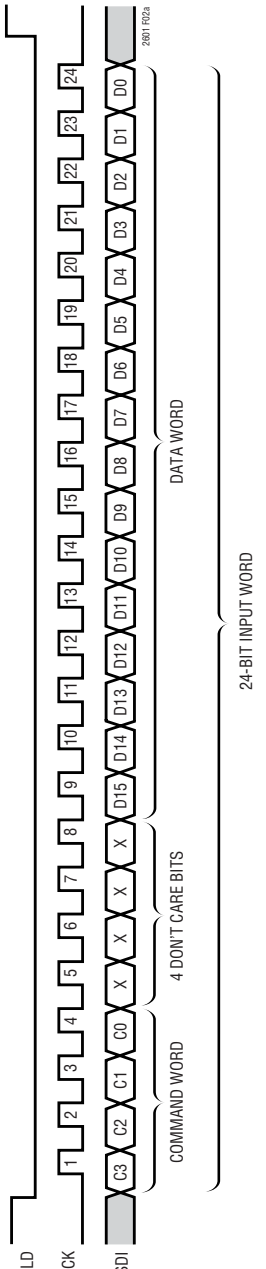


Figure 2a. LTC2601 24-Bit Load Sequence (Minimum Input Word). LTC2611 SDI Data Word: 14-Bit Input Code + 2 Don't-Care Bits; LTC2621 SDI Data Word: 12-Bit Input Code + 4 Don't-Care Bits

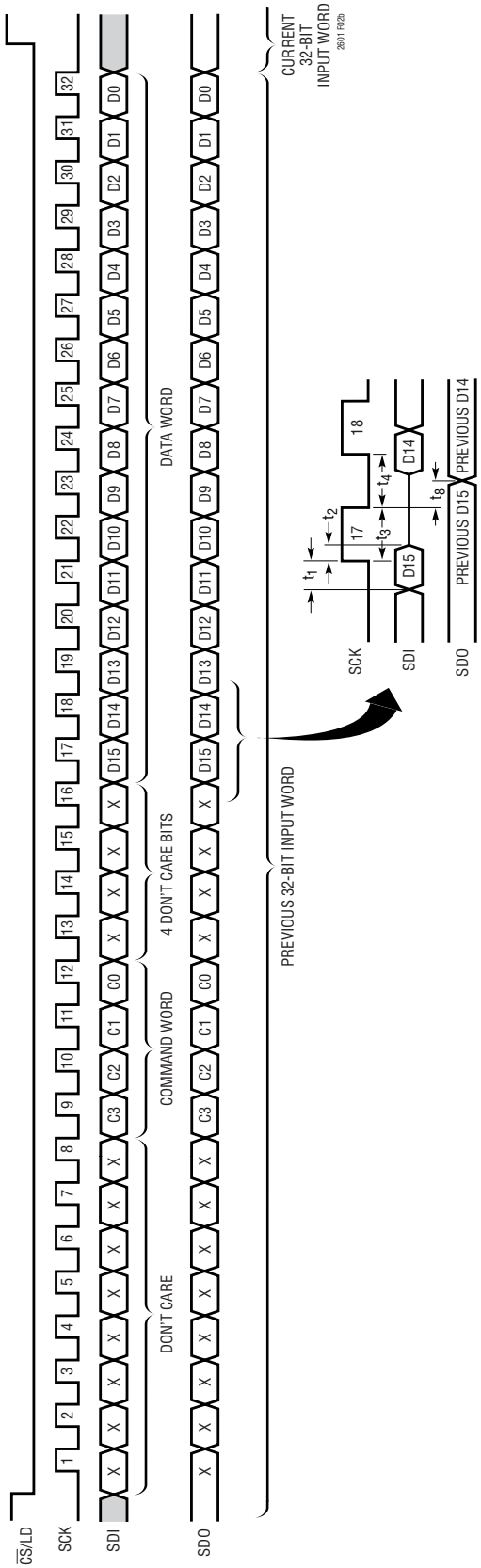


Figure 2b. LTC2601 32-Bit Load Sequence (Required for Daisy-Chain Operation). LTC2611 SDI/SDO Data Word: 14-Bit Input Code + 2 Don't-Care Bits; LTC2621 SDI/SDO Data Word: 12-Bit Input Code + 4 Don't-Care Bits

OPERATION

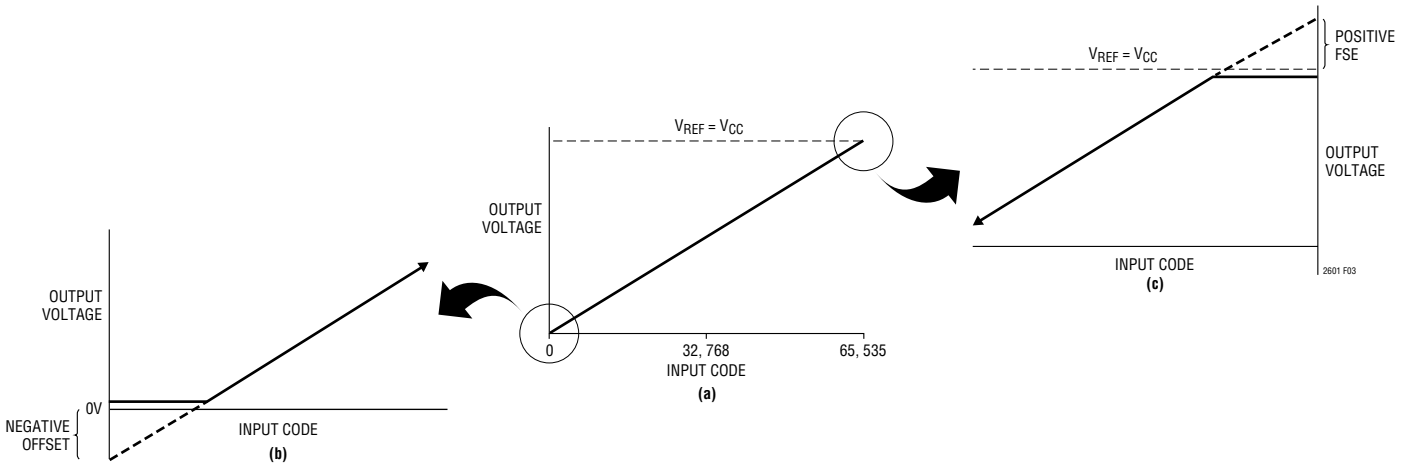
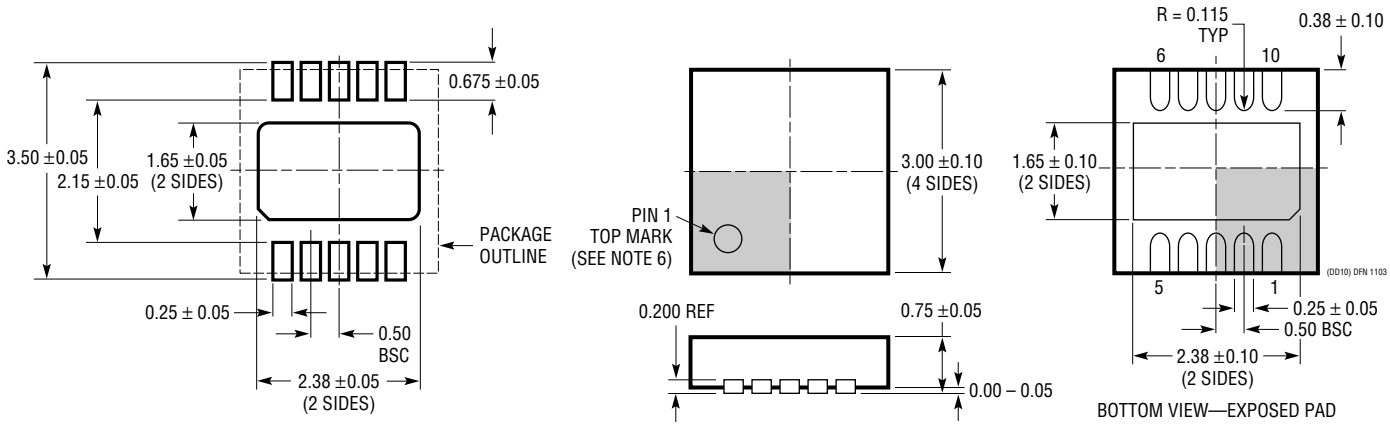


Figure 3. Effects of Rail-to-Rail Operation On the DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



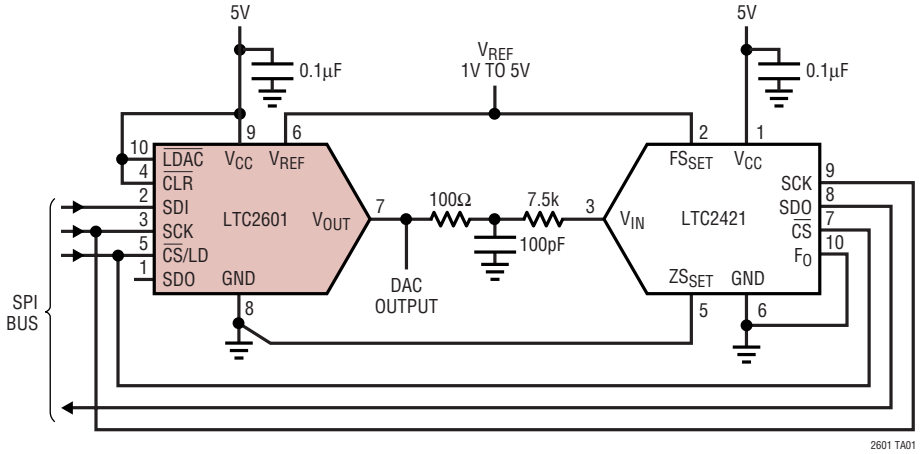
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Demo Circuit DC777 Schematic. Onboard 20-Bit ADC Measures Key Performance Parameters



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5µs/750µA, 8µs/450µA
LTC1655/LTC1655L	Single 16-Bit V_{OUT} DACs with Serial Interface in SO-8	V_{CC} = 5V(3V), Low Power, Deglitched
LTC1657/LTC1657L	Parrallel 5V/3V 16-Bit V_{OUT} DACs	Low Power, Deglitched, Rail-to-Rail V_{OUT}
LTC1660/LTC1665	Octal 10/8-Bit V_{OUT} DACs in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1661	Dual 10-Bit V_{OUT} DAC 8-Lead MSOP	Micropower Rail-to-Rail Output, 3-Wire Interface
LTC1662	Dual 10-Bit V_{OUT} DAC 8-Lead MSOP	Ultralow Power, Rail-to-Rail Output
LTC1663	Single 10-Bit V_{OUT} DAC in SOT-23	SMBus Interface, Pin-for-Pin Compatible with LTC1669
LTC1664	Quad 10-Bit V_{OUT} DAC 16-Lead SSOP	Micropower Rail-to-Rail Output, 3-Wire Interface
LTC1669	Single 10-Bit VOUT DAC 5-Lead SOT-23	Pin-for-Pin Compatible with LTC1663
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2µs for 10V Step
LTC2600/LTC2610 LTC2620	Octal 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output
LTC2602/LTC2612 LTC2622	Dual 16-/14-/12-Bit V_{OUT} DACs in 8-Lead MSOP	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output
LTC2604/LTC2614 LTC2624	Quad 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2605/LTC2615 LTC2625	Octal 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	250µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, I^2C Interface
LTC2606/LTC2616 LTC2626	16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	270µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, I^2C Interface
LTC2607/LTC2617 LTC2627	Dual 16-/14-/12-Bit V_{OUT} DACs in 12-Lead DFN with I^2C Interface	260µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, I^2C Interface
LTC2609/LTC2619 LTC2629	Quad 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	250µA Range per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output with Separate V_{REF} Pins for Each DAC

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