

## IRS2117/IRS2118(S)PbF

### SINGLE CHANNEL DRIVER

#### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input (IRS2117) or out of phase with input (IRS2118)
- RoHS compliant

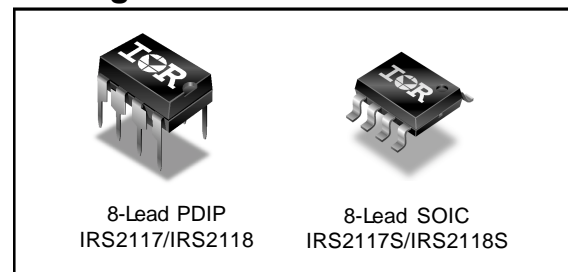
#### Product Summary

|                            |                 |
|----------------------------|-----------------|
| $V_{\text{OFFSET}}$        | 600 V max.      |
| $I_{\text{O}+/-}$          | 200 mA / 420 mA |
| $V_{\text{OUT}}$           | 10 V - 20 V     |
| $t_{\text{on/off}}$ (typ.) | 125 ns & 105 ns |

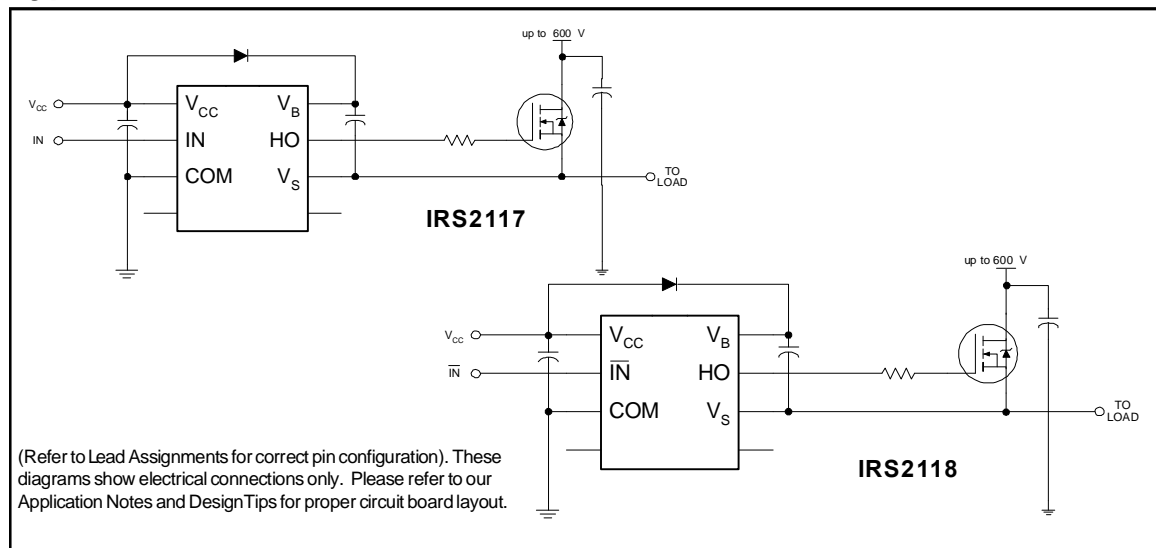
#### Description

The IRS2117/IRS2118 are a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side or low-side configuration which operates up to 600 V.

#### Packages



#### Typical Connection



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figs. 5 through 8.

| Symbol              | Definition  | Min.                 | Max.                  | Units |      |
|---------------------|---|----------------------|-----------------------|-------|------|
| V <sub>B</sub>      | High-side floating supply voltage                   | -0.3                 | 625                   | V     |      |
| V <sub>S</sub>      | High-side floating supply offset voltage            | V <sub>B</sub> - 25  | V <sub>B</sub> + 0.3  |       |      |
| V <sub>HO</sub>     | High-side floating output voltage                   | V <sub>S</sub> - 0.3 | V <sub>B</sub> + 0.3  |       |      |
| V <sub>CC</sub>     | Logic supply voltage                                | -0.3                 | 25                    |       |      |
| V <sub>IN</sub>     | Logic input voltage                                 | -0.3                 | V <sub>CC</sub> + 0.3 |       |      |
| dV <sub>S</sub> /dt | Allowable offset supply voltage transient (Fig. 2)  | —                    | 50                    | V/ns  |      |
| P <sub>D</sub>      | Package power dissipation @ T <sub>A</sub> ≤ +25 °C | (8 lead PDIP)        | —                     | 1.0   | W    |
|                     |   | (8 lead SOIC)        | —                     | 0.625 |      |
| R <sub>thJA</sub>   | Thermal resistance, junction to ambient             | (8 lead PDIP)        | —                     | 125   | °C/W |
|                     |   | (8 lead SOIC)        | —                     | 200   |      |
| T <sub>J</sub>      | Junction temperature                                | —                    | 150                   | °C    |      |
| T <sub>S</sub>      | Storage temperature                                 | -55                  | 150                   |       |      |
| T <sub>L</sub>      | Lead temperature (soldering, 10 seconds)            | —                    | 300                   |       |      |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15 V differential.

| Symbol          | Definition                                 | Min.                | Max.                | Units |
|-----------------|--|---------------------|---------------------|-------|
| V <sub>B</sub>  | High-side floating supply absolute voltage | V <sub>S</sub> + 10 | V <sub>S</sub> + 20 | V     |
| V <sub>S</sub>  | High-side floating supply offset voltage   | Note 1              | 600                 |       |
| V <sub>HO</sub> | High-side floating output voltage          | V <sub>S</sub>      | V <sub>B</sub>      |       |
| V <sub>CC</sub> | Logic supply voltage                       | 10                  | 20                  |       |
| V <sub>IN</sub> | Logic input voltage                        | 0                   | V <sub>CC</sub>     |       |
| T <sub>A</sub>  | Ambient temperature                        | -40                 | 125                 | °C    |

Note 1: Logic operational for V<sub>S</sub> of -5 V to +600 V. Logic state held for V<sub>S</sub> of -5 V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $C_L$  = 1000 pF and  $T_A$  = 25 °C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

| Symbol    | Definition                 | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|----------------------------|------|------|------|-------|-----------------|
| $t_{on}$  | Turn-on propagation delay  | —    | 125  | 200  | ns    | $V_S = 0$ V     |
| $t_{off}$ | Turn-off propagation delay | —    | 105  | 180  |       | $V_S = 600$ V   |
| $t_r$     | Turn-on rise time          | —    | 75   | 130  |       |                 |
| $t_f$     | Turn-off fall time         | —    | 35   | 65   |       |                 |

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V and  $T_A$  = 25 °C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol      | Definition  | Min.                        | Typ. | Max. | Units             | Test Conditions  |
|-------------|---|-----------------------------|------|------|-------------------|--|
| $V_{IH}$    | Input voltage - logic "1" (IRS2117) logic "0" (IRS2118) | 9.5                         | —    | —    | V                 | $I_O = 2$ mA   |
| $V_{IL}$    | Input voltage - logic "0" (IRS2117) logic "1" (IRS2118) | —                           | —    | 6.0  |                   |  |
| $V_{OH}$    | High level output voltage, $V_{BIAS} - V_O$             | —                           | 0.05 | 0.2  |                   |  |
| $V_{OL}$    | Low level output voltage, $V_O$                         | —                           | 0.02 | 0.1  |                   |  |
| $I_{LK}$    | Offset supply leakage current                           | —                           | —    | 50   | $\mu$ A           | $V_B = V_S = 600$ V  |
| $I_{QBS}$   | Quiescent $V_{BS}$ supply current                       | —                           | 50   | 240  |                   | $V_{IN} = 0$ V or $V_{CC}$                                   |
| $I_{QCC}$   | Quiescent $V_{CC}$ Supply Current                       | —                           | 70   | 340  |                   | $V_{IN} = V_{CC}$  |
| $I_{IN+}$   | Logic "1" input bias current                            | (IRS2117)<br>—<br>(IRS2118) | 20   | 40   |                   | $V_{IN} = 0$ V   |
| $I_{IN-}$   | Logic "0" input bias current                            | (IRS2117)<br>—<br>(IRS2118) | —    | 5.0  | $V_{IN} = V_{CC}$ |  |
| $V_{BSUV+}$ | $V_{BS}$ supply undervoltage positive going threshold   | 7.6                         | 8.6  | 9.6  | V                 |  |
| $V_{BSUV-}$ | $V_{BS}$ supply undervoltage negative going threshold   | 7.2                         | 8.2  | 9.2  |                   |  |
| $V_{CCUV+}$ | $V_{CC}$ supply undervoltage positive going threshold   | 7.6                         | 8.6  | 9.6  |                   |  |
| $V_{CCUV-}$ | $V_{CC}$ supply undervoltage negative going threshold   | 7.2                         | 8.2  | 9.2  |                   |  |
| $I_{O+}$    | Output high short circuit pulsed current                | 200                         | 290  | —    | mA                | $V_O = 0$ V<br>$V_{IN} =$ Logic "1"<br>$PW \leq 10$ $\mu$ s  |
| $I_{O-}$    | Output low short circuit pulsed current                 | 420                         | 600  | —    |                   | $V_O = 15$ V<br>$V_{IN} =$ Logic "0"<br>$PW \leq 10$ $\mu$ s |

## Functional Block Diagram (IRS2117)



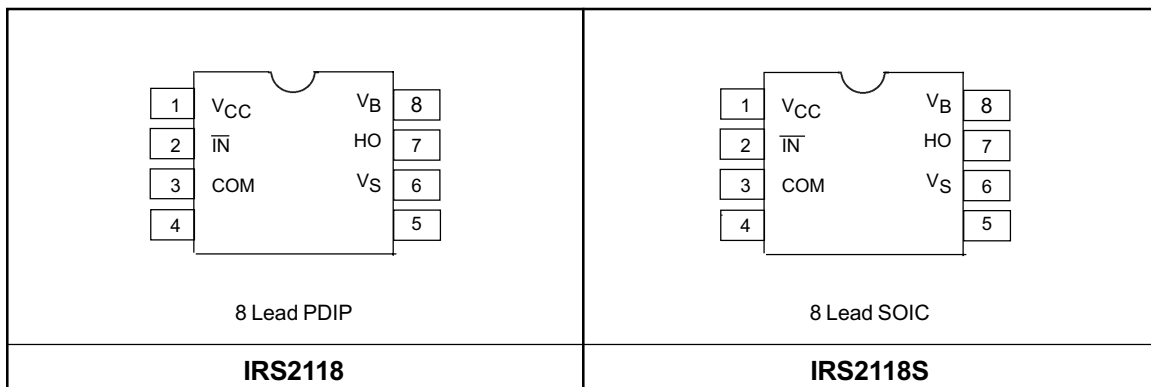
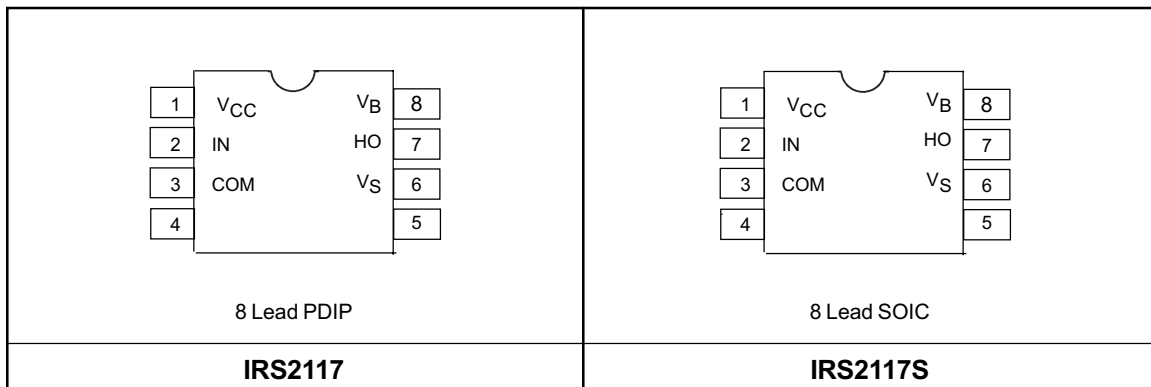
## Functional Block Diagram (IRS2118)



## Lead Definitions

| Symbol                 | Description   |
|------------------------|---|
| V <sub>CC</sub>        | Logic and gate drive supply   |
| IN                     | Logic input for gate driver output (HO), in phase with HO (IRS2117)     |
| $\overline{\text{IN}}$ | Logic input for gate driver output (HO), out of phase with HO (IRS2118) |
| COM                    | Logic ground  |
| V <sub>B</sub>         | High-side floating supply   |
| HO                     | High-side gate drive output   |
| V <sub>S</sub>         | High-side floating supply return  |

## Lead Assignments



# IRS2117/IRS2118(S)PbF

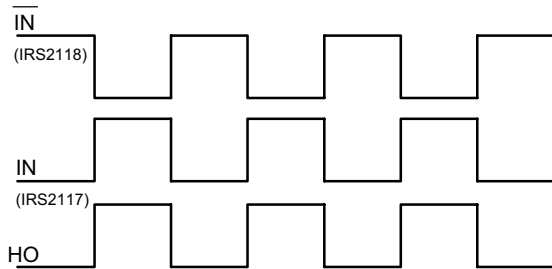


Figure 1. Input/Output Timing Diagram

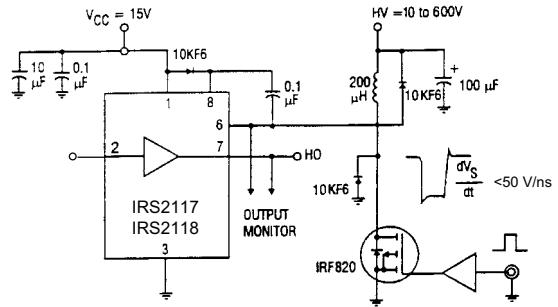


Figure 2. Floating Supply Voltage Transient Test Circuit

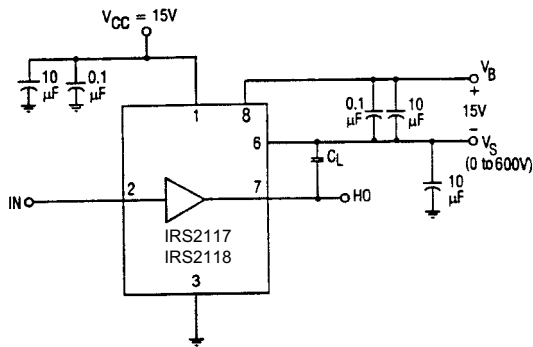


Figure 3. Switching Time Test Circuit

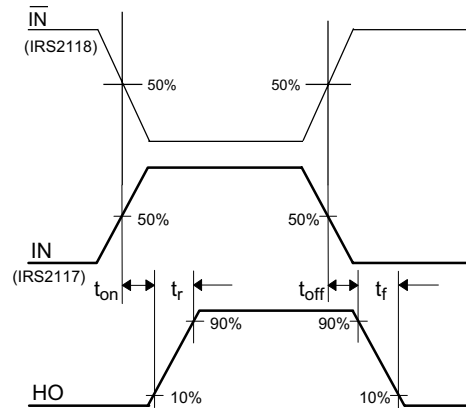
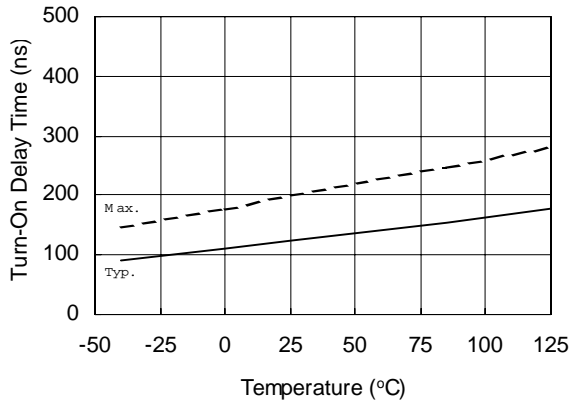
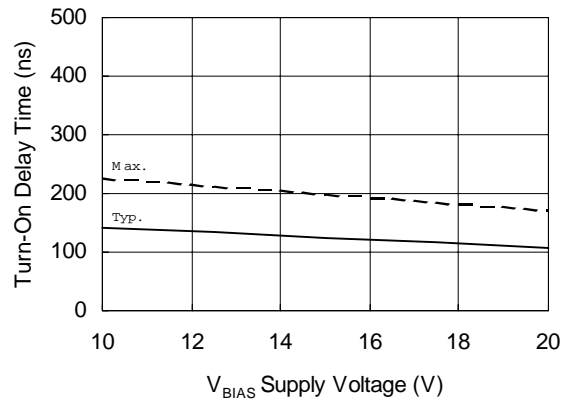


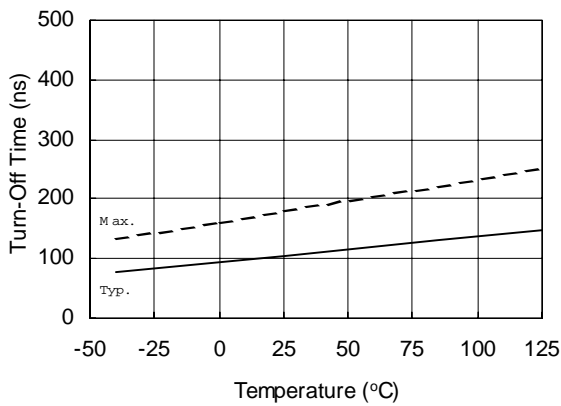
Figure 4. Switching Time Waveform Definition



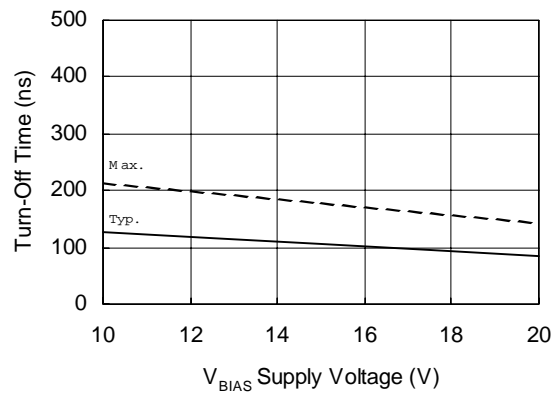
**Figure 5A. Turn-On Time vs. Temperature**



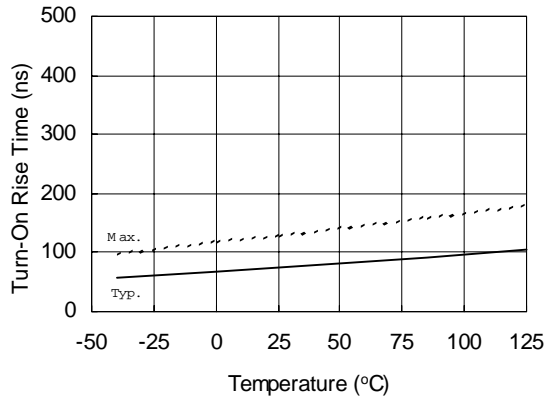
**Figure 5B. Turn-On Time vs. Supply Voltage**



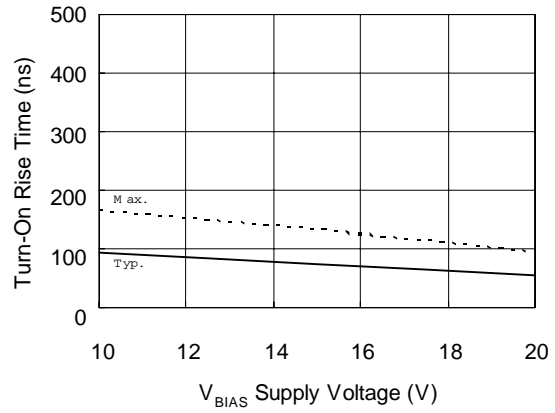
**Figure 6A. Turn-Off Time vs. Temperature**



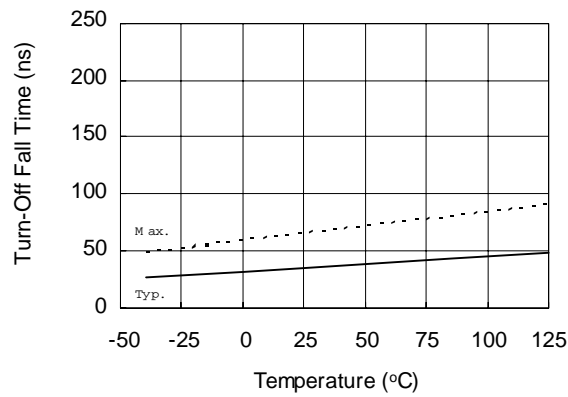
**Figure 6B. Turn-Off Time vs. Supply Voltage**



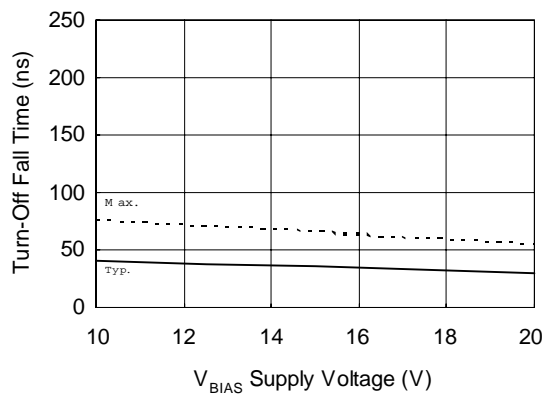
**Figure 7A. Turn-On Rise Time vs. Temperature**



**Figure 7B. Turn-On Rise Time vs. Supply Voltage**

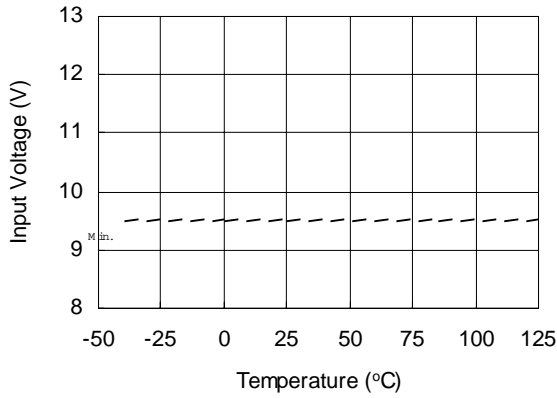


**Figure 8A. Turn-Off Fall Time vs. Temperature**

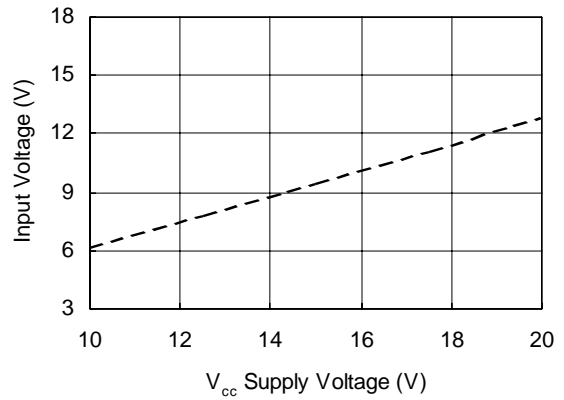


**Figure 8B. Turn-Off Fall Time vs. Supply Voltage**

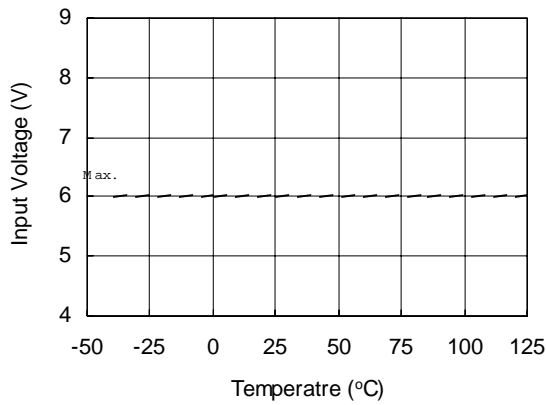




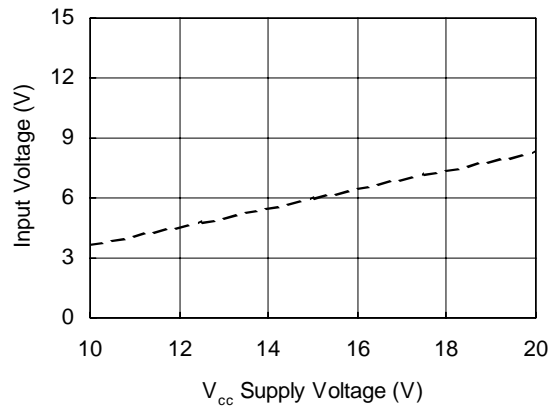
**Figure 9A. Logic "1" (IRS2118 "0") Input Voltage vs. Temperature**



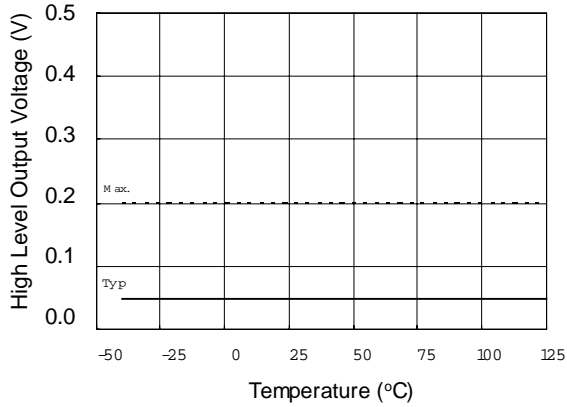
**Figure 9B. Logic "1" (IRS2118 "0") Input Voltage vs. Supply Voltage**



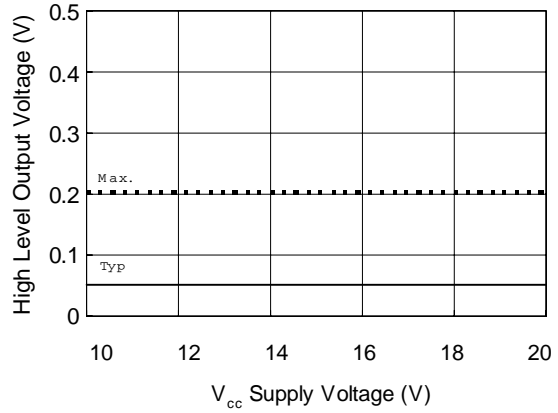
**Figure 10A. Logic "0" (IRS2118 "1") Input Voltage vs. Temperature**



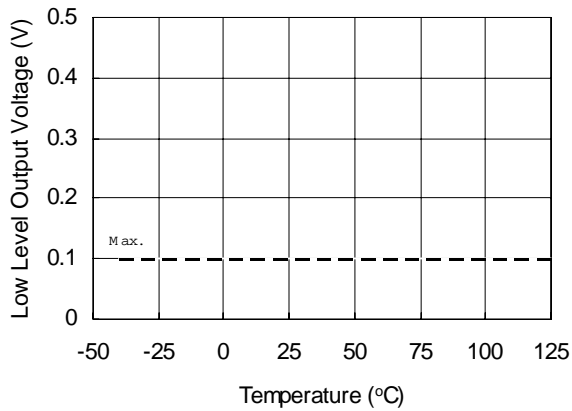
**Figure 10B. Logic "0" (IRS2118 "1") Input Voltage vs. Supply Voltage**



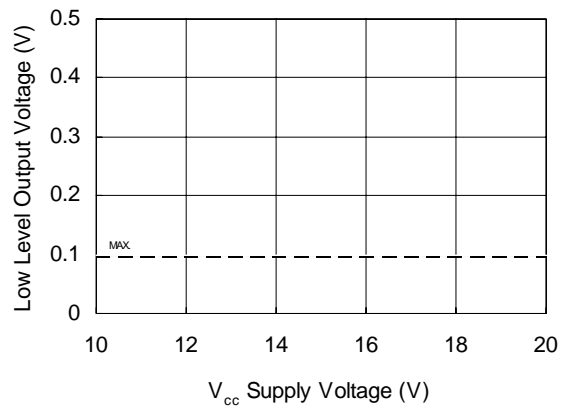
**Figure 11A. High Level Output vs. Temperature ( $I_o = 2\text{ mA}$ )**



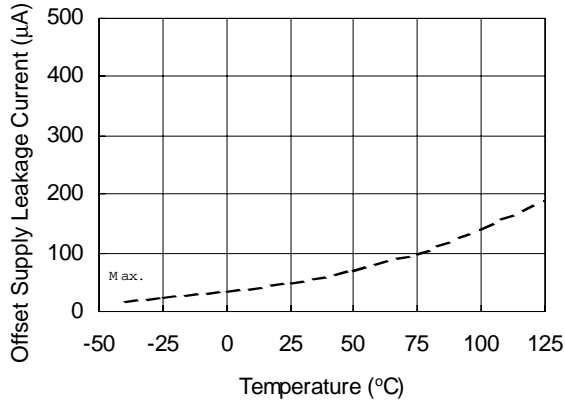
**Figure 11B. High Level Output vs. Supply Voltage ( $I_o = 2\text{ mA}$ )**



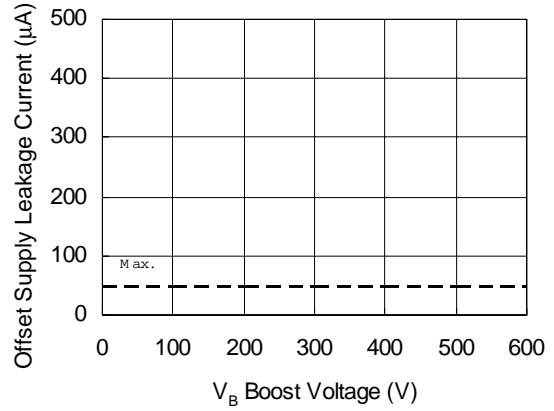
**Figure 12A. Low Level Output vs. Temperature**



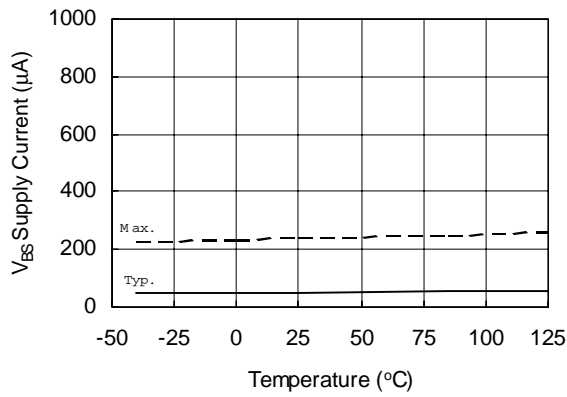
**Figure 12B. Low Level Output vs. Supply Voltage**



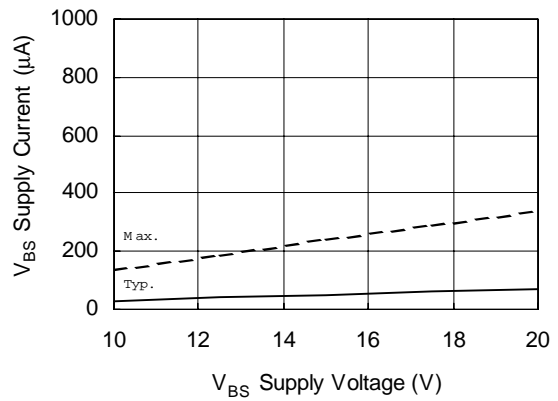
**Figure 13A. Offset Supply Leakage Current vs. Temperature**



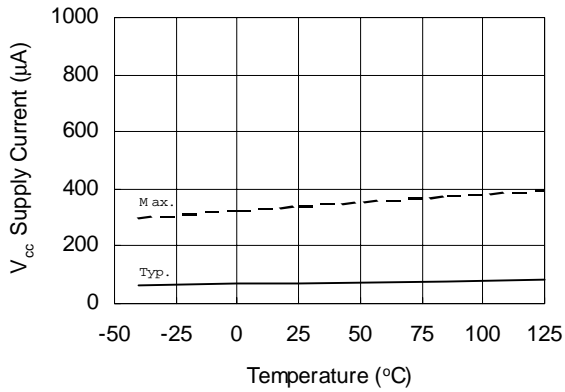
**Figure 13B. Offset Supply Leakage Current vs. V<sub>B</sub> Boost Voltage**



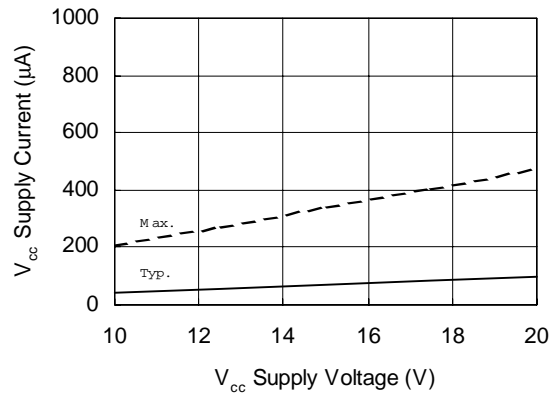
**Figure 14A. V<sub>BS</sub> Supply Current vs. Temperature**



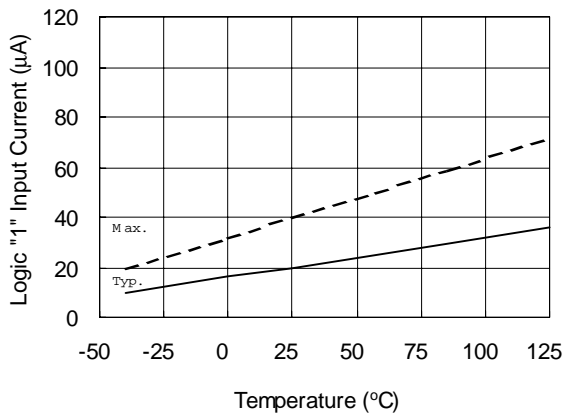
**Figure 14B. V<sub>BS</sub> Supply Current vs. Supply Voltage**



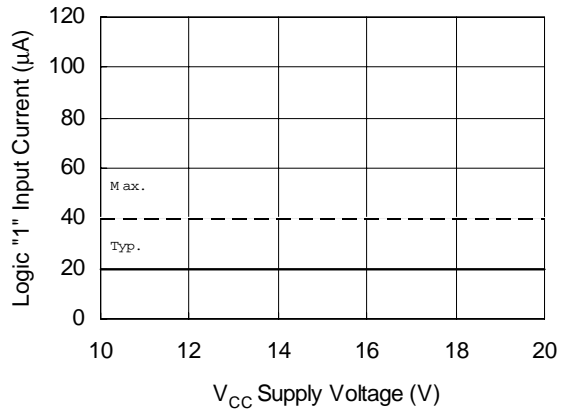
**Figure 15A. V<sub>CC</sub> Supply Current vs. Temperature**



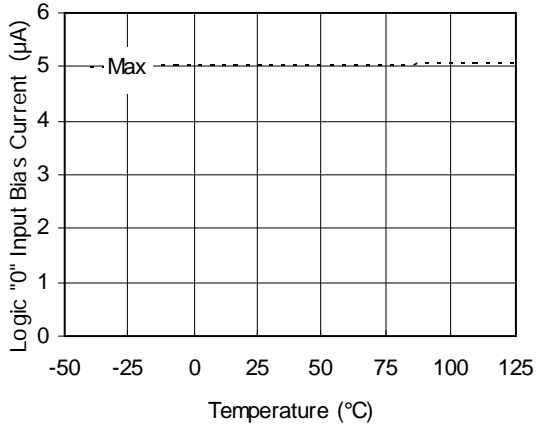
**Figure 15B. V<sub>CC</sub> Supply Current vs. Supply Voltage**



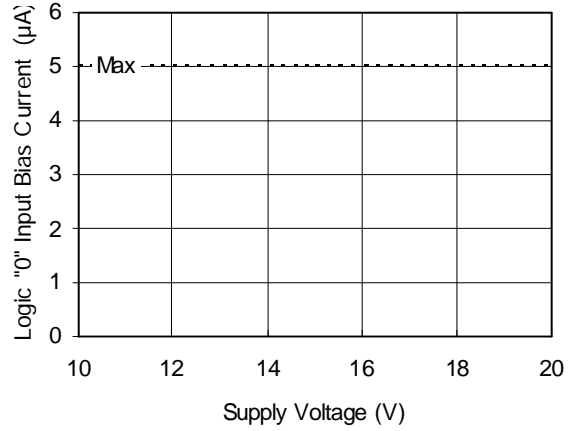
**Figure 16A. Logic "1" (IRS2118 Logic "0") Input Current vs. Temperature**



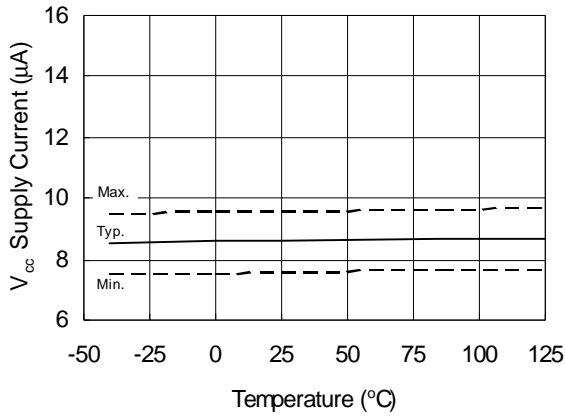
**Figure 16B. Logic "1" (IRS2118 Logic "0") Input Current vs. Supply Voltage**



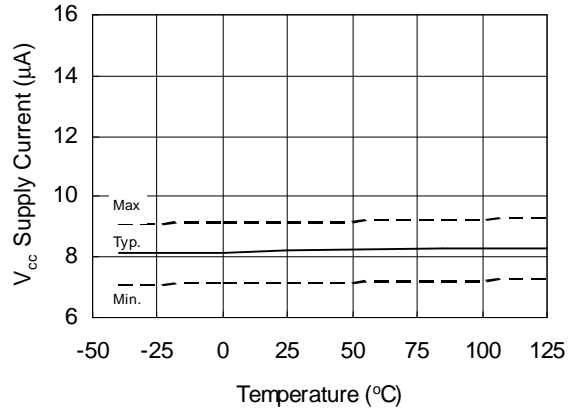
**Figure 17A. Logic "0" Input Bias Current vs. Temperature**



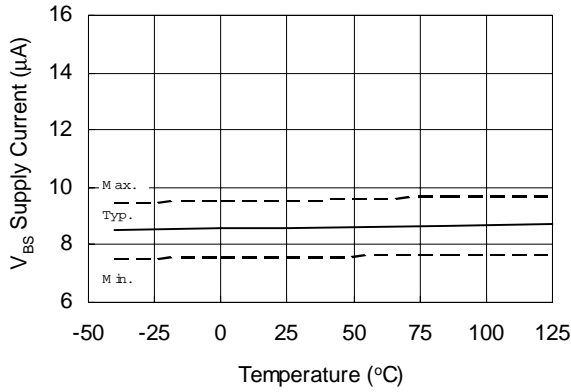
**Figure 17B. Logic "0" Input Bias Current vs. Voltage**



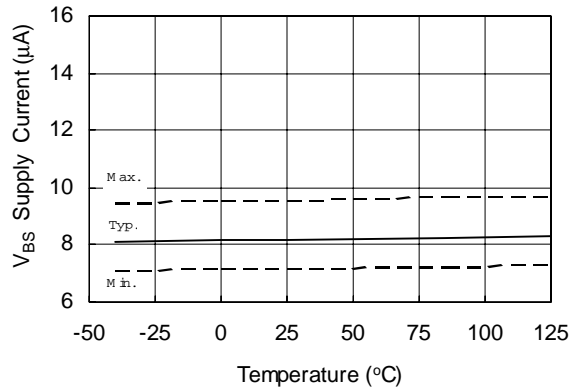
**Figure 18. V<sub>cc</sub> Undervoltage Threshold (+) vs. Temperature**



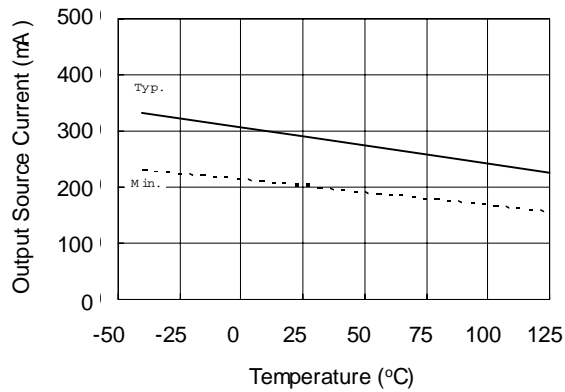
**Figure 19. V<sub>cc</sub> Undervoltage Threshold (-) vs. Temperature**



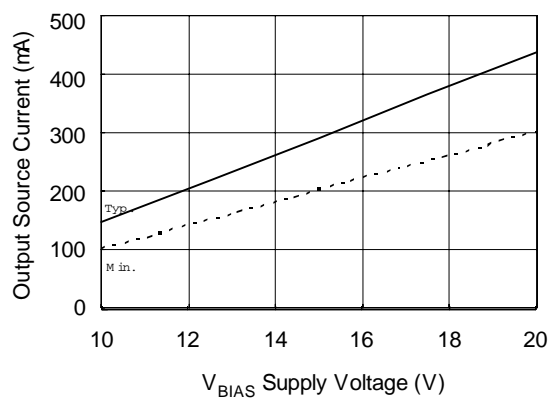
**Figure 20.  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**



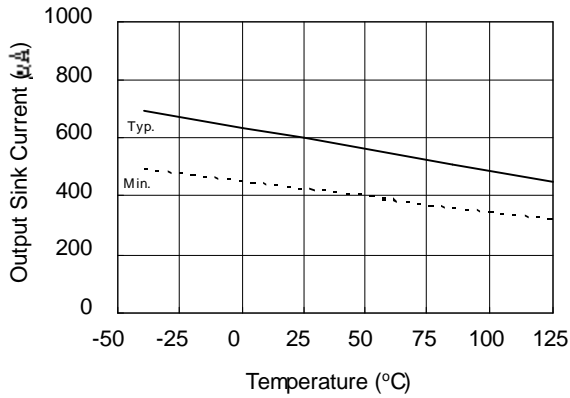
**Figure 21.  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature**



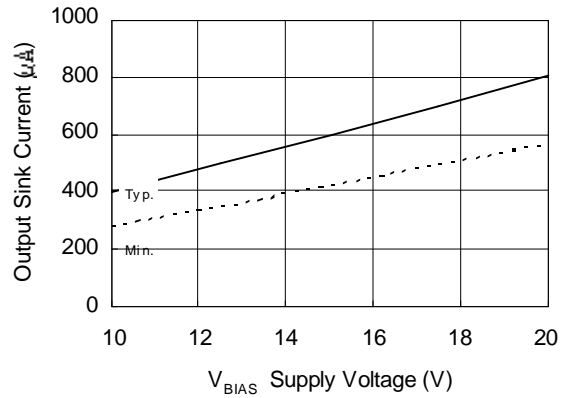
**Figure 22A. Output Source Current vs. Temperature**



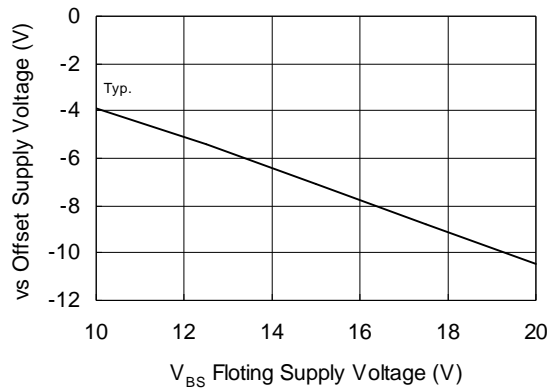
**Figure 22B. Output Source Current vs. Supply Voltage**



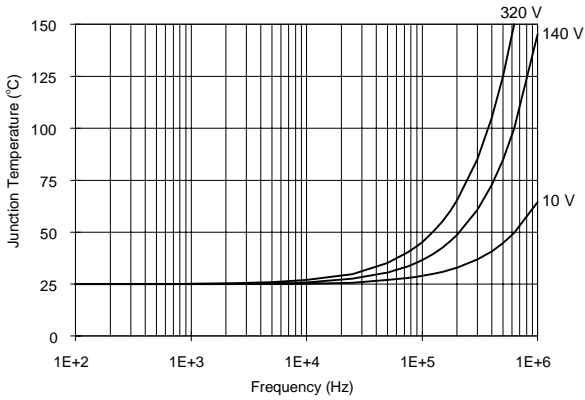
**Figure 23A. Output Sink Current vs. Temperature**



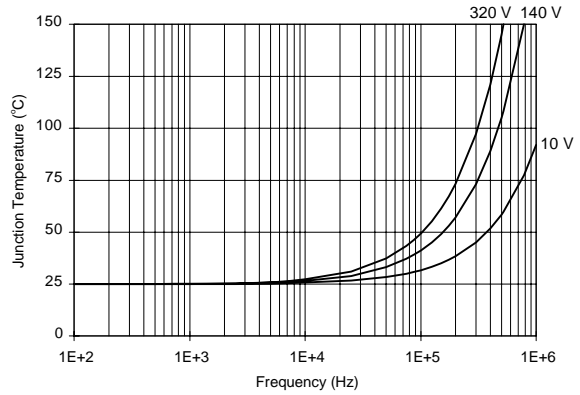
**Figure 23B. Output Sink Current vs. Supply Voltage**



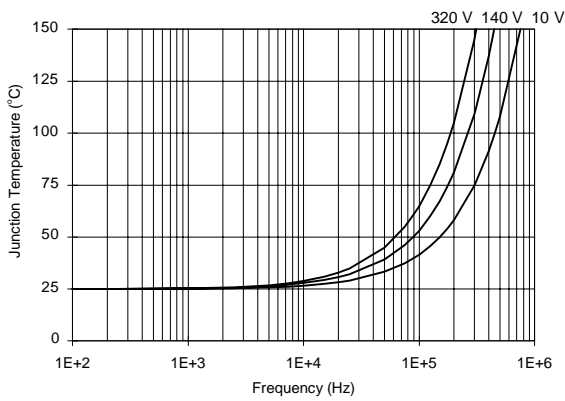
**Figure 24. Maximum VS Negative Offset vs. Supply Voltage**



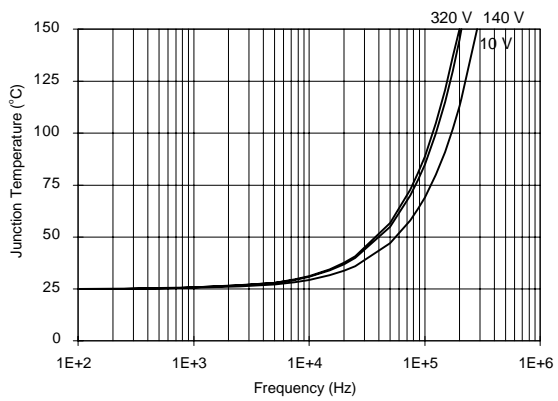
**Figure 24. IRS2117/IRS2118 T<sub>J</sub> vs. Frequency (IRFBC20)**  
**R<sub>GATE</sub> = 33 Ω, V<sub>CC</sub> = 15 V**



**Figure 25. IRS2117/IRS2118 T<sub>J</sub> vs. Frequency (IRFBC30)**  
**R<sub>GATE</sub> = 22 Ω, V<sub>CC</sub> = 15 V**



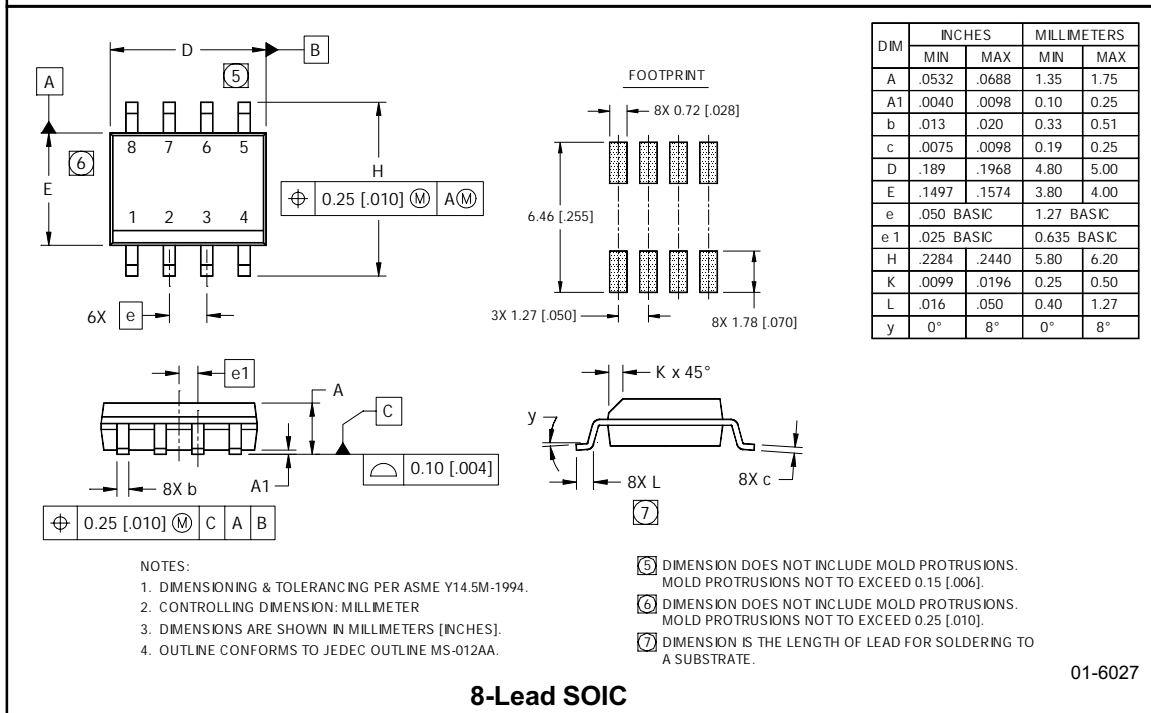
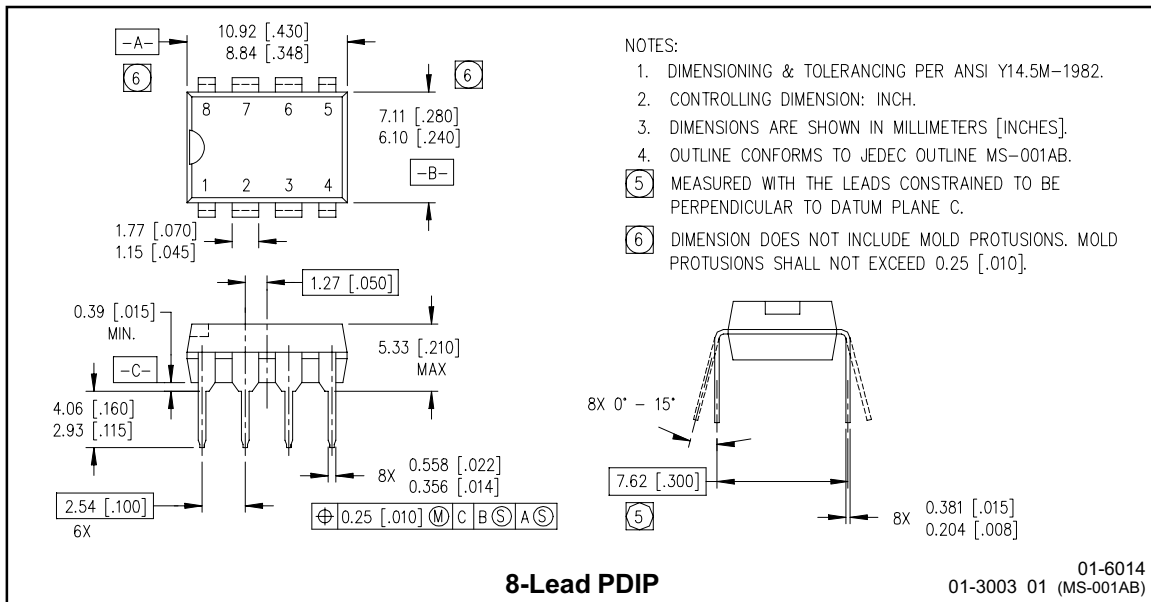
**Figure 26. IRS2117/IRS2118 T<sub>J</sub> vs. Frequency (IRFBC40)**  
**R<sub>GATE</sub> = 15 Ω, V<sub>CC</sub> = 15 V**



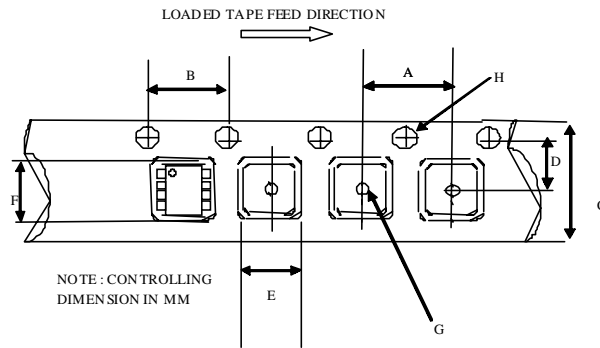
**Figure 27. IRS2117/IRS2118 T<sub>J</sub> vs. Frequency (IRFPE50)**  
**R<sub>GATE</sub> = 10 Ω, V<sub>CC</sub> = 15 V**



## Case outlines

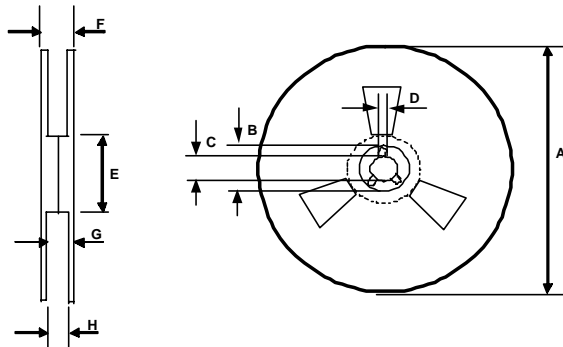


**Tape & Reel  
8-Lead SOIC**



CARRIER TAPE DIMENSION FOR 8SOICN

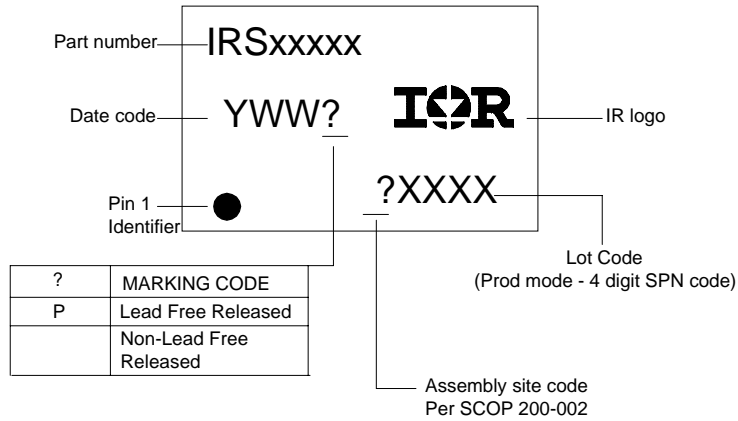
| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 7.90   | 8.10  | 0.311    | 0.318 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 11.70  | 12.30 | 0.46     | 0.484 |
| D    | 5.45   | 5.55  | 0.214    | 0.218 |
| E    | 6.30   | 6.50  | 0.248    | 0.255 |
| F    | 5.10   | 5.30  | 0.200    | 0.208 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |



REEL DIMENSIONS FOR 8SOICN

| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 18.40  | n/a      | 0.724  |
| G    | 14.50  | 17.10  | 0.570    | 0.673  |
| H    | 12.40  | 14.40  | 0.488    | 0.566  |

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

- 8-LeadPDIP IRS2117PbF
- 8-LeadPDIP IRS2118PbF
- 8-LeadSOIC IRS2117SPbF
- 8-LeadSOIC IRS2118SPbF
- 8-Lead SOIC Tape & Reel IRS2117STRPbF
- 8-Lead SOIC Tape & Reel IRS2118STRPbF