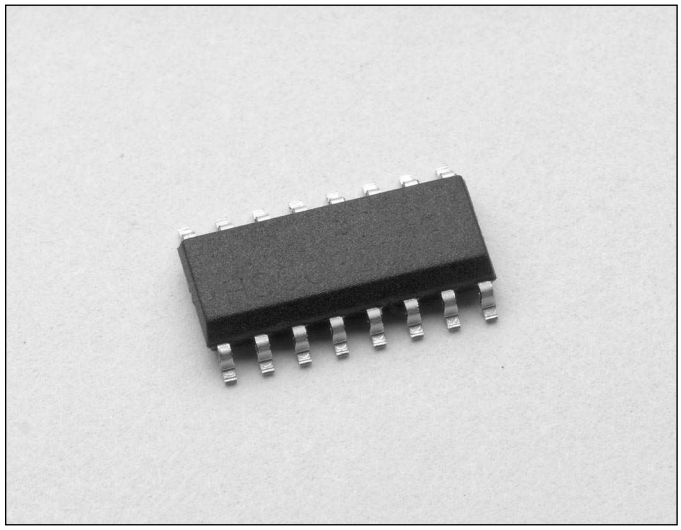
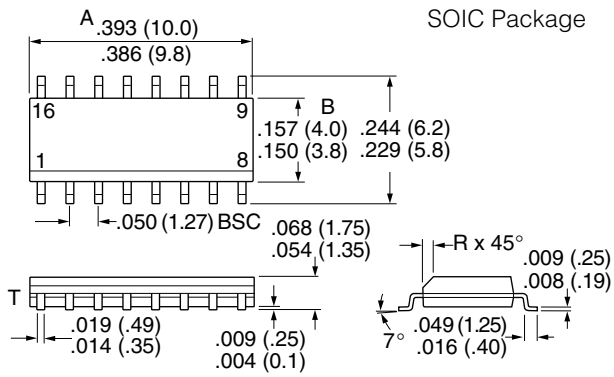


Dimensions in inches (mm)



Notes:
1. Dimensions A and B are datums and T is a datum surface.
2. Dimensioning and tolerancing per ansi Y14.5M, 1982
3. Controlling dimension: millimeter.
4. Dimension A and B do not include mold protrusion.
5. Maximum mold protrusion 0.15 (0.005) per side.

Figure 1. IRM7001 pin out

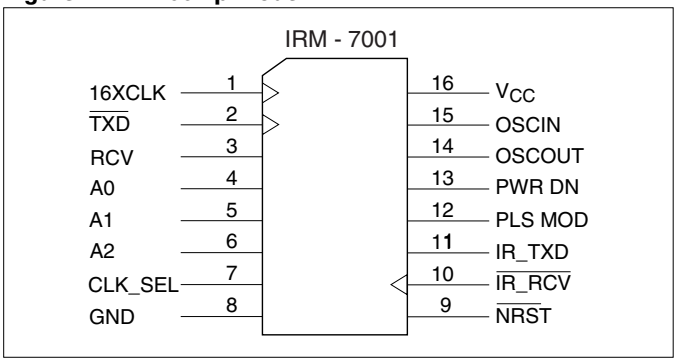
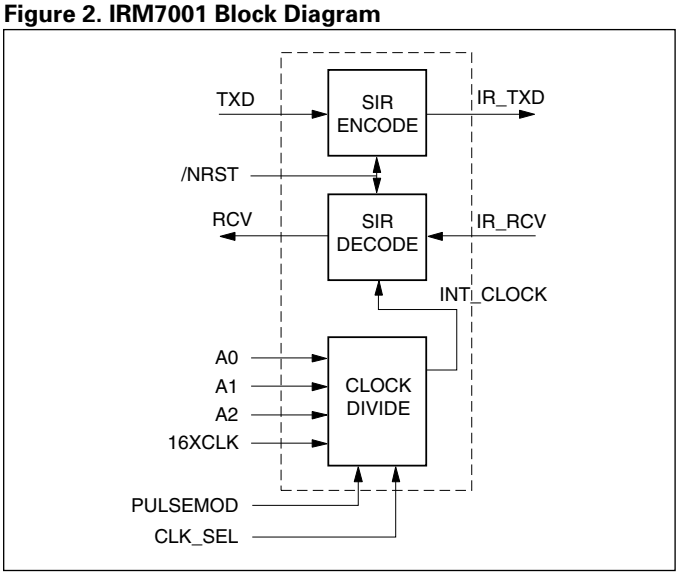


Figure 2. IRM7001 Block Diagram



FEATURES

- **Compliant with IrDA 1.0 Physical Layer Specifications**
- **Interfaces with IrDA 1.0 Compliant IR Transceivers**
- **Used in conjunction with Standard 16550 UART**
- **Transmits/Receives either 1.6µs or 3/16 Pulse Mode**
- **Internal or External Clock Mode**
- **Programmable Baud Rate**
- **2.7–5.5 V Operation**
- **16 Pin SOIC Package**

APPLICATIONS

- **Interfaces with IR Transceivers in:**
  - **Computer Applications:**
    PDAs
    Dongle or other RS232 Adapter
  - **Telecom Application:**
    Modems
    Fax Machines
    Pagers
  - **Handheld Data Collection:**
    Industrial
    Medical
    Transportation

DESCRIPTION

The IRM7001 SIR-Encoder/Decoder is a CMOS modulator/demodulator chip that is used to both encode and decode information as per the IrDA® SIR (Serial InfraRed) signal modulation and demodulation scheme. This chip is designed to work with Infineon IrDA compatible transceivers and all other IrDA compatible transceivers. The chip contains a clock divider circuit used to generate the 16X clock internally. This makes it very suitable for microcontroller-based embedded system design.

Figure 3. IRM7001 Usage Scenario (with Internal Clock)

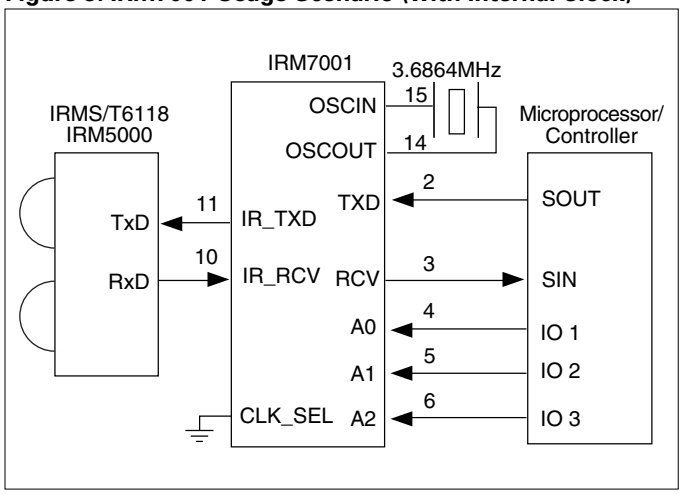


Figure 4. IRM7001 Usage Scenario (with External Clock)

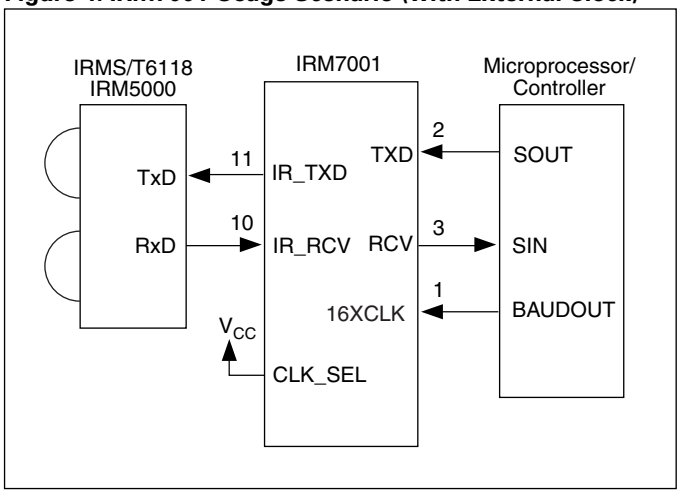
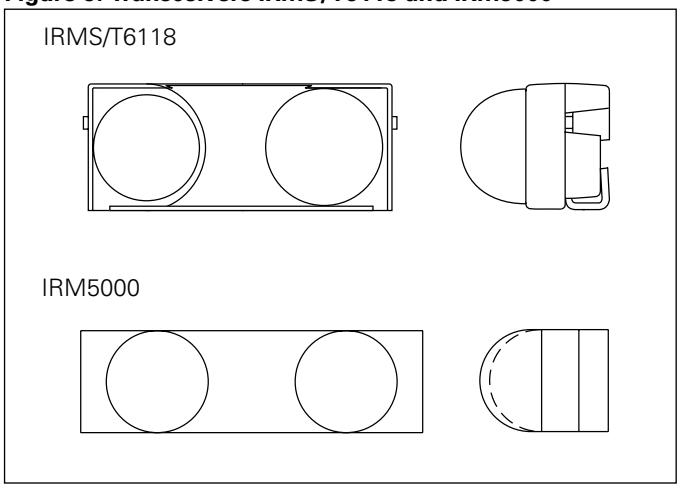


Table 1. Selection of Internal Clock Rate from Crystal Oscillator

Selected Clock Rate (bps)	A2	A1	A0	CRYSTAL FREQ. DIVISION
115200	0	0	0	Divided by 2
57600	0	0	1	Divided by 4
19200	0	1	0	Divided by 12
9600	0	1	1	Divided by 24
38400	1	0	0	Divided by 6
4800	1	0	1	Divided by 48
2400	1	1	0	Divided by 96
TEST PURPOSE	1	1	1	No Division

0=L, 1=H

Figure 5. Transceivers IRMS/T6118 and IRM5000



IRM7001 SIR Modulator/Demodulator functions extremely well with Infineon IRMS6118/IRMT6118 and IRM5000 SIR (115 Kb/s) Infrared Data transceivers. These products provide the user with a low component count and cost effective way of implementing an IrDA port on their products where the microcontroller does not have a built-in IrDA port support

Figures 12, 13, and 14 show the schematic, PCB front side and back side for an IRM5000/7001 based port. Table 7 provides the Bill of Materials list to implement the port. Figures 15, 16, and 17 show the schematic, PCB front and the back side for an IRMS6118/IRM7001 based port. Table 8 provides the Bill of Materials list to implement the port.

Table 2. Pin Out and Signal Description

Signal	Pin	Type	Description
16X CLK	1	DIGIN	Positive edge triggered input clock signal that is set to 16 times the data transmission baudrate. This clock is used to drive the Encoder/Decoder state machine. Depending on the application, the 16XCLK can be provided by the application circuitry, or the internal clock divider circuitry can be used. Selection of operating mode (Internal or External clock) is selected by the CLK_SEL line. If External clock mode is selected, the application circuitry need not provide an oscillator.
TXD	2	DIGIN	Negative edge triggered input signal that is normally tied to the SOUT signal of a UART (serial data to be transmitted). Data is modulated and output as IR_TXD.
RCV	3	DIGOUT	Output signal normally tied to SIN signal of a UART (received serial data). RCV is the demodulated output of IR_RCV.
A0-A2	4-6	DIGIN	Clock multiplex signals. These signals are asserted to select the appropriate clock rate to support the following baudrate: 115200, 57600, 38400, 19200, 9600, 4800 and 2400 bps.
CLK_SEL	7	DIGIN	Active high signal, used to activate either the Internal or External clock. A high on this line activates the External clock (16XCLK), or if it is pulled low, the Internal clock is used.
GND	8		Chip ground
NRST	9	DIGIN	Active low signal used to reset the IrDA-SIR Decode state machine. Normally this line is tied to the POR (power on reset) line of the circuit or simply to Vcc. In addition to resetting the circuitry, this signal can be asserted to disable any data reception.
IR_RCV	10	DIGIN	Input is from the SIR optoelectronics. Input signal is a 3/16th pulse which is demodulated (pulse stretched) to generate the RCV (3) output signal.
IR_TXD	11	DIGOUT	This signal is the modulated TXD signal.
PULSEMOD	12	DIGIN (with pulldown)	A level high on this input puts the chip into the monoshot transmit mode. In this mode, when there is a negative transition on the TXD input, a rising edge on the internal transmit modulation state machine will activate a high pulse on IR_TXD for 6 crystal clock cycles. With a 3.6864MHz crystal, this corresponds to 1.63us. This mode cannot be used in conjunction with the 16XCLK clock. It is meant to be used with the external crystal clock. By default, this input pin is pulled to GND.
POWER-DN	13	DIGIN (with pulldown)	A high on this input puts the internal oscillator in POWERDOWN MODE. The internal oscillator normally is not powered down.
OSCOUT	14	ANAOUT	Crystal Oscillator input
OSCIN	15	ANAIN	Crystal Oscillator input
V_{CC}	16		Power (see Electrical Specifications for detail)

Function

The IRM7001 can be used in conjunction with a microcontroller/microprocessor that has a serial communication interface (UART). Prior to communication the processor selects the transmission baudrate by selecting appropriate levels on the A0-A2 lines. This process sets up the communication system to operate at the prescribed data rate. After this initial step, serial data can be transmitted or received at the prescribed data rate.

The IRM7001 consists of two state machines–the SIR Encode and SIR Decode blocks, and a sequential block Clock Divide, which synthesizes the required internal signal INT-CLOCK, based on the inputs A0-A2 and the CLK_ SEL line. The IRM7001 can be placed into Internal Clock Mode (CLK_SEL set to low) or External Clock Mode (CLK_ SEL set to high).

The internal clock signal INT_CLOCK source is then gated appropriately through to the INT_CLOCK signal. In application where the external 16XCLK signal is provided, there is no need to provide an oscillator.

The SIR Encode block is driven by TXD (negative edge triggered signal), which initiates the modulation state machine, resulting in the modulated IR_TXD signal (which drives the SIR compatible electronics).

The SIR Decode block is driven by the IR_RCV signal (negative edge triggered signal, derived from the optoelectronics). IR_RCV is demodulated by the SIR Decode block resulting in the RCV signal, which represents the *stretched* input pulse.

In addition, there is a pin provided to the user, called the PULSEMOD. A high level input on this pin activates the 1.6us mode on the IR_TXD. In this mode, whenever there is a negative edge on the TXD, the rising edge on the modulation state machine will set the IR_TXD signal high for 6 crystal clock cycles no matter what the selection on A2, A1 and A0 lines is. With a crystal frequency of 3.6864MHz, this corresponds to a high pulse of 1.63us.

ELECTRICAL SPECIFICATIONS

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	–0.5	+7.0	V
Input/Output Voltage	V_I/V_O	–0.5	V_{CC} +0.5	V
Power Dissipation	P_{max}		0.46	W
Output Current	I_O	-100	100	mA
Operating Temperature	T_A	–40	+85	°C
Storage Temperature	T_S	–65	+150	°C

Table 4. AC Characteristics V_{CC}=5 V ±10%, T_A=–20 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation Delay Time	t_{pd}	V_{CC}=5.5 V, C_L=50 pF			80	ns
Output Rise Time	t_r	V_{CC}=5.5 V, C_L=50 pF	4.0	7.0	12	ns
		V_{CC}=2.7 V, C_L=50 pF	10	16	24	ns
Output Fall Time	t_f	V_{CC}=5.5 V, C_L=50 pF	4.0	8.0	11	ns
		V_{CC}=2.7 V, C_L=50 pF	11	16	26	ns
Output Capacitance	C_{OUT}				50	pF

Operating conditions

Operating conditions are specified with respect to GND unless otherwise specified.

All the parameters below have been specified for V_{CC} in the range of 2.7 V(min) and 5.5 V(max) and for a temperature range of –20°C to 85°C.

Propagation Delay Time in the output buffer is the time taken from the input passing $V_{CC}/2$ to the time of the output reaching $V_{CC}/2$ with 50pF as the output load.

The output rise time is the time taken for the output (RCV, IRTXD) to rise from 10% to 90% of final value.
The output fall time is the time taken for the outputs (RCV, IR_TXD) to fall from 90% of original value to 10% of final value.

Table 5. Operating Conditions at V_{CC}=2.7 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	2.7	5	5.5	V	
Input voltage	V_{IN}	0		V_{CC}	V	
Ambient temperature	Ta	–20		+85	°C	
High-Level Input Voltage	V_{IH}	0.7 V_{CC}		V_{CC}	V	
Low-Level Input Voltage	V_{IL}	0		0.3 V_{CC}	V	
Output High Voltage	V_{OH}	2.2			V	I_{OH}=2.0 mA
Output Low Voltage	V_{OL}			0.5	V	I_{OL}=2.0 mA
Static Power Dissipation	P_{STAT}		0.11	0.15	mW	
Dynamic Power Dissipation	P_{DYN}		5.4	8.1	mW	
Static Current Consumption	I_{STAT}		40	54	µA	
Dynamic Power Dissipation	I_{DYN}		2	3	mA	
Max Clk Frequency(16XCLK)	f_{16xclk}			2	MHz	
Minimum Pulse Width(IR_TXD)	t_{mpw}	1630			ns	
Pulse Width on monoshot (IR_TXD)	t_{mpw}	1630	1710	1730	ns	
Output Capacitance on Output Pads used for simulation	C_{OUT}			50	pF	
Value of pulldown resistor used on POWERDN & PULSEMOD input pins	R_{DWN}	114	152	256	KOhms	
Trigger Low Level Input Voltage (For /NRST input pin)	VIL_TRIG	0.7	0.8	0.9	V	
Trigger High Level Input Voltage (For /NRST input pin)	VIH_TRIG	1.7	1.85	1.9	V	

Table 6. Operating Conditions at V_{CC}=5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	2.7	5	5.5	V	
Input voltage	V_{IN}	0		V_{CC}	V	
Ambient temperature	Ta	–20		+85	°C	
High-Level Input Voltage	V_{IH}	0.7 V_{CC}		V_{CC}	V	
Low-Level Input Voltage	V_{IL}	0		0.3 V_{CC}	V	
Output High Voltage	V_{OH}	4.5			V	I_{OH}=2.0 mA
Output Low Voltage	V_{OL}			0.5	V	I_{OL}=2.0 mA
Static Power Dissipation	P_{STAT}		0.44	0.61	mW	
Dynamic Power Dissipation	P_{DYN}		11	16.5	mW	
Static Current Consumption	I_{STAT}		80	110	µA	
Dynamic Power Dissipation	I_{DYN}		2	3	mA	
Max Clk Frequency(16XCLK)	f_{16xclk}			2	MHz	
Minimum Pulse Width(IR_TXD)	t_{mpw}	1630			ns	
Pulse Width on monoshot (IR_TXD)	t_{mpw}	1630	1710	1730	ns	
Output Capacitance on Output Pads used for simulation	C_{OUT}			50	pF	
Value of pulldown resistor used on POWERDN & PULSEMOD input pins	R_{DWN}	114	152	256	KOhms	
Trigger Low Level Input Voltage (For /NRST input pin)	VIL_TRIG	0.7	0.8	0.9	V	
Trigger High Level Input Voltage (For /NRST input pin)	VIH_TRIG	1.7	1.85	1.9	V	

IRDA Parameters

1. The Max Clk Frequency (f16xClk) represents the maximum clock frequency that the IRM7001 internal state machine should be driven at. Under normal circumstances, this clock input should not exceed 16*115200(bps) =1.8432 MHz. This is the maximum transmission rate under the IRDA Physical layer 1.0 specification. The IRM7001 can handle higher clock rates, but the recommended maximum is as specified above.
2. The Minimum Pulse Width (tmpw), represents the minimum pulse width of the encoded IR_TXD pulse as well as the minimum pulse width for the IR_RCV pulse. As per the IRDA specification, the minimum pulse width of the IR_TXD and IR_RCV pulses should be 3*(1/1.8432 MHz) = 1.63 µS. The minimum pulse width that can be handled by the IRM7001 is 250ns, which is within the IRDA SIR specifications. Under normal circumstances using a 16XCLK clock that does not exceed 2 MHz, the minimum pulse width of IR_TXD should not be shorter than 1.63 µs.

IRDA-SIR Encoding and Decoding Scheme

Overview of Encoding Scheme

Figures 5 and 6 outline the IRDA-SIR encoding scheme. The encoding scheme relies on a clock being present, which is set to 16 times the data transmission baud rate (16XCLK).

The encoder sends a pulse for every space (0) that is sent. On a high to low transition of the TXD line, the generation of the pulse is delayed for 7 clock cycles of the 16XCLK clock before the pulse is set high for 3 clock cycles (or 3/16 of a bit time) and subsequently pulled low. This in essence generates a 3/16th bit time pulse centered around the bit of information (0) that is being transmitted.

For consecutive spaces, pulses with a 1 bit time delay are generated in series. If a logic 1 (mark) is sent, then the encoder does not generate a pulse.

Figure 6. Encoding Scheme—Macro Perspective

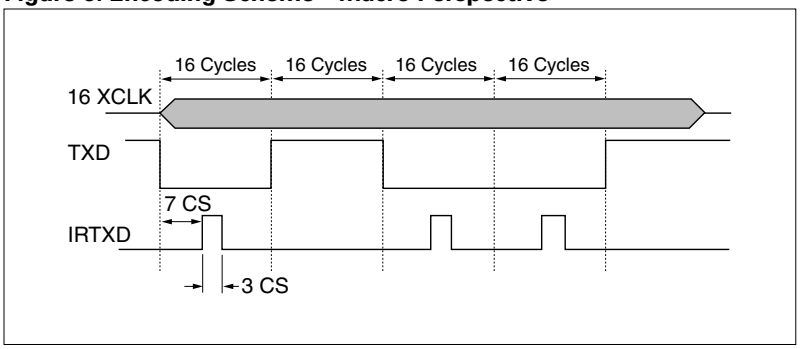
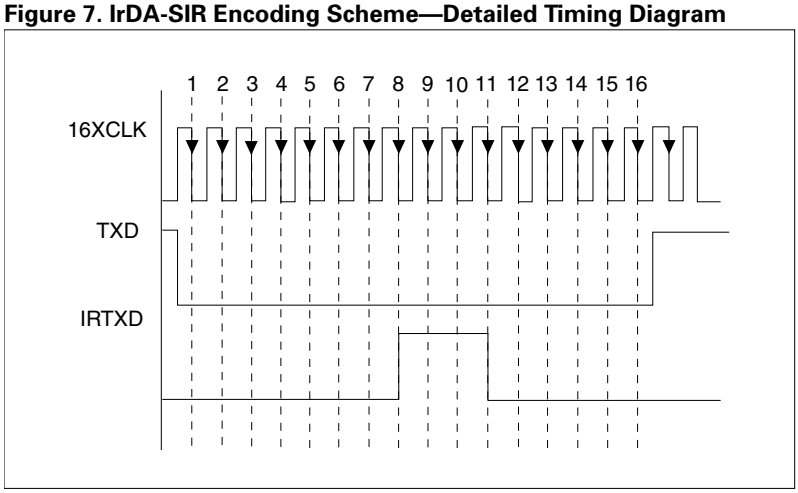


Figure 7. IrDA-SIR Encoding Scheme—Detailed Timing Diagram



Overview of the Decoding Scheme

The IRDA-SIR decoding modulation method can be thought of as a pulse stretching scheme:

Every high to low transition of the IR-RXD line signifies the arrival of a 3/16th pulse. This pulse needs to be *stretched* to accommodate 1 bit time (or 16 16XCLK cycles). Every pulse that is received is translated into a'O' or space on the RXD line. If a series of pulses separated by 1 bit time are received, then the net result is a *I bit time low pulse* for every 3/16th pulse received (see figure 9).

To be correctly received and interpreted by a UART, the stretched pulse must be at least 3/4 of a bit time in duration.

Figure 8. Decoding Scheme—Macro Perspective

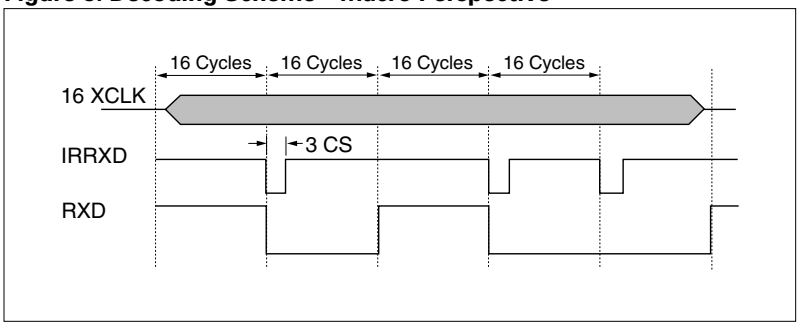


Figure 9. IrDA-SIR Decoding Scheme—Detailed Timing Diagram

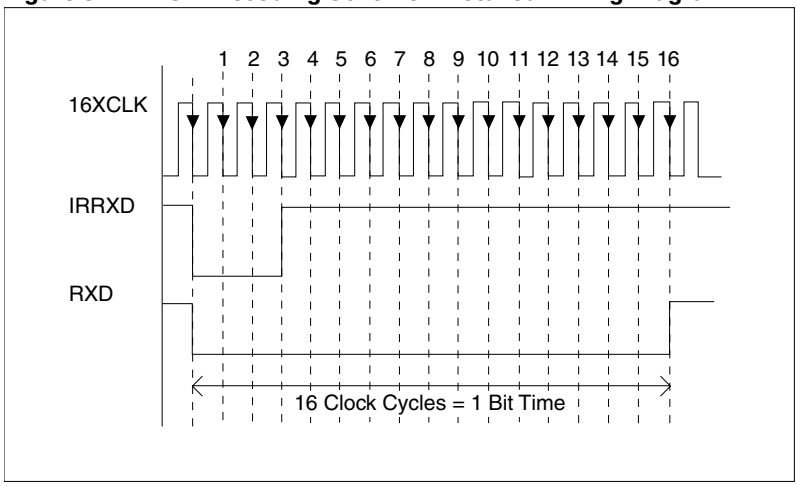


Figure 10. Monoshot Operation

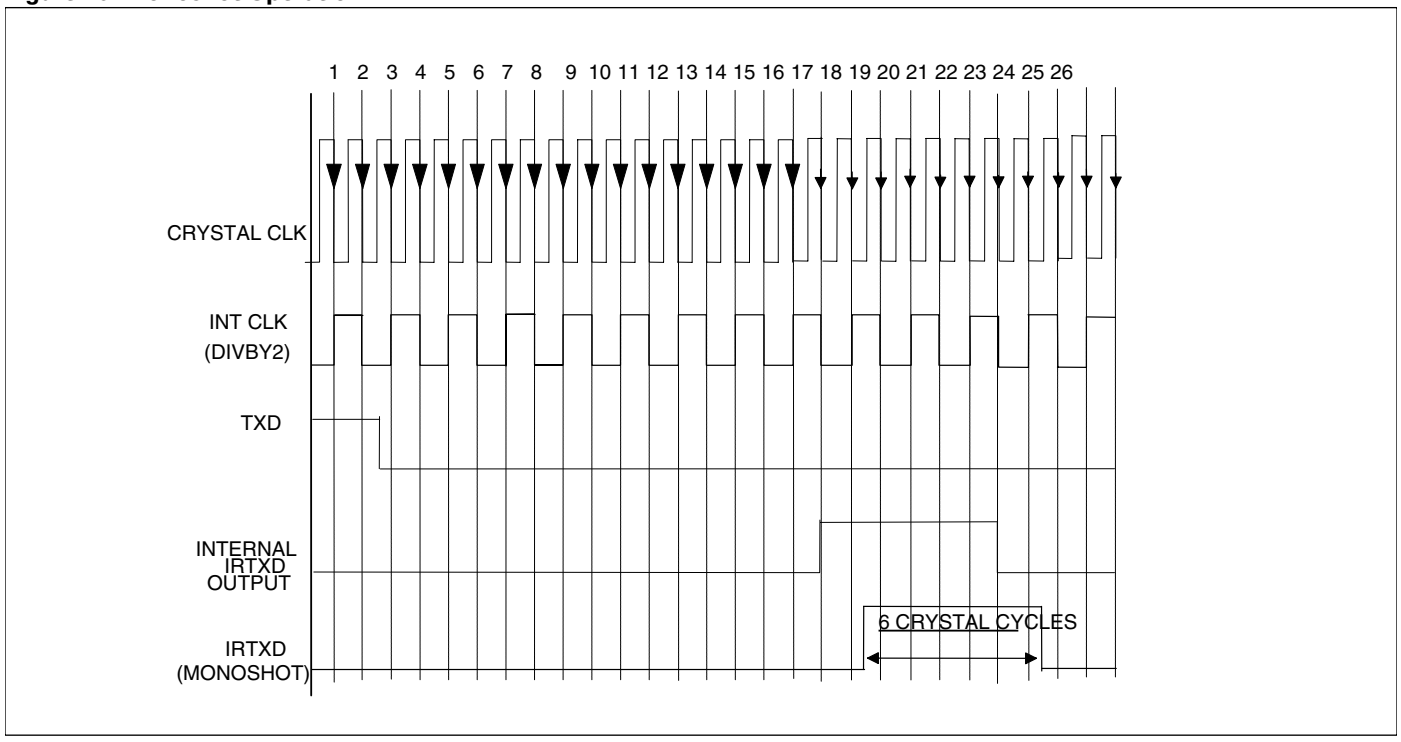


Fig 7 illustrates the operation of the monoshot when the internal clock is set to divide by 2 mode, i.e. when A2=0, A1=0 and A0=0. A rising edge on the internal modulation state machine (here called IRTXD OUTPUT), will cause the output on the IRTXD to go up for 6 crystal clock cycles. With a 3.6864MHz clock, this corresponds to a pulse of 1.63us. The duration of this pulse is independent of the code A2, A1, A0 and is always 6 clock cycles of the crystal, corresponding to the monoshot operation.

Figure 11. IRM5000/7001 Schematic with External Clock

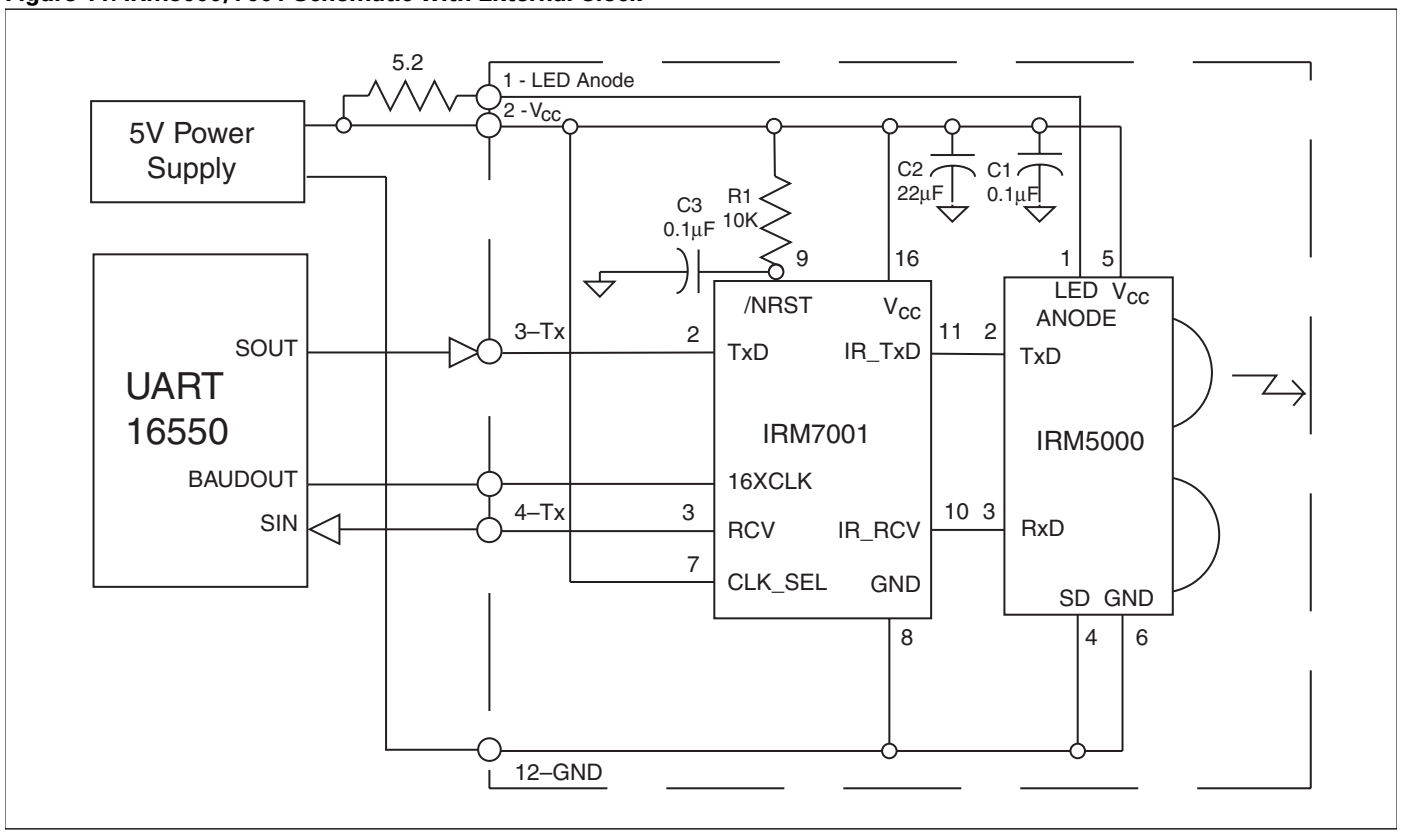


Figure 12. IRM5000/7001 Schematic using Internal Clock

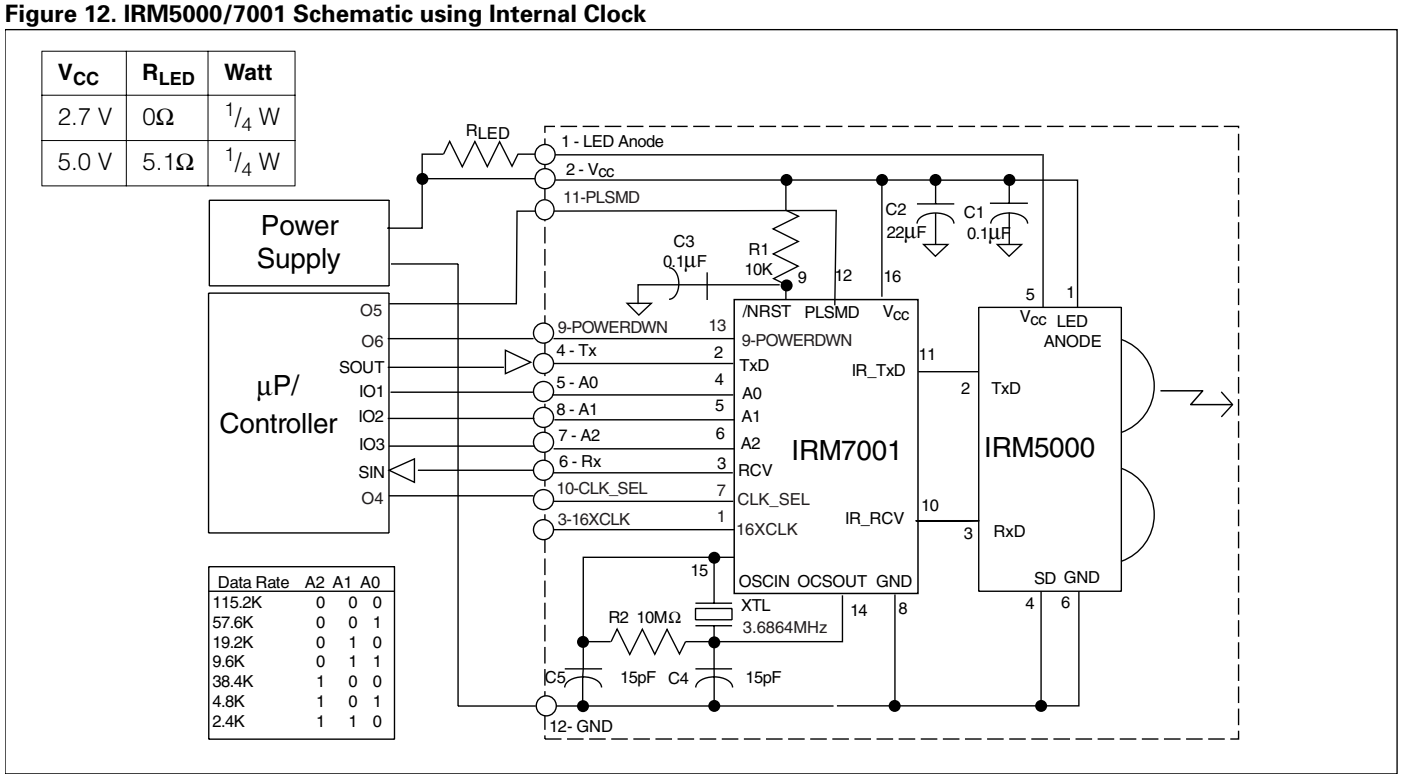


Table 7. IRM5000/7001 Eval Board Bill of Materials

Component	Case type	Description	Quantity
U1		IRM7001-Encoder/ Decoder IC (Infineon)	1 EA
U2		IRMS5000-IR Data Transceiver (Infineon)	1 EA
Y1	HC49	3.6864MHz Crystal Oscillator	1 EA
R1	1206	10KΩ Resistor	1 EA
R2	1206	10MΩ Resistor	1 EA
C1	1210	0.1µF Capacitor	1 EA
C2	C	22µF Capacitor	1 EA
C3	1210	0.1µF Capacitor	1 EA
C4	1206	15pF Capacitor	1 EA
C5	1206	15pF Capacitor	1 EA
PCB		DO2436-2 (Infineon)	1 EA

Figure 13. IRM5000/7001 Eval Board Looking from Front Side

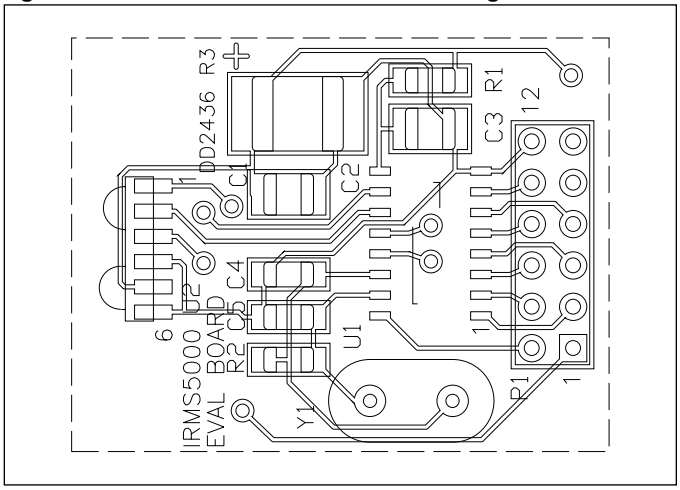


Figure 14. IRM5000/7001 Eval Board Looking from Back Side

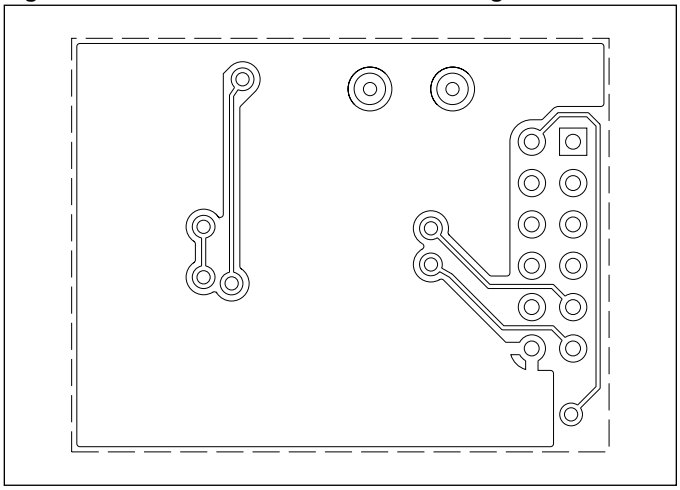


Figure 15. IRMS6118/7001 Schematic using Internal Clock

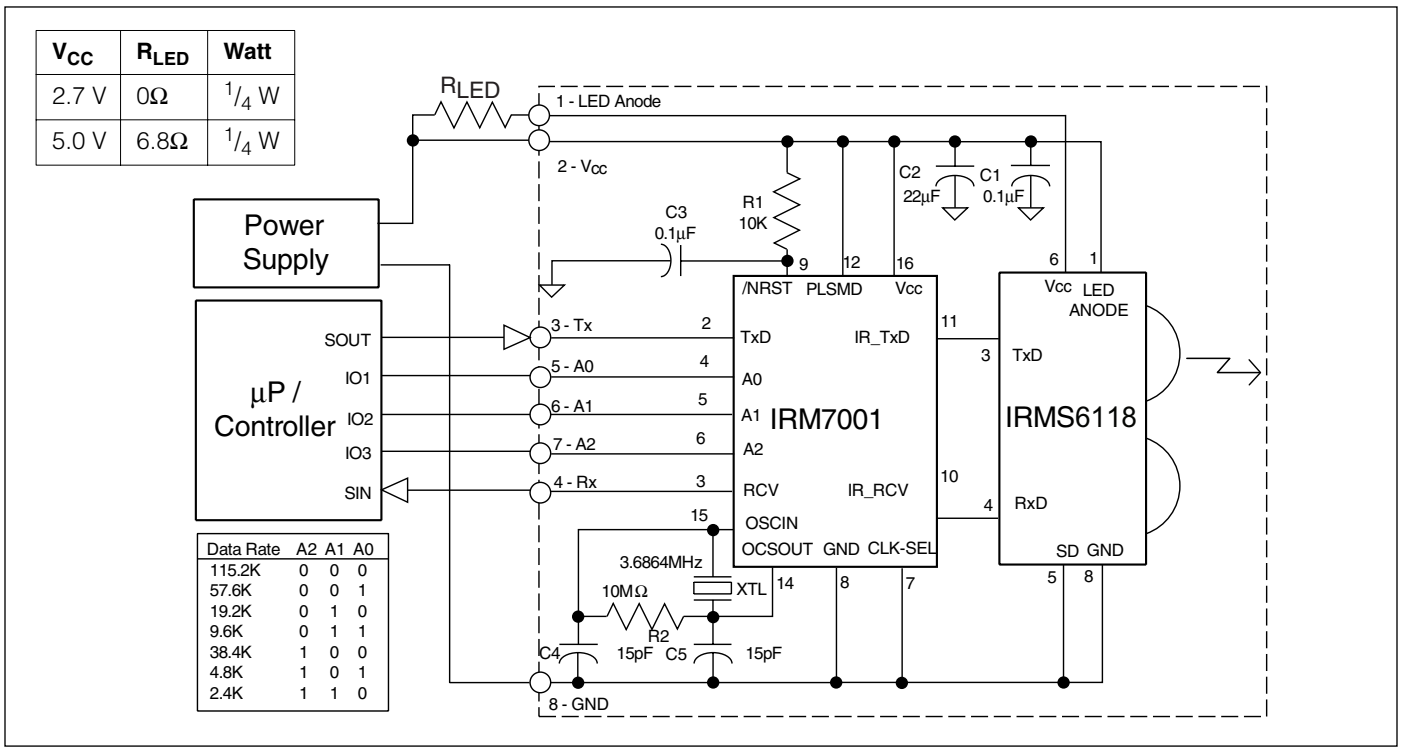
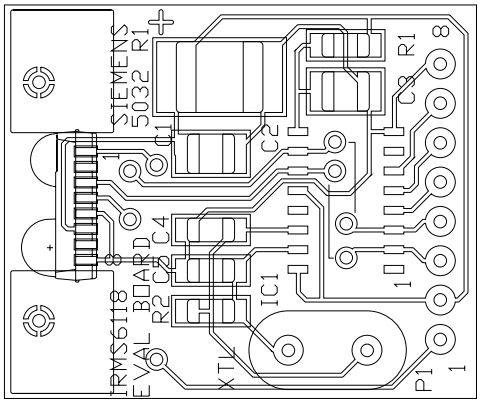


Table 8. IRMS6118/7001 Eval Board Bill of Materials

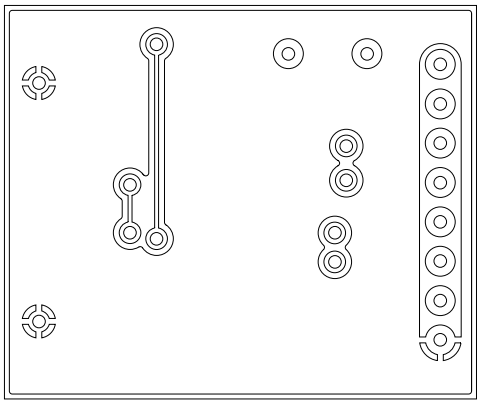
Component	Case type	Description	Quantity
U1		IRM7001-Encoder/ Decoder IC (Infineon)	1 EA
U2		IRMS6118-IR Data Transceiver (Infineon)	1 EA
Y1	HC49	3.6864MHz Crystal Oscillator	1 EA
R1	1206	10KΩ Resistor	1 EA
R2	1206	10MΩ Resistor	1 EA
C1	1210	0.1µF Capacitor	1 EA
C2	C	22µF Capacitor	1 EA
C3	1210	0.1µF Capacitor	1 EA
C4	1206	15pF Capacitor	1 EA
C5	1206	15pF Capacitor	1 EA
PCB		DO2436-(Infineon)	1 EA

Figure 16. IRMS6118/7001 Eval Board Looking from Front Side



Note:
For proper operation Pin 7 of IRM7001 should be connected to GND.

Figure 17. IRMS6118/7001 Eval Board Looking from Back Side



Design Notes:

1. When internal is used, CLK_SEL should be held low (connected to GND). In case of external clock CLK_SEL should be tied high (V_{CC}).
2. If PULSEMOD is held high and the internal clock is used, the IR_TXD is limited to a duration of 1.6µs irrespective of data rate. This helps in reducing LED current at lower data rates. This function cannot be used with external clock (16XCLK).
3. There are two methods of putting the internal oscillator cell in POWERDN MODE. Firstly, whenever CLKSEL line is asserted high, the oscillator cell is automatically put in power down mode. Secondly, the user may also decide to put the oscillator in power down mode by providing a high signal on the POWERDN input pin. Normally the POWERDN pin stays low.

PACKAGING

Production Package

The package is SOIC 16 pins (150 mils) plastic package.

Chips will be available in Tape and Reel (2500 units per reel).

QUALITY AND RELIABILITY

E.S.D. and latch-up

Maximum DC current through any pin thus avoiding latch-up: +/- 100 mA Electrostatic discharge protection: 4000 V for mono-supply voltage Electrostatic discharge protection: 2000 V for multi-supplies voltages E.S.D. sensitivity: MIL STD-883-3015.7 Class 2

Specific requirements: environmental endurance

A. Permanence of marking: MIL-STD-883 - Method 2015

B. Solderability: MIL-STD-883 - Method 2003

C. Resistance to soldering heat: MIL-STD-883 - Method 200