ICM7111

SPEECH AND RINGER IC WITH DIGITAL VOLUME CONTROL

FEATURES

- Includes Speech and Ringer Circuit in a single chip
- Digital volume control
- DTMF interface with adjustable gain
- Voltage regulator output
- Ring Frequency Discrimination
- Ring Melody Generator
- Operating Range From 15 to 100mA

OVERVIEW

ICM7111 is a low cost CMOS Speech and Ringer integrated circuit that performs all the necessary speech and line interface functions for telephone sets.

ICM7111 supports digital interface to adjust received audio level.

TYPICAL APPLICATION CIRCUIT

Typical application circuit is as specified in Appendix A.

PACKAGE

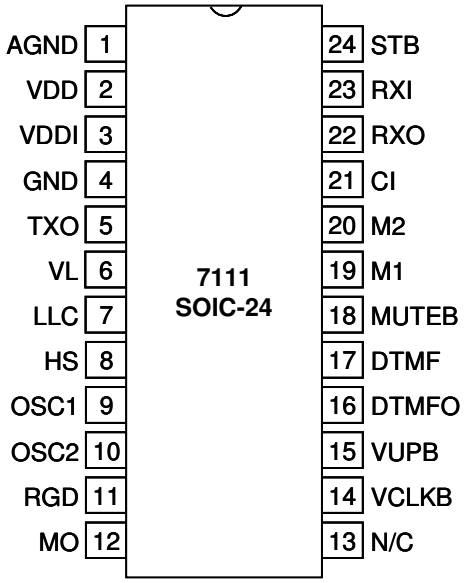


Figure 1.1: 24-lead SOIC Package

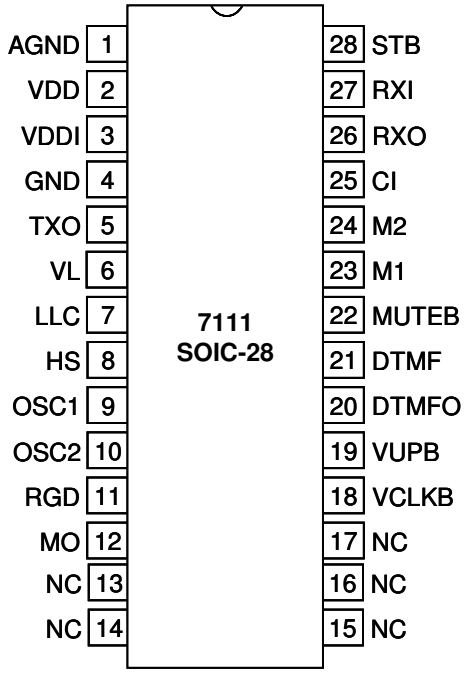


Figure 1.2: 28-lead SOIC Package

ORDERING INFO

Part No	Package
ICM7111	24-Lead SOIC
ICM7111S28	28-Lead SOIC

PIN DESCRIPTION

Pin No		Symbol	Description
SO24	SO28		
1	1	AGND	**Analog Ground** 1.4V regulated voltage output. Used by internal amplifiers. External capacitor about 100uF should be connected to this pin.
2	2	VDD	**Regulated Supply Voltage** When HS pin is HIGH, the VDD pin is regulated to 3.5V, and the input power is extracted from VDDI pin. Most internal circuits are powered by VDD pin.
3	3	VDDI	**Supply Input Voltage** Power for the chip is extracted from this VDDI pin. See also VDD pin description. At steady state, VDDI is regulated to 4.3V by use of external PNP transistor whose base terminal is connected to the TXO pin. See typical application circuit. The external PNP transistor also functions to drain the excess line current.
4	4	GND	**Ground**
5	5	TXO	**Transmit Output** Transmit output is to be connected to external PNP transistor (typically medium power PNP) for the modulation of line voltage and for shorting the line during make period of pulse dialing. See the typical application circuit. The external PNP transistor also functions to drain the excess line current.
6	6	VL	**Line Voltage** If line-loss compensation (LLC) scheme is not used, then this pin can be shorted to GND. If LLC scheme is used, then this pin is used to sense the line current. The sense resistor (R11 in typical application circuit) must be 30 ohm for the LLC scheme to work properly. The receive and transmit gains are adjusted according to the sensed current and the chosen LLC scheme. See also description on "Line Loss Compensation" section. Since VL pin will typically experience high transient voltage, it is advisable to properly add external protection circuit to suppress the high transient voltage which can damage the pin.
8	8	HS	**Hook Switch Input and Dial Pulse Output** When off-hook, this pin needs to be pulled HIGH (by the hook switch) to activate the speech and dialer circuits. When on-hook this pin needs to be pulled LOW to activate ringer circuit and deactivate speech and dialer circuits. During pulse dialing (while off-hook, and pulse dialing mode is chosen), this pin is pulled LOW during line-break periods.
9	9	OSC1	**Oscillator Input** 3.58MHz ceramic resonator input.
10	10	OSC2	**Oscillator Output** 3.58MHz clock output. Can be used to drive other few high impedance inputs.
11	11	RGD	**Ring Detection Input** Input for ring frequency detection. Active when HS=LOW. When pulses with frequency between 13Hz and 70Hz are detected on this pin, ring melody is generated on the MO pin.
12	12	MO	**Melody Output** Open drain output. When ring signal is detected on the RGD pin, ring melody pulses are generated on this pin.
13	13 14 15 16 17	NC	**No Connect**

14	18	VCLKB	**Volume Control Clock Input** If VUPB = 0; VCLKB pulse increases the volume in 3 steps to maximum. If VUPB = 1; VCLKB pulse decreases the volume in 4 steps to minimum. VCLKB has a weak internal pull-up. It should be connected to VDD if not used.
15	19	VUPB	**Volume Up/Down** Determines whether a pulse on VCLKB would increase or decrease the volume. See VCLKB description. VUPB has a weak internal pull-up. It should be connected to VDD if not used.
16	20	DTMFO	**DTMF Amplifier Output** DTMF amplifier output. Connecting a resistor between DTMF and DTMFO pins provides feedback for the internal DTMF amplifier.
17	21	DTMF	**DTMF Amplifier Inverting Input** DTMF amplifier inverting input. A resistor must be connected to this pin. The ratio of the feedback resistor (see DTMFO pin description) and this resistor sets the gain of internal DTMF amplifier, thereby sets the generated DTMF level.
18	22	MUTEB	**M1/M2 Input Inhibit** When MUTEB pin is LOW, the M1/M2 mic input is blocked, and the input from DTMF pin is transmitted.
19 20	23 24	M1 M2	**Microphone Inputs** Input for electret microphone. M1 connects to inverting input of internal differential amplifier via a resistor. M2 connects to the non-inverting input via a resistor.
21	25	CI	**Complex Impedance and AC Impedance Input** Placing resistor between CI and AGND pins adjusts the AC impedance. If CI pin is left floating the typical AC impedance is 1000 ohm (when current sense resistor (R11 as in typical application circuit) is 30 ohm).
22	26	RXO	**Received Audio Amplifier Output** Received audio amplifier output. RXO can drive a typical 120-ohm dynamic earpiece speaker.
23	27	RXI	**Received Audio Amplifier Input** Non-inverting input for internal received audio differential amplifier. RXI connects to the amplifier via an internal resistor. RXI also internally connects to the feedback path of the circuitry that determines the AC impedance.
24	28	STB	**Side Tone Balance Input** Inverting input for internal received audio differential amplifier. STB connects to the amplifier via an internal resistor.

FUNCTIONAL DESCRIPTION

SYSTEM STARTUP

ICM7111 generates internal power-on-reset when VDD reaches around 1.5V. Power-on-reset appropriately initiates the system to a known initial state. Note that the initial ramp up of VDD could come from external ringer interface circuit, or it could come from internal regulator when the system goes off-hook.

As long as HS pin stays LOW, ICM7111 operates in shutdown mode with only the ringer circuitry being activated to monitor the incoming ringing signal.

OSCILLATOR

All the timing of ICM7111 is based on a clock frequency of 3.58 MHz. A Crystal or ceramic resonator of this frequency should be connected to OSC1 and OSC2 pins. Care has to be taken in selecting this components since in practise minor deviations from the nominal frequency may occur due to the characteristics of the oscillator.

It is recommended to connect a small value capacitors (≤ 47pF) in parallel with the oscillator to ensure proper start-up and operation at the nominal frequency.

TONE RINGER

The tone ringer of ICM7111 consists of ring detection circuit and melody generator circuit. These circuits are active when the system is in on-hook state (HS pin is LOW).

Ring Detection Circuit

Ring detection circuit will assures the signal present on RGD pin input is valid. The signal is considered valid if it has frequencies between 13Hz and 70Hz. This signal is monitored continuously and the ring melody is turned on/off accordingly.

Melody Generator

Once the valid ring signal is detected on the schmitt-triggered ring detection pin (RGD) and the signal is present for about 75 ms continously, the melody generator will be enabled, generating ring tones of 1250Hz and 1600Hz on the MO pin. Note that MO is an open-drain pin.

SPEECH NETWORK

The speech network of ICM7111 consists of a transmitter and a receiver path, side tone cancellation and line loss compensation.

The speech network is activated as soon as the phone goes off-hook (i.e. when HS pin goes HIGH). At the same time the ringer circuitry is deactivated.

Transmit

The typical total transmit gain from microphone input (M1/M2 pins) to the VDDI pin is 35dB when the AC impedance is 600Ω.

Receive

The typical total receive gain from the line voltage to RXO pin is 5dB when the AC impedance is 600Ω.

Side Tone Cancellation

As shown in the typical application circuit in Appendix A, side tone cancellation can be achieved best by balancing the Whitestone bridge comprised of R11, R12, R13+R14//C6, and the line impedance.

Line Loss Compensation

LLC pin input level is scanned as the phone goes off-hook (i.e. as HS pin goes HIGH). At the same time, the loop current level is sensed and determined. If LLC=0, no compensation scheme is in effect.

If LLC=AGND, "low" compensation scheme is in effect. Transmit and receive gains are reduced by as much as 6dB when the loop current exceeds 50mA.

If LLC=VDD, "high" compensation scheme is in effect. Transmit and receive gains are reduced by as much as 6dB when the loop current exceeds 75mA.

AC Impedance (Z_{AC})

Placing a resistor, R_{ZAC} between CI and AGND pins adjusts the AC impedance. If R_{ZAC} is not

present, the typical AC impedance is 1000Ω. Refer to Figure 2 for the equivalent test circuit. R_{ZAC}=100KΩ typically sets the AC impedance to 600Ω. Please note that the overall system AC impedance also depends on the whole system circuit.

DTMF Signal

The ratio of resistor R35 over R37, as shown in the typical application circuit in Appendix A, is used to set the DTMF signal level. Higher ratio will result in higher DTMF signal level.

MUTEB pin must be pulled LOW to allow DTMF signal to be transmitted. This will also mute the M1/M2 input.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
VDDI	Supply Line Voltage	-0.3 to 7.0	V
V_{IN}	Digital Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-55 to +150	°C
T_{SOL}	Soldering Temperature	300	°C

Note 1: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature
Commercial	-25 °C to 70 °C

DC CHARACTERISTICS

(I_{LINE} = 15mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VDDI	Regulated Line Voltage	I_{LINE}: 13mA to 100mA	3.8	4.3	4.6	V
VDD	Regulated Supply			3.5		V
AGND	Regulated Reference		1.3	1.4	1.5	V
I_{DD}	Operating Current	Speech mode		2.5	5.5	mA
		Ring mode		0.3		mA
I_{OL}	Output Current Sink	HS, MO; V_{OL} = 0.4V		1.5		mA
VIL	Input Voltage Low	HS, RGD; T_A=25°C	0.0		1.5	V
VIH	Input Voltage High	HS, RGD; T_A=25°C	2.2		6.0	V

AC CHARACTERISTICS

(I_{LINE} = 15mA, Frequency = 800Hz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Transmit (TX)						
G_{TX}	Transmit Gain	LLC=GND, R_{ZAC}=100KΩ	32	33.5	35	dB
THD	Distortion	V_L < 0.5 V_{RMS}			2	%
$Z_{IN\ M1,M2}$	Input Impedance			20		KΩ
G_{MUTE}	Mute Attenuation	Mute activated	80			dB
$V_{IN\ M1,M2}$	Input Voltage Range	Differential Single Ended		± 1.0 ± 0.5		V_{PEAK} V_{PEAK}
Receive (RX)						
G_{RX}	Receive Gain	LLC=GND, R_{ZAC}=100KΩ, Volume=Reset	3.5	5.0	6.5	dB
THD	Distortion	V_{RXI} < 0.5 V_{RMS}			2	%
$Z_{IN\ RXI}$	Input Impedance			8		KΩ
$V_{IN\ RXI}$	Input Voltage Range			± 2.8		V_{PEAK}

Side Tone (ST)						
G_{ST}	Side Tone Cancellation	LLC=GND, R_{ZAC}=100KΩ	23			dB
$Z_{IN\ STB}$	Input Impedance			80		KΩ
$V_{IN\ STB}$	Input Voltage Range			± 2.8		V_{PEAK}
Output Driver (BJT)						
$V_{IN\ PNP}$	Input Voltage Range			± 2.8		V_{PEAK}
V_{TXPNP}	Dynamic Range			± 2.8		V_{PEAK}
Return Loss						
RL	Return Loss	Z_{LINE}=600Ω, R_{ZAC}=100KΩ	18			dB
HS INPUT						
t_{HS-L}	Low to High Debounce	Going off-hook		15		ms
t_{HS-H}	High to Low Debounce	Going on-hook		240		ms
Tone Ringer						
V_{MO}	Melody Output			PDM		
t_{MD}	Melody Delay				10	ms
F1	Frequency 1			1250		Hz
F2	Frequency 2			1600		Hz
t_{DT}	Detection Time	Ring Freq = 20Hz	50		80	ms
f_{MIN}	Min. Detection Freq.		13			Hz
f_{MAX}	Max. Detection Freq.				70	Hz

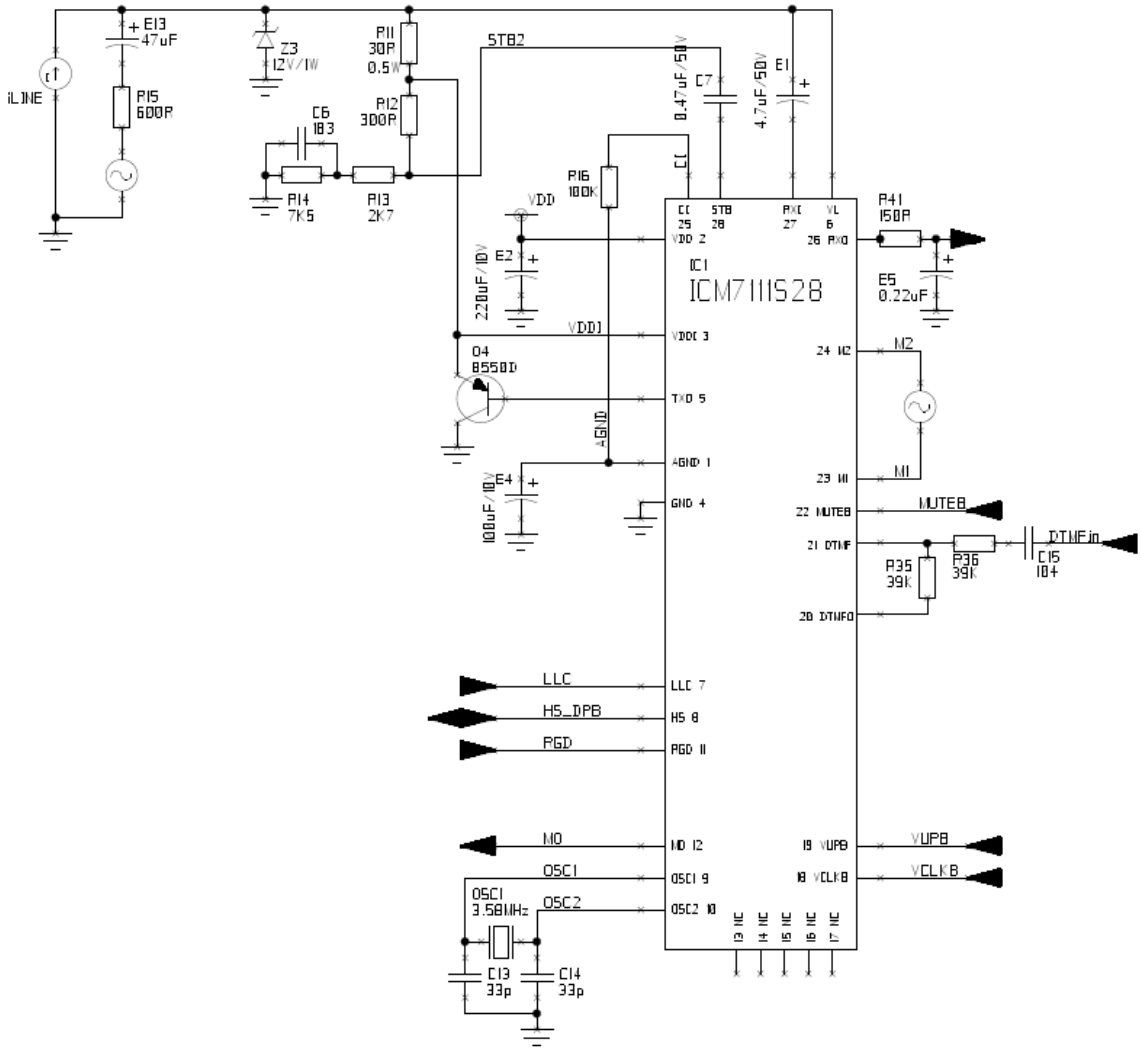
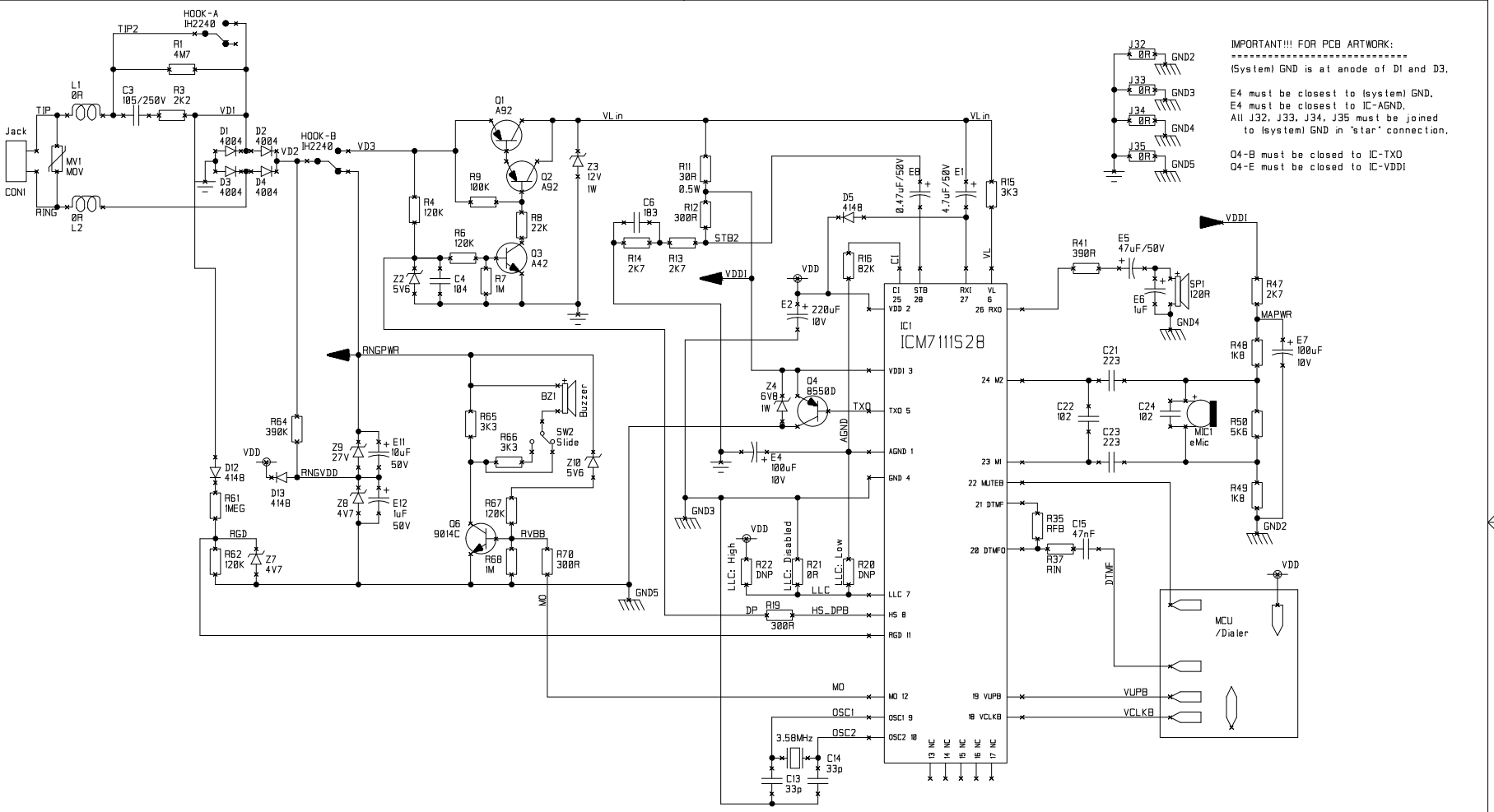


Figure 2: Equivalent Test Circuit

APPENDIX A: TYPICAL APPLICATION CIRCUIT

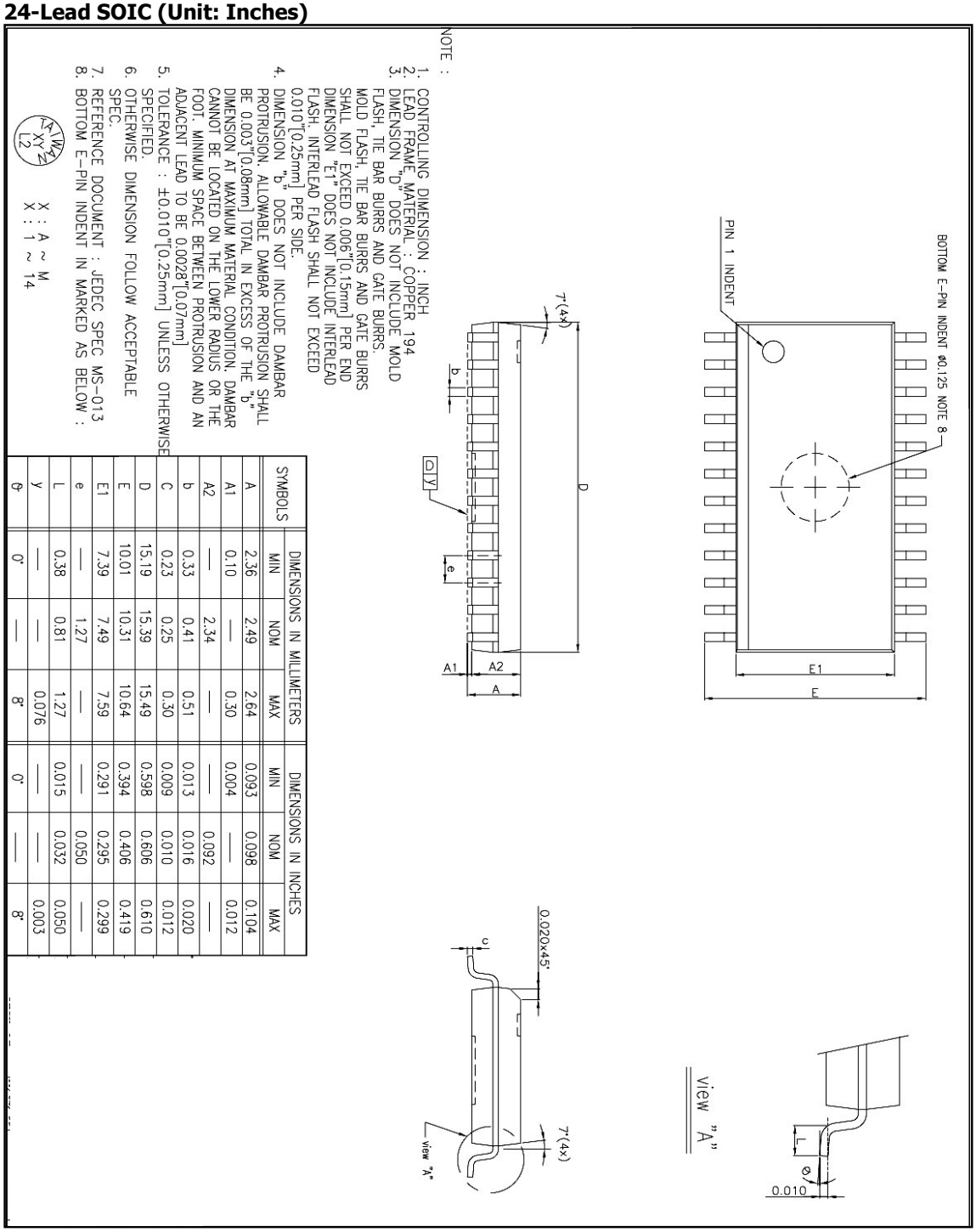


ICmic reserves the right to change the specifications without prior notice.

CONTRACT NO.		COMPANY NAME	IC Microsystems Sdn Bhd
APPROVALS	DATE	DWG	7111HA03
DRAWN	25-FEB-08	SIZE: B	FSCM NO. / DWG NO. / REV. 3.3
CHECKED	27-FEB-08		
ISSUED	27-FEB-08	SCALE	SHEET 1 of 1

APPENDIX B1: PACKAGE INFORMATION

24-Lead SOIC (Unit: Inches)



NOTE :

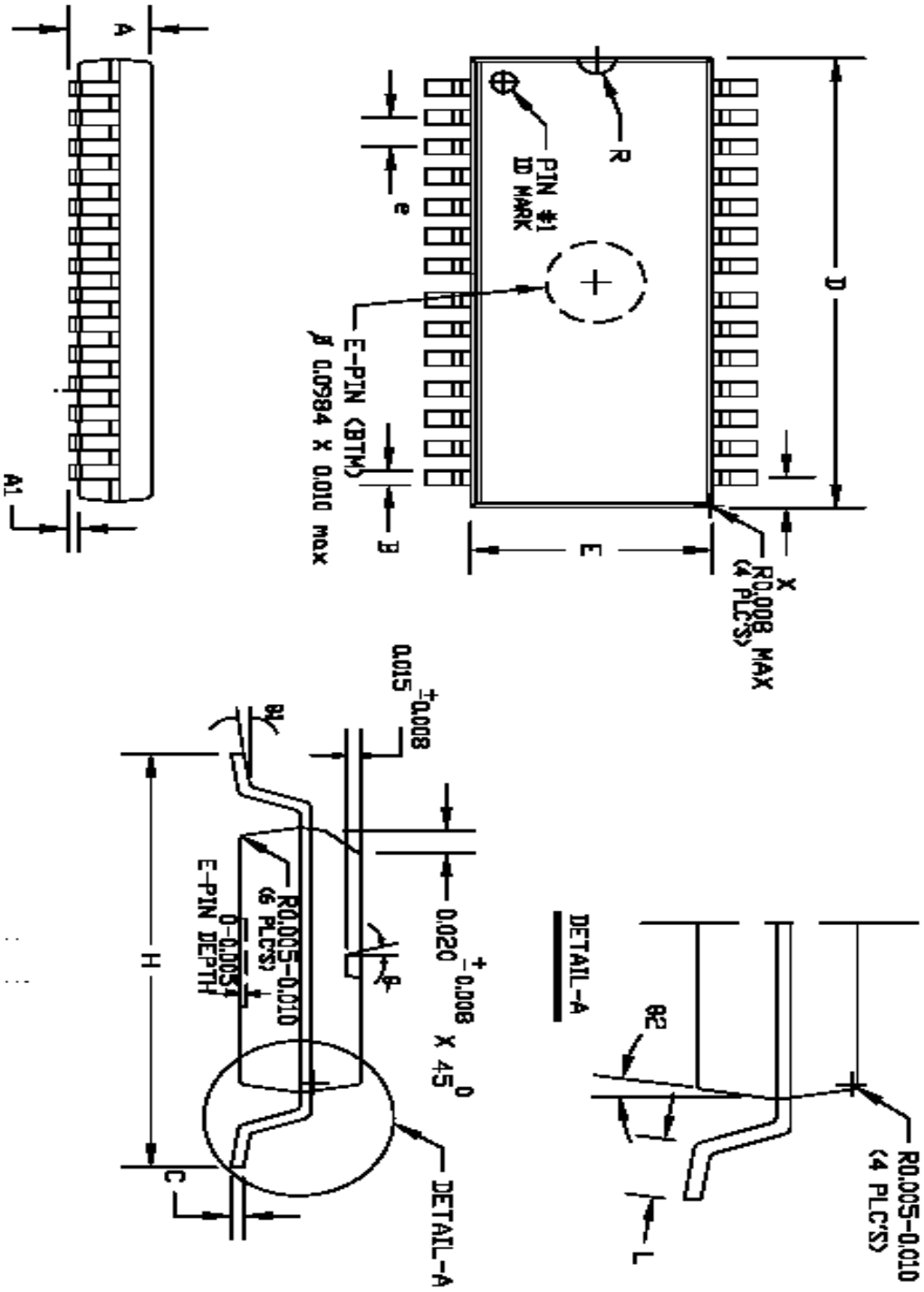
1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-013
8. BOTTOM E-PIN INDENT IN MARKED AS BELOW :

X : A ~ M
X : 1 ~ 14

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	—	2.34	—	—	0.092	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.23	0.25	0.30	0.009	0.010	0.012
D	15.19	15.39	15.49	0.598	0.606	0.610
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	—	1.27	—	—	0.050	—
L	0.38	0.81	1.27	0.015	0.032	0.050
y	—	—	0.076	—	—	0.003
Φ	0°	—	8°	0°	—	8°

APPENDIX B2: PACKAGE INFORMATION

28-Lead SOIC (Unit: Inches)



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