5 – 18 GHz High Power Amplifier

GaAs Monolithic Microwave IC

Preliminary

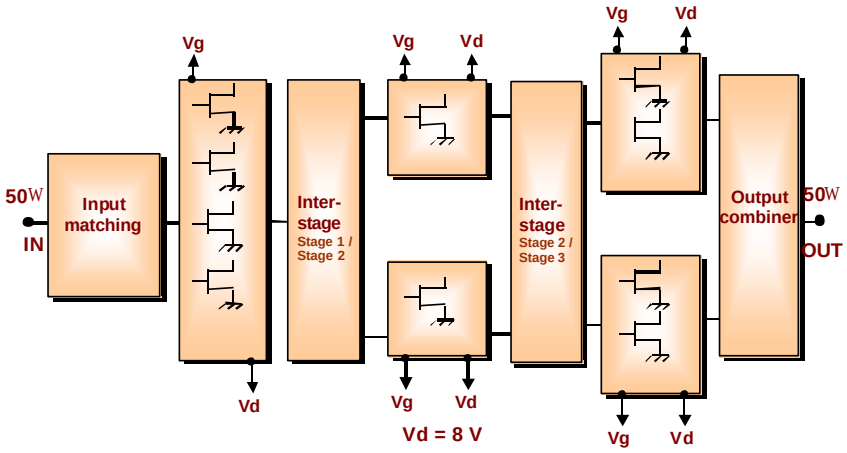
Description

The **CHA6518** is a monolithic three-stage GaAs high power amplifier designed for wide band applications.
This device is manufactured using a UMS 0.25 µm Power pHEMT process, including, via holes through the substrate and air bridges.
To simplify the assembly process:

- the backside of the chip is both RF and DC grounded
- bond pads and back side are gold plated for compatibility with eutectic die attach method and thermosonic or thermocompression bonding process.

Main Features

- 0.25 µm Power pHEMT Technology
- 5 – 18 GHz Frequency Range
- 2W Output Power
- 24 dB nominal Gain
- Quiescent Bias point : 8V ; 1A
- Chip size: 5.23 mm x 3.26 mm x 0.07 mm



Main Characteristics

Tamb = +25°C (Tamb is the back-side of the chip)

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency range	5		18	GHz
P_sat	Saturated output power		33.5		dBm
G_lin	Linear gain		24		dB

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Electrical Characteristics

Tamb = 25°C (2), Vd=8V, Ic (Quiescient) = 1A, CW biasing mode

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency	5		18	GHz
G_lin_1	Linear gain	20	24		dB
G_lin_T	Linear gain variation versus temperature		-0.045		dB/°C
RL_in	Input Return Loss	5.5	10		dB
RL_out	Output Return Loss	3.5	10		dB
P_sat_1	Saturated output power (5 to 6 GHz)	32.5	33		dBm
P_sat_2	Saturated output power (6 to 7 GHz)	33	34		dBm
P_sat_3	Saturated output power (8 to 10 GHz)	32.5	33		dBm
P_sat_4	Saturated output power (11 to 12 GHz)	32	32.5		dBm
P_sat_5	Saturated output power (13 to 14 GHz)	32.5	33		dBm
P_sat_6	Saturated output power (15 to 17 GHz)	33	34		dBm
P_sat_7	Saturated output power (18 GHz)	32	32.5		dBm
PAE_sat	Power Added Efficiency in saturation	11	20		%
Vd	Positive supply voltage		8		V
Id	Power supply quiescent current (1)		1		A
Vg	Negative supply voltage		-0.8		V
Top	Operating temperature range (2)	-30		+80	°C
NF	Noise Figure		5		dB

(1) This parameter is fixed by gate voltage Vg
(2) The reference is the back-side of the chip

Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
Pin (2)	Input continuous power	17	dBm
Vd (2)	Positive supply voltage without RF power	9	V
Id (2)	Positive supply quiescent current	1.5	A
|Ig| (2)	Gate supply current	88	mA
Pd (2)	Power dissipation	13.5	W
Tj	Junction temperature	175	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) These values are specified for Tamb = 25°C

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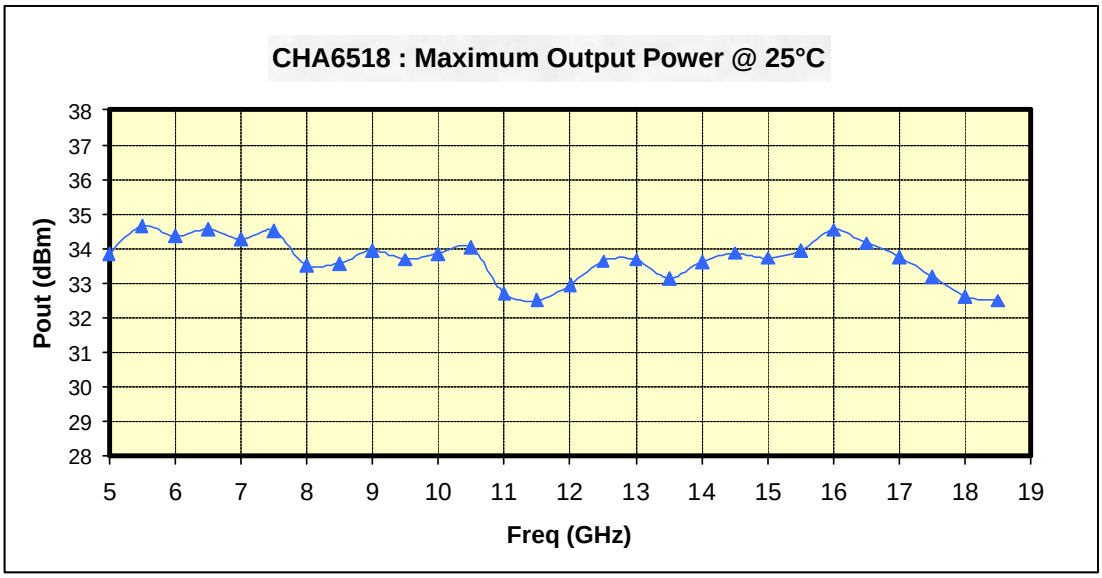
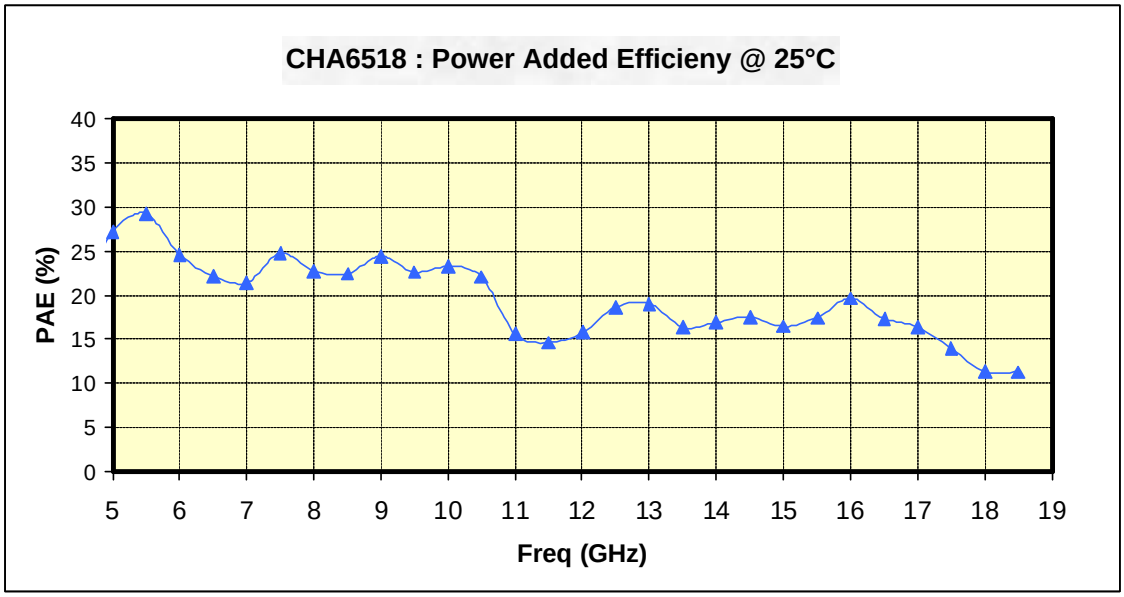
Typical measured characteristics

Measurements in test fixture :
Tamb=25°C, Vd=8V, Id (Quiescient) = 1A, CW Biasing mode, Pin=13dBm





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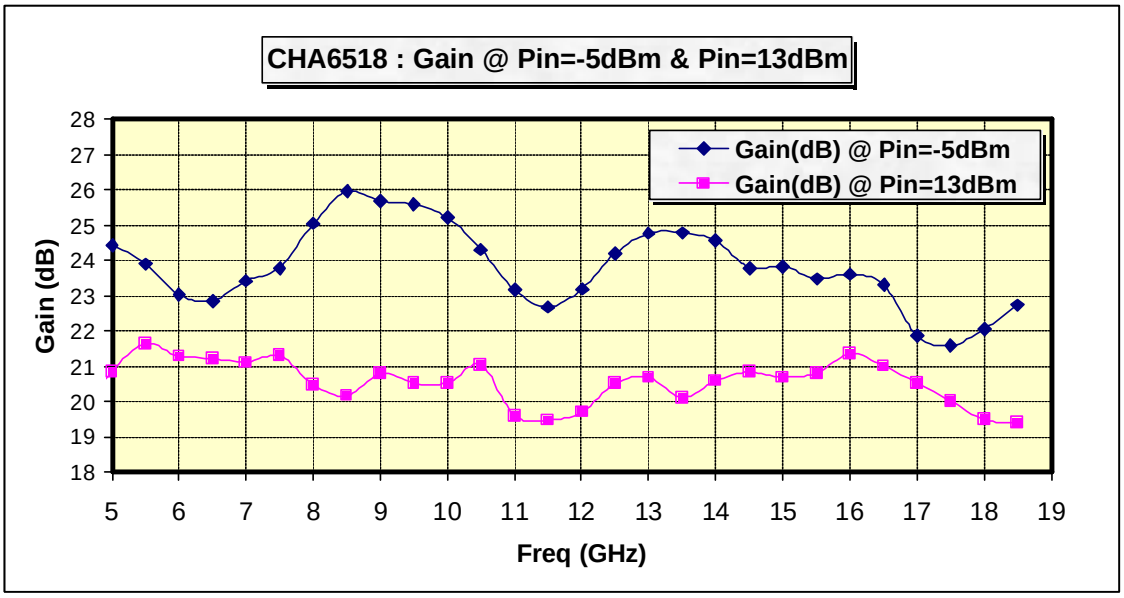

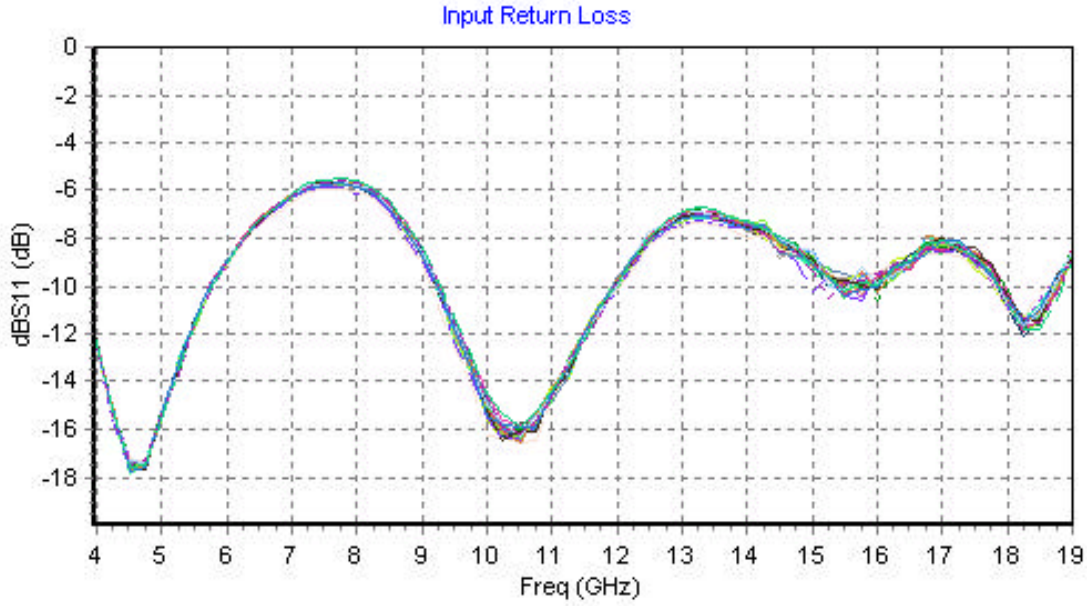

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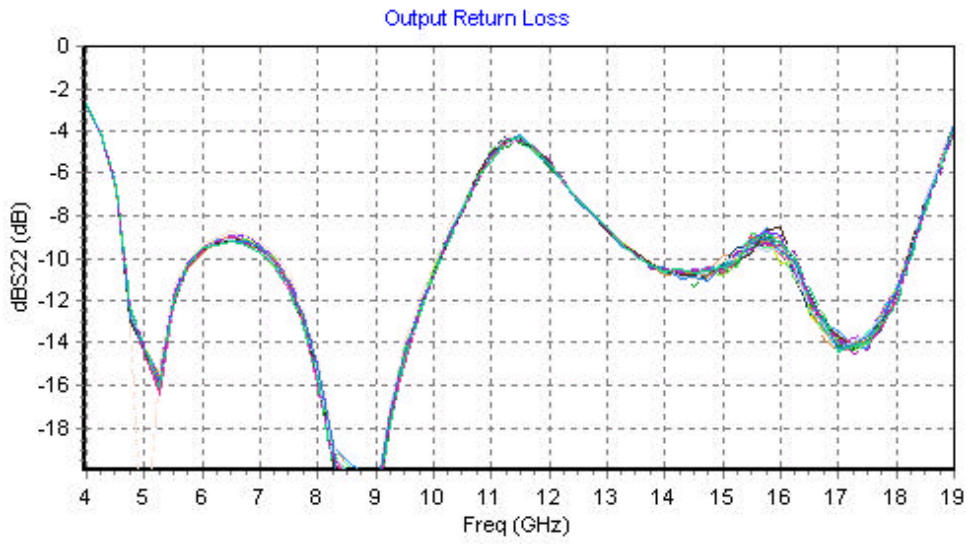
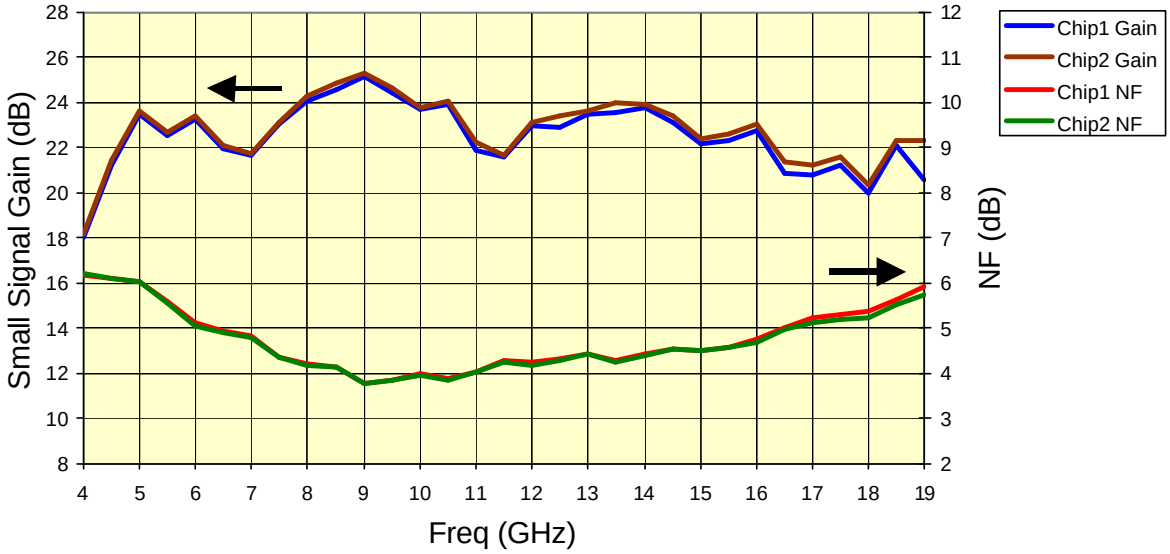


CHA6518 : Noise Figure @ 25°C



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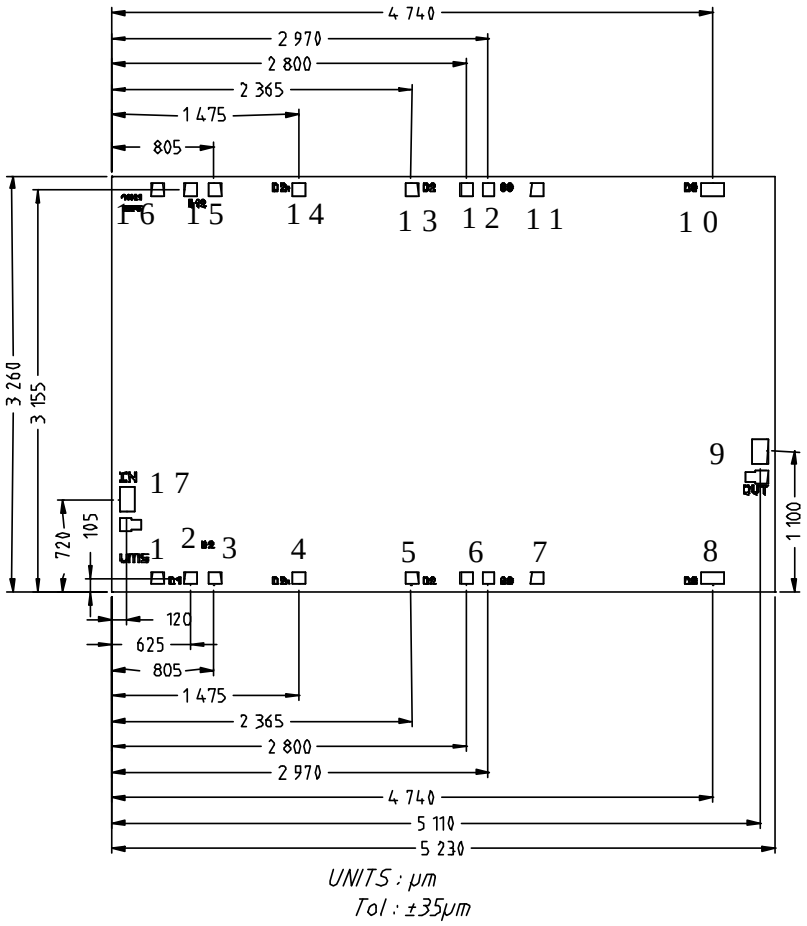
Chip Mechanical Data and Pin references



Chip thickness = 70µm +/- 10µm
HF pads (9, 17) = 118 x 196
DC pads (2, 3, 4, 5, 13, 14) = 96 x 96
DC pads (6, 12) = 268 x 96
DC pads 15 = 280 x 96
DC pads (8, 10) = 188 x 96

Pin number	Pin name	Description
17	IN	Input RF port
4, 14		NC
3, 6, 12, 15	VG	Negative supply voltage
1, 7,11, 16	GND	Ground (NC)
2, 5, 8, 10, 13	VD	Positive supply voltage
9	OUT	Output RF port

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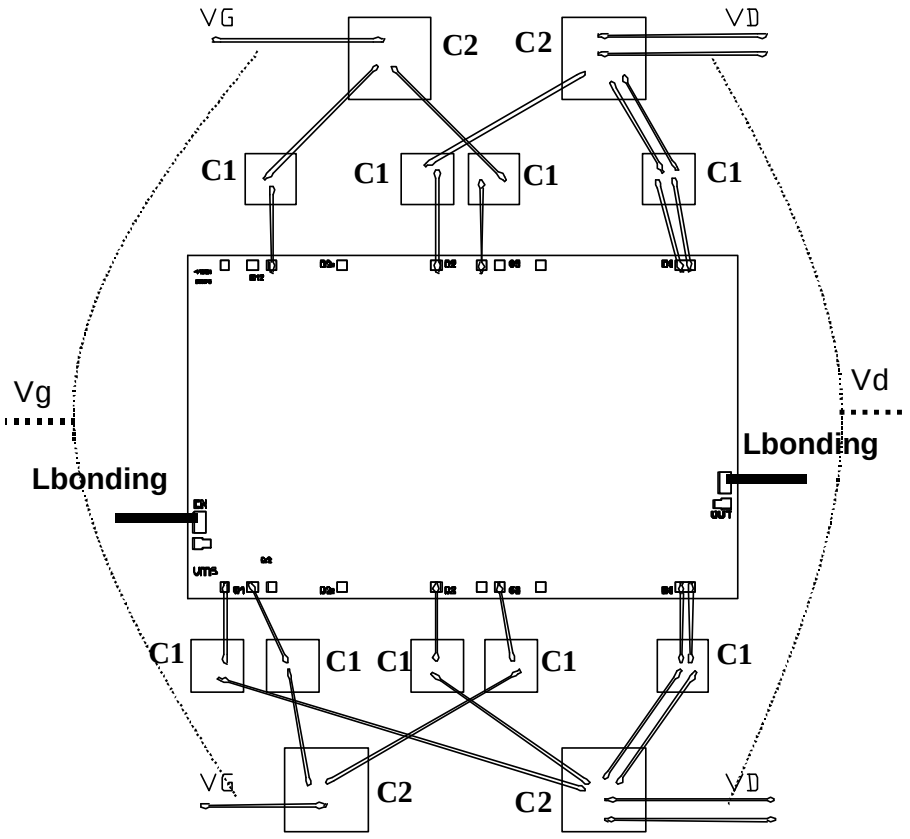
Assembly recommendations



For thermal and electrical considerations, the chip should be brazed on a metal base plate.
The RF, DC and modulation port inter-connections should be done according to the following table:

Port	Connection	External capacitor
IN (17)	Inductance (Lbonding) = 0.3nH	
OUT (9)	Inductance (Lbonding) = 0.3nH	
VD (2, 5, 8, 10, 13)	Inductance ≤ 1nH	C1 ~ 100pF C2 ~ 100nF
VG (3, 6, 12, 15)	Inductance ≤ 1nH	C1 ~ 100pF C2 ~ 100nF

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Ordering Information

Chip form : CHA6518-99F/00

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