

VOICE OTP IC

aP8921A – 21sec

aP8910A – 10sec

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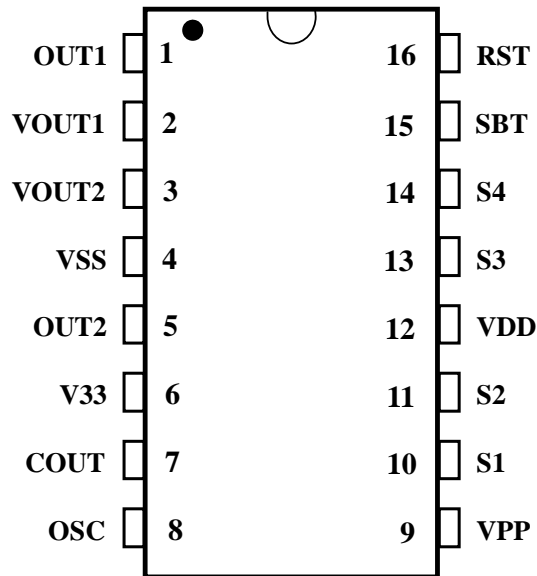
FEATURES

- Standard CMOS process.
- Embedded 512K/256K bits EPROM.
- 21/10 sec Voice Length at 6KHz sampling and 4-bit ADPCM compression.
- Maximum 12 voice groups.
- Combination of voice blocks to extend playback duration.
- 960 table entries are available for voice block combinations.
- User selectable PCM or ADPCM data compression.
- Two triggering modes are available (EPROM programmable options).
 - Key Trigger Mode – Combinations of S1 ~ S4 to trigger 12 Voice Groups; SBT sequential trigger is possible.
 - CPU Parallel Trigger Mode – Combinations of S1 ~ S4 with SBT goes HIGH to strobe start the voice playback.
- Voice Group Trigger Options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
- Whole Chip Options: Ramp / No-ramp; Output Options; Key / CPU trigger mode.
- 16ms (@ 8KHz sampling rate) Debounce Time in Key Trigger Mode.
- 65us (@ 8KHz sampling rate) Debounce Time in CPU Parallel Trigger Mode.
- RST pin set to HIGH to stop playback at once.
- Two user programmable outputs for STOP pulse, BUSY signal and flashing LED.
- Built-in oscillator to control sampling frequency with an external resistor.
- 2.6V – 5.0V; Wide range single power supply and < 5uA low stand-by current.
- PWM Vout1 and Vout2 drive speaker directly.
- D/A COUT to drive speaker through an external BJT.
- Development System support voice compilation and options selection.

DESCRIPTION

aP8921A/10A series high performance Voice OTP is fabricated with Standard CMOS process with embedded 512K/256K bits EPROM. It can store up to 21/10sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 8-bit PCM is also available as user selectable option. Two trigger modes, simple Key trigger mode and Parallel CPU trigger mode facilitate different user interface. User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 8-bit current mode D/A output and PWM direct speaker driving output minimize the number of external components. PC controlled programmer and developing software are available.

PIN CONFIGURATIONS



PIN NAMES

PIN	Playback Mode	OTP Program Mode	Description
1	OUT1	OEB	Programmable output (I/O pin)
2	VOUT1	-	PWM output to drive speaker directly
3	VOUT2	-	PWM output to drive speaker directly
4	VSS	VSS	Power Ground
5	OUT2	IO	Programmable output (I/O pin)
6	V33	V33	Power Supply for OTP programming
7	COUT	-	D/A current output
8	OSC	ACLK	Oscillator input
9	VPP	VPP	Supply voltage for OTP programming
10	S1	S1	Trigger pin (input with internal pull-down)
11	S2	S2	Trigger pin (input with internal pull-down)
12	VDD	VDD	2.6 – 5.0V Positive Power Supply
13	S3	S3	Trigger (input with internal pull-down)
14	S4	S4	Trigger (input with internal pull-down)
15	SBT	PGM	Trigger pin (input with internal pull-down)
16	RST	DCLK	Reset pin (input with internal pull-down)

PIN DESCRIPTIONS

S1 ~ S4

Input Trigger Pins:

- S1 to S4 is used to trigger the 12 Voice Groups in both Key and CPU Parallel Trigger Mode.
 - In OTP Programming Mode, S1 to S4 are used as program enable pins.
-

SBT

Input Trigger Pin:

- In Key Trigger Mode, this pin is trigger pin to trigger the playback of Voice Groups one by one sequentially.
 - In CPU Parallel Command Mode, this pin is used as address strobe to latch the input from S1 to S4 and starts the voice playback.
 - In OTP Programming Mode, this pin is used as PGM signal.
-

VDD and V33

Power Supply Pin for normal and programming operation

VSS

Power Ground Pin

VOUT1 and VOUT2

Digital PWM output pins which can drive speaker and buzzer directly for voice playback.

OSC

During voice playback, an external resistor is connected between this pin and the VDD pin to set the sampling frequency. In OTP Programming Mode, this is the ACLK input signal.

VPP

No connection during voice playback. In OTP Programming Mode, this pin is connected to a separate 6.5V power supply.

OUT1 and OUT2

- In Key Trigger Mode and CPU Parallel Command Mode, these pins are user programmable pins for the STOP pulse, BUSY and LED signals.
 - During OTP programming, OUT1 serves as OEB while OUT2 serves as data IO.
-

COU1

Analog 8-bit current mode D/A output for voice playback

RST

Chip reset in playback mode or DCLK pin in OTP programming mode.

VOICE SECTION COMBINATIONS

Voice files created by the PC base developing system are stored in the built-in EPROM of the aP8921A/10A chip as a number of fixed length Voice Blocks. Voice Blocks are then selected and grouped into Voice Groups for playback. Up to 12 Voice Groups are allowed. A Voice Block Table is used to store the information of combinations of Voice Blocks and then group them together to form Voice Group.

Chip	aP8921A	aP8910A
Memory size	512K bits	256K bits
Max no. of Voice Block	126	126
No. of bytes per Voice Block	512	256
Max. no. of Voice Group	12	12
No. of Voice Table entries	960	960
Voice Length (@ 6KHz 4-bit ADPCM)	21 sec	10 sec

Example of Voice Block Combination

Assume here we have three voice files, they are “How are You?”, Sound Effect and Music. Each of the voice file is divided into a number of fixed length Voice Block and stored into the memory.

Voice File 1 - “How are You?” is stored in Voice Block B0 to B12.

Voice File 2 - Sound Effect is stored in Voice Block B13 to B15.

Voice File 3 - Music is Voice Block B16 to B40.

Voice Blocks are grouped together using Voice Table to form Voice Group for playback:

Group no.	Voice Group contents	Voice Table Entries
Group 1	“How are You?”	B0 ... B12
Group 2	Sound Effect + “How are You?”	B13 ... B15 + B0 ... B12
Group 3	“How are You?” + Music	B0 ... B12 + B16 ... B40
Group 4	Music	B16 ... B40

Voice Data Compression

Voice File data is stored in the on-chip EPROM as either 4-bit ADPCM or 8-bit PCM format.

Voice data stored as 4-bit ADPCM provides 2:1 data compression which can save 50% of memory space. On the other hand, voice data are stored as 8-bit PCM format means no data compression is employed but voice playback quality will be better.

Programmable Options

In both Key Trigger Mode and CPU Parallel Trigger Mode, user can select different trigger functions and output signals to be sent out from the pins OUT1 and OUT2.

Options affect all Voice Group playback are called Whole Chip Options. Options only affect the playback of individual Voice Group are called Group Options.

Whole Chip Options

- Key or CPU Parallel Trigger Mode.
- Ramp-up-down enable or disable:

When COUT is used for playback, Ramp-up-down should be enabled. This function eliminates the ‘POP’ noise at the beginning and end of voice playback.

When VOUT1 and VOUT2 are used to drive speaker directly, Ramp-up-down should be disabled.

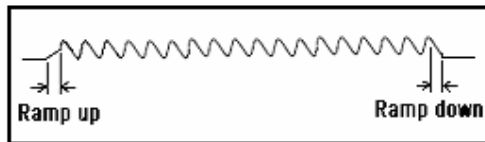


Fig. 1 Ramp-up-down Enable

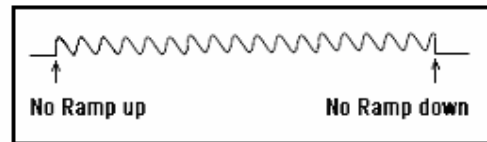


Fig.2 Ramp-up-down Disable

- Output Options:

This option sets up the three output pins OUT1 and OUT2 to send out different signals during voice playback. Four settings are allowed:

	aP8910A		aP8921A	
	OUT1	OUT2	OUT1	OUT2
Option 1	LED2	LED1	LED2	LED1
Option 2	STOP	LED1	LED2	STOP
Option 3	LED2	BUSY	LED2	BUSY
Option 4	-	-	STOP	BUSY

Note: Stop plus must be set to enable in order to have STOP plus to come out.

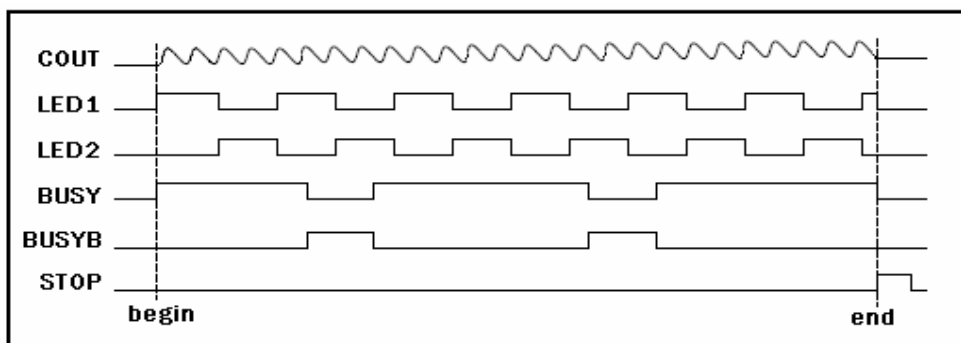


Fig. 3 Output waveforms

Group Options

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable
- Stop pulse disable or enable

Fig. 4 to Fig. 9 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

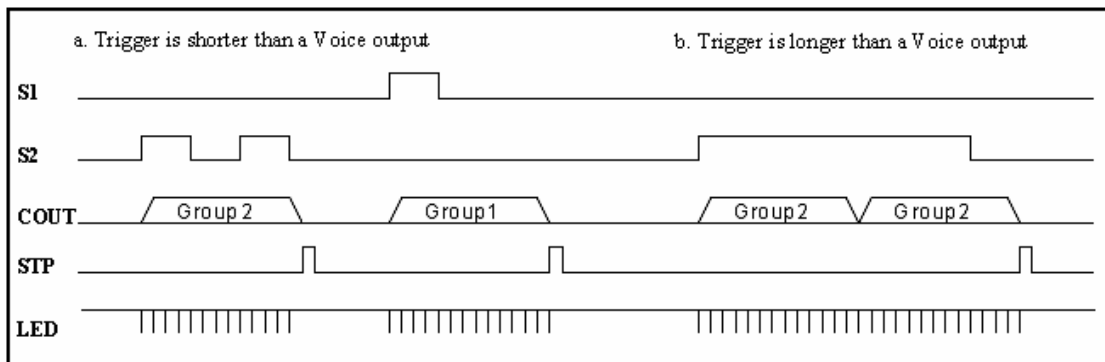


Fig. 4 Level, Unholdable, Non-retriggerable

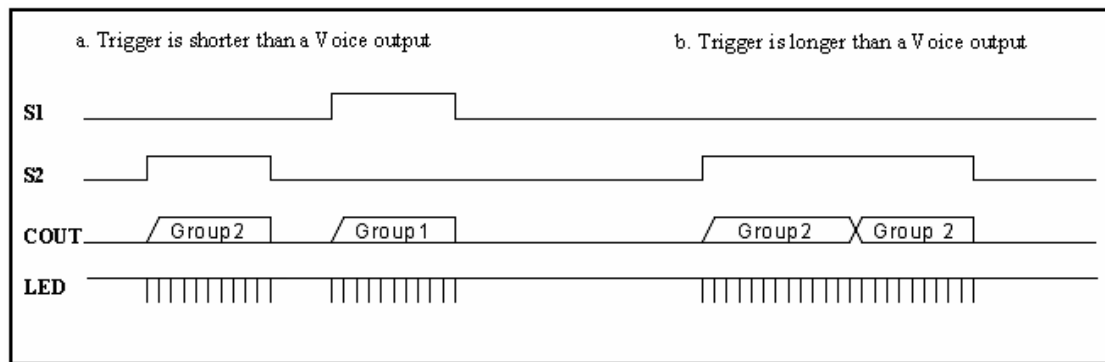


Fig. 5 Level Holdable

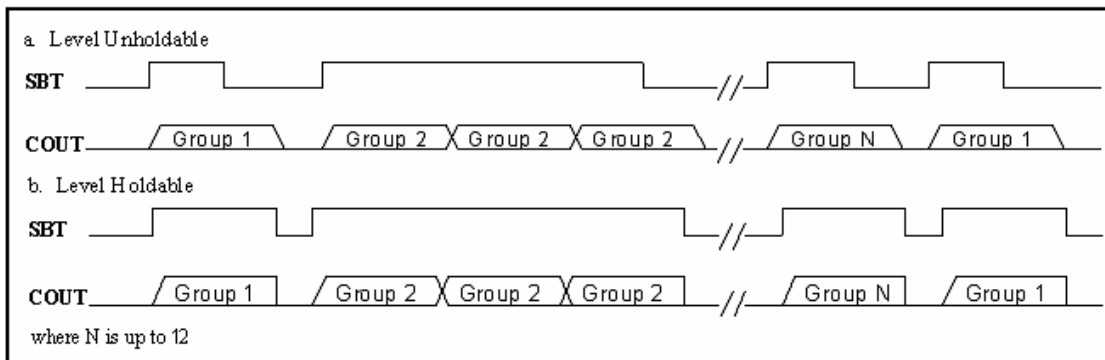


Fig. 6 SBT sequential trigger with Level Holdable and Unholdable

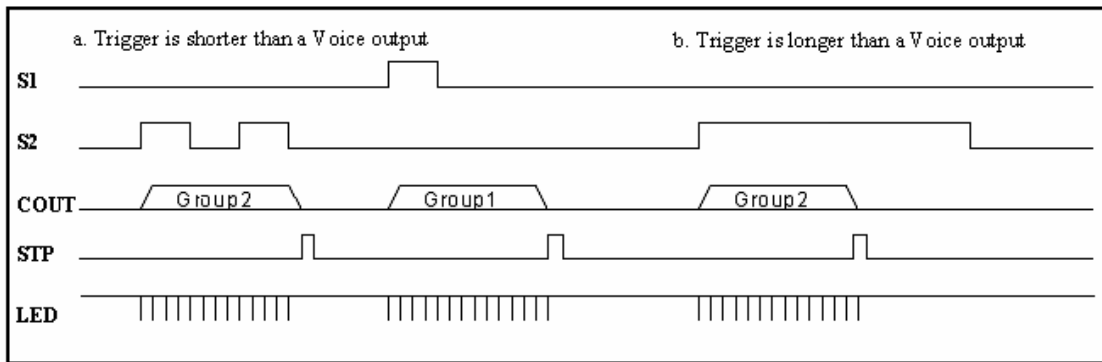


Fig. 7 Edge, Unholdable, Non-retrigger

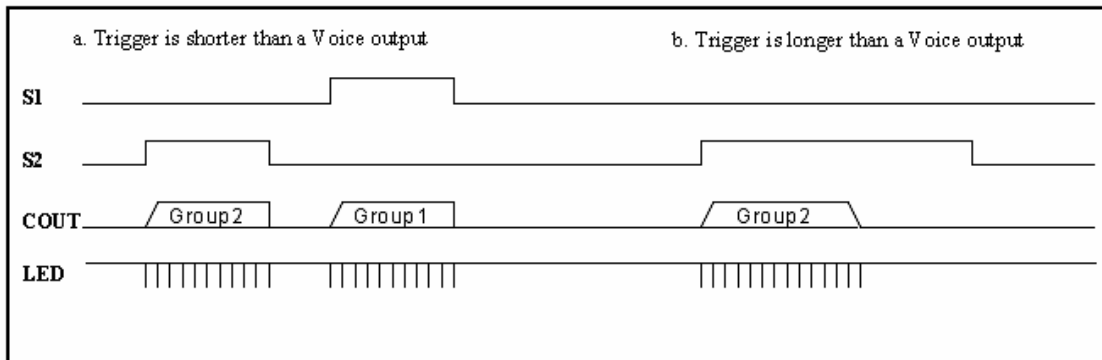


Fig. 8 Edge, Holdable

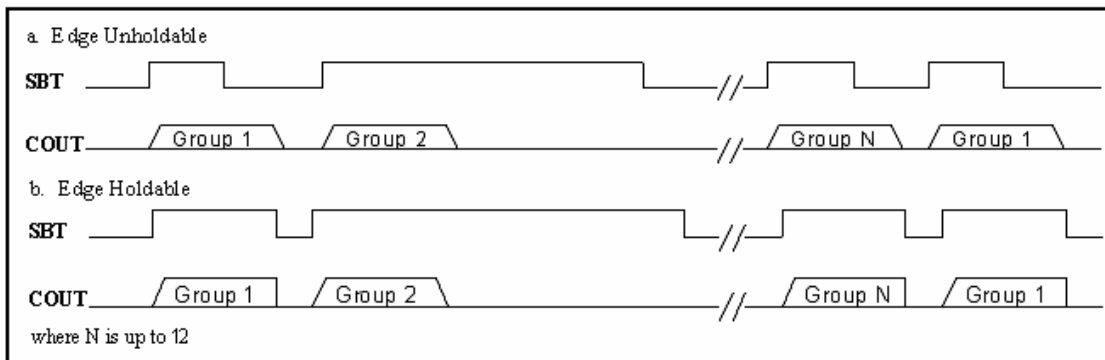


Fig. 9 SBT sequential trigger with Edge Holdable and Unholdable

Overlap trigger is supported with Level/Unholdable trigger options:

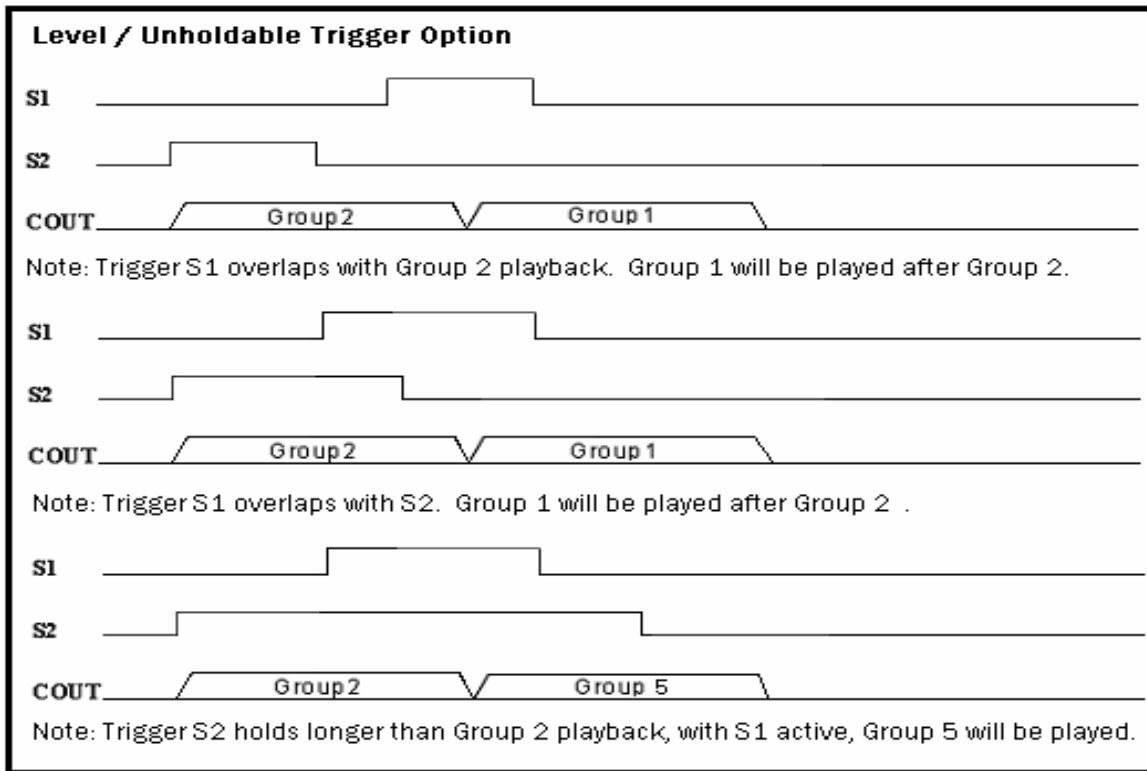


Fig. 10 Overlap trigger

TRIGGER MODES

Two trigger modes, the KEY and CPU modes, are available for aP8921A/10A series which are determined by setting the EPORM programmable options during voice data compilation.

For both trigger modes, up to 12 Voice Groups are being played back according to the following setting of trigger pins S1 to S4.

Voice Group	S1	S2	S3	S4
1	HIGH	NC	NC	NC
2	NC	HIGH	NC	NC
3	NC	NC	HIGH	NC
4	NC	NC	NC	HIGH
5	HIGH	HIGH	NC	NC
6	NC	HIGH	HIGH	NC
7	NC	NC	HIGH	HIGH
8	HIGH	NC	NC	HIGH
9	HIGH	HIGH	HIGH	NC
10	NC	HIGH	HIGH	HIGH
11	HIGH	NC	HIGH	HIGH
12	HIGH	HIGH	NC	HIGH

Note: Where NC (open or no connection) should be replaced by a logic input LOW in CPU Parallel Trigger Mode.

Key Trigger Mode

With this trigger mode, up to 12 Voice Groups are triggered by setting S1 to S4 to HIGH or NC in different combinations. Each Voice Group can have its only independent trigger options (See Fig. 4, 5, 7 and 8 for trigger options definition).

Voice Groups can also be triggered sequentially by setting SBT pin to HIGH.

CPU Parallel Trigger Mode

In this mode, S1 to S4 are set to HIGH or LOW according to the table above and followed by setting the SBT input pin to HIGH, the corresponding Voice Group will be triggered.

Trigger options defined in Fig. 4, 5, 7 and 8 are valid for this mode.

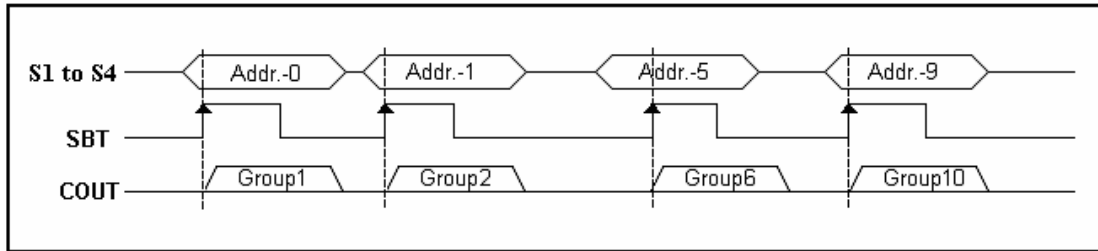


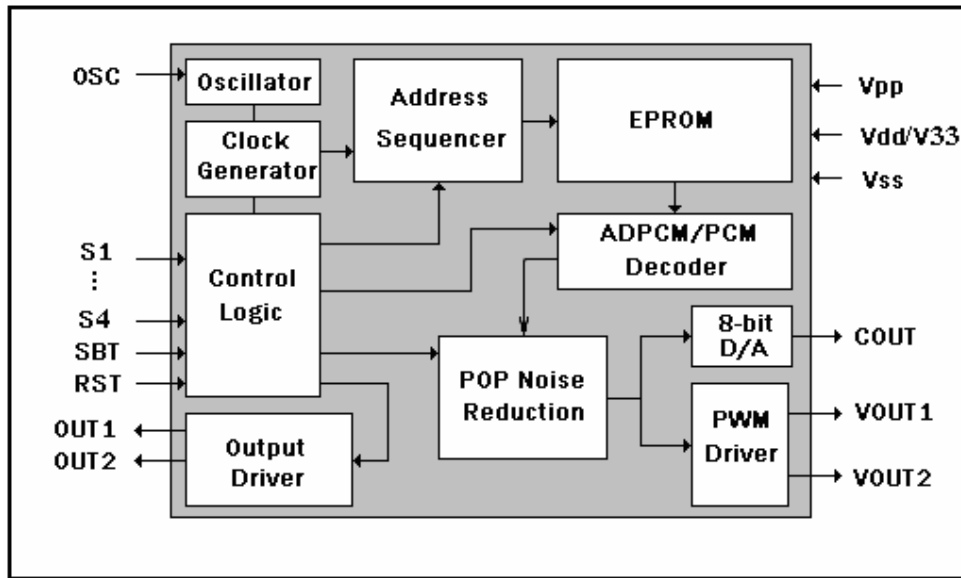
Fig. 11 CPU Parallel Trigger Mode

Note that SBT pin cannot be used as Single Button Sequential trigger in this mode. In stead, it acts as a Strobe input to clock-in the data input from S1 to S4 into the chip.

Voice Groups address is determined by the Voice Group Trigger Table. For example:

- S1..S4 = 1000 for Voice Group #1
- S1..S4 = 0100 for Voice Group #2
- ...
- S1..S4 = 1100 for Voice Group #5
- ...
- S1..S4 = 1110 for Voice Group #9
- ...
- S1..S4 = 1101 for Voice Group #12

BLOCK DIAGRAM



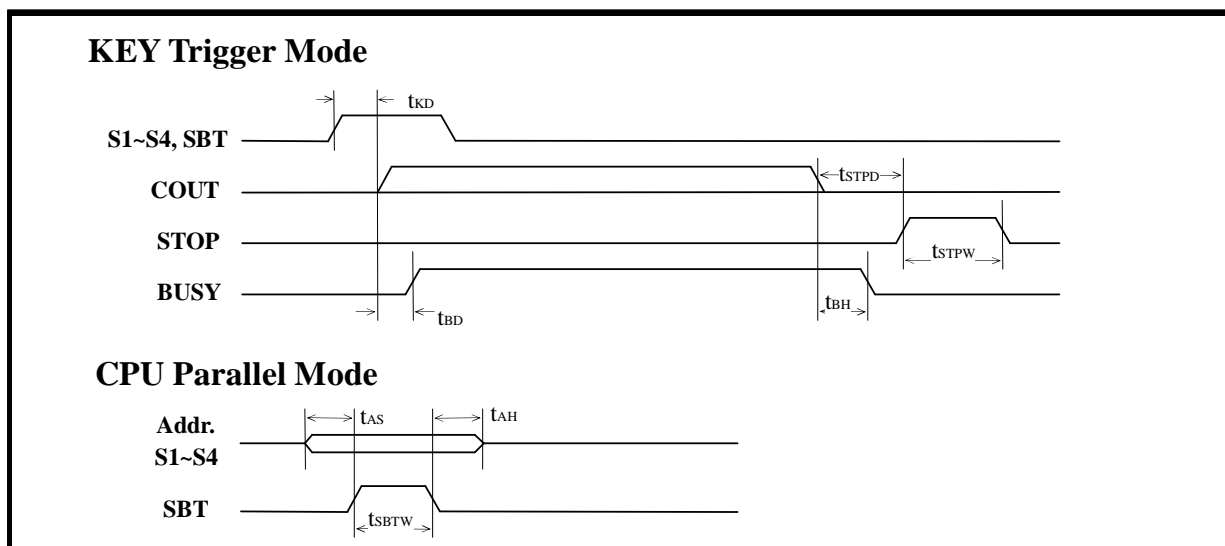
ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
$V_{DD} - V_{SS}$	-0.5 ~ +6	V
V_{IN}	$V_{SS} - 0.3 < V_{IN} < V_{DD}/33 + 0.3$	V
V_{OUT}	$V_{SS} < V_{OUT} < V_{DD}/33$	V
T (Operating):	-40 ~ +85	°C
T (Junction)	-40 ~ +125	°C
T (Storage)	-55 ~ +125	°C

DC CHARACTERISTICS ($T_A = 0$ to 70°C , $V_{DD} = 4.5\text{V}$, $V_{SS} = 0\text{V}$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	2.6	4.5	5.0	V	
I_{SB}	Standby current	—	1	5	μA	I/O open
I_{OP}	Operating current	—	—	15	mA	I/O open
V_{IH}	"H" Input Voltage	2.5	3.0	3.5	V	$V_{DD}=3.0\text{V}$
V_{IL}	"L" Input Voltage	-0.3	0	0.5	V	$V_{DD}=3.0\text{V}$
I_{OL}	V_{OUT} low O/P Current	—	110	—	mA	$V_{out}=0.3\text{V}$, $V_{DD}=5.0\text{V}$
I_{OH}	V_{OUT} high O/P Current	—	-110	—	mA	$V_{out}=2.5\text{V}$, $V_{DD}=5.0\text{V}$
I_{CO}	C_{OUT} O/P Current	—	-3	—	mA	$V_{COUT}=1.0\text{V}$
I_{OH}	O/P high Current	—	-8	—	mA	$V_{OH}=2.5\text{V}$, $V_{DD}=5.0\text{V}$
I_{OL}	O/P low Current	—	8	—	mA	$V_{OL}=0.3\text{V}$, $V_{DD}=5.0\text{V}$
$\Delta F/F$	Frequency Stability	-5	—	+5	%	$\frac{F_{osc}(5.0\text{V}) - F_{osc}(4.0\text{V})}{F_{osc}(4.5\text{V})}$

TIMING WAVEFORMS



AC CHARACTERISTICS ($T_A = 0$ to 70°C , $V_{DD} = 4.5\text{V}$, $V_{SS} = 0\text{V}$, 8KHz sampling)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_{KD}	Key trigger debounce time	16	—	—	ms	1
t_{KD}	Key trigger debounce time – retrigger	24	—	—	ms	1
t_{STPD}	STOP pulse output delay time	—	—	256	μs	
t_{STPW}	STOP pulse width	—	64	—	ms	1
t_{BD}	BUSY signal output delay time	—	—	100	ns	
t_{BH}	BUSY signal output hold time	—	100	—	ns	
t_{AS}	Address set-up time	100	—	—	ns	
t_{AH}	Address hold time	100	—	—	ns	
t_{SBTW}	SBT stroke pulse width	65	—	—	μs	1
t_{LEDC}	LED flash frequency	—	3	—	Hz	2

Notes :

1. This parameter is inversely proportional to the sampling frequency.
2. This parameter is proportional to the sampling frequency.

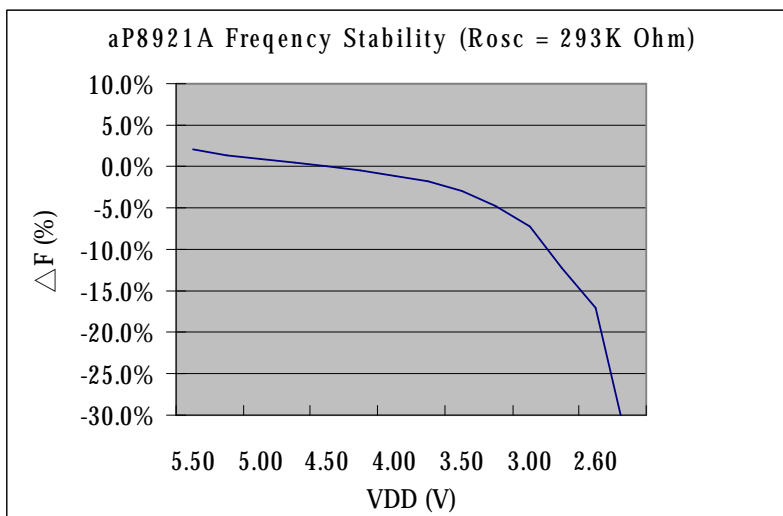
OSCILLATOR RESISTANCE TABLE

Sampling Frequency KHz	R _{OSC} KΩ
22	83
18	108
16	125
15	134
13	158
12	168
11	183
10	202
9	227
8	252
7	296
6	344

R _{OSC} KΩ	Sampling Frequency KHz
400	5.4
370	5.9
350	6.3
330	6.5
300	7.0
280	7.6
250	8.5
220	9.5
200	10.3
170	11.9
150	13.8
120	16.5
100	19.3
91	20.5
82	22.4

Note: The data in the above tables are within 3% accuracy and measured at V_{DD} = 4.5V. Oscillator frequency is subjected to IC lot to lot variation.

FREQUENCY AGAINST VDD STABILITY



TYPICAL APPLICATIONS

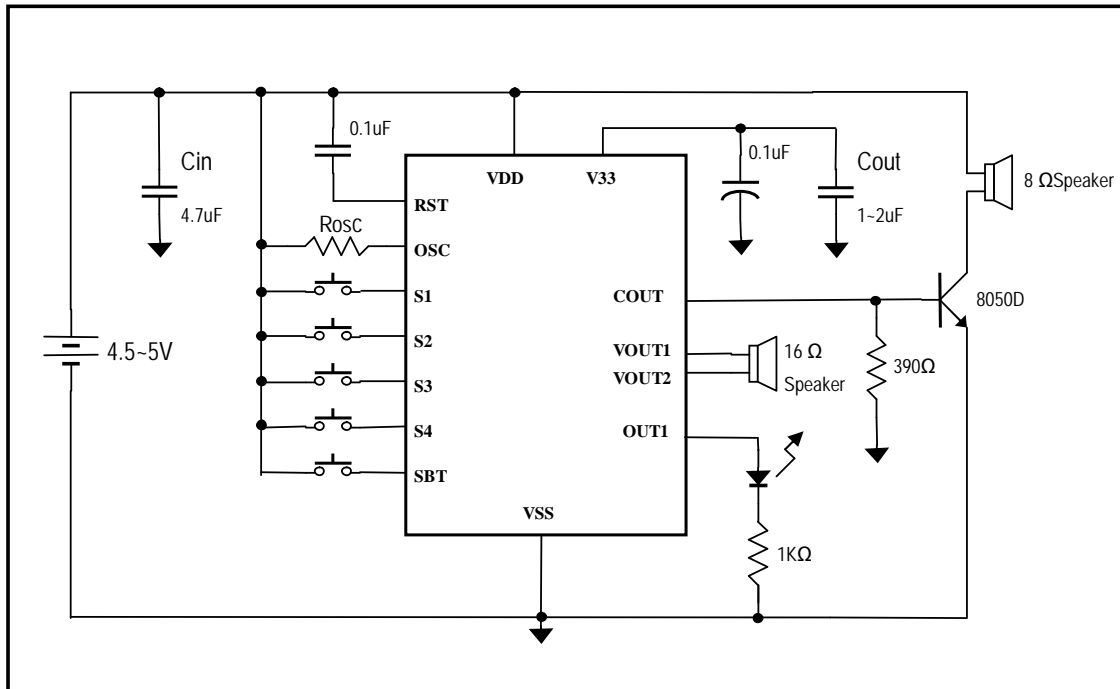


Fig. 12 Using 4.5V Battery

Note 1: Two capacitors C_{in} and C_{out} must be connected from VDD and V33 pins to VSS to stabilize the power supply to the chip. When small capacity battery, e.g. AG10, is used, C_{in} and C_{out} may need to be as large as 22uF. However, if C_{in} and C_{out} is too large, the power-up reset generated by 0.1uF at the RST pin may not be function because it takes longer time for both C_{in} and C_{out} to discharge.

Note 2: 16 Ohm speaker will provide louder and better sound quality when the VOUT speaker direct drive is used.

Note 3: The value of the 390 Ohm base resistor should be modified according to different Vdd value, the kind of speaker and NPN transistor.

Note 4: The VPP pin should be leave unconnected for playback.

BONDING PADS

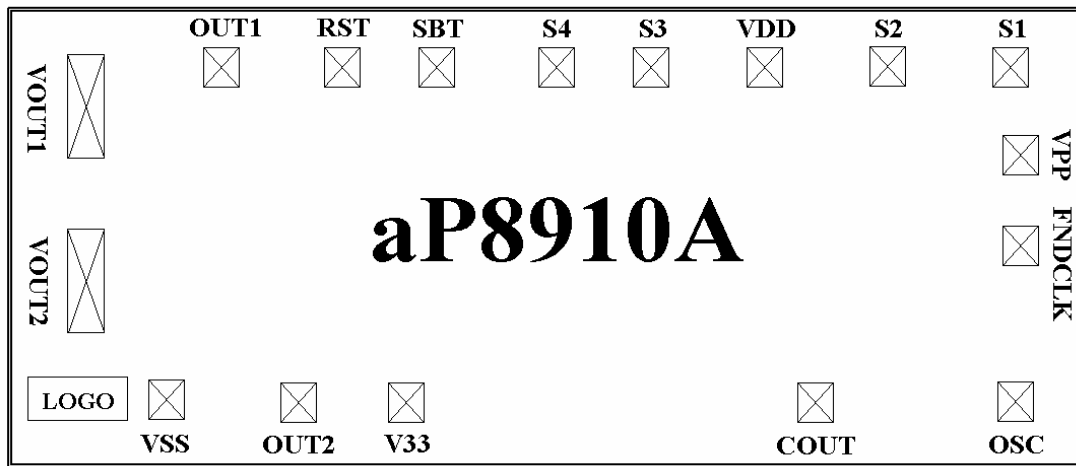
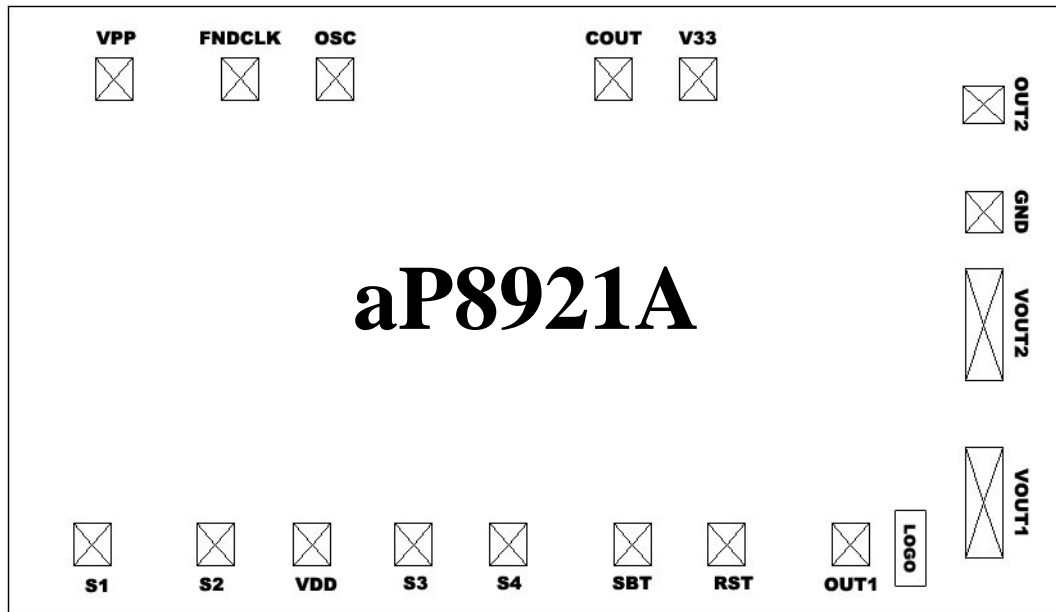


Fig. 12 Pad Locations

Notes:

1. VPP pad should be not connected during voice playback.
2. Substrate should be connected to the Power GND.