N- and P-Channel Quad Power MOSFET Arrays

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS\ (ON)}$ (max) Q1 + Q2 or Q3 + Q4	$V_{GS\ (th)}$ (max)		Order Number / Package
		N-Channel	P-Channel	14-Pin P-Dip
40V	3.0Ω	2.0V	-3.0V	VQ3001N6
20V	3.0Ω	2.0V	-3.0V	VQ7254N6

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices
- ☐ Low threshold version available

Advanced DMOS Technology

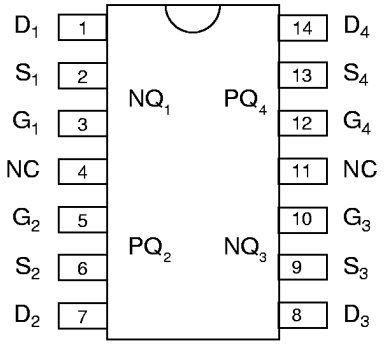
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Telecom switches
- ☐ Logic level interfaces
- ☐ Battery operated systems
- ☐ Photo voltaic drives
- ☐ Soild state relays
- ☐ Motor controls

Pin Configuration



top view
14-pin DIP

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)†		I_D (pulsed)†		Power Dissipation*	θ_{jc}	θ_{ja}	I_{DR}		I_{DRM}†	
	N	P	N	P	@ T_C = 25°C	°C/W	°C/W	N	P	N	P
Plastic Dip	1.4A	-0.65A	3.0A	-3.0A	1.5W	83.3	41.6	1.4A	-0.65A	3.0A	-3.0A

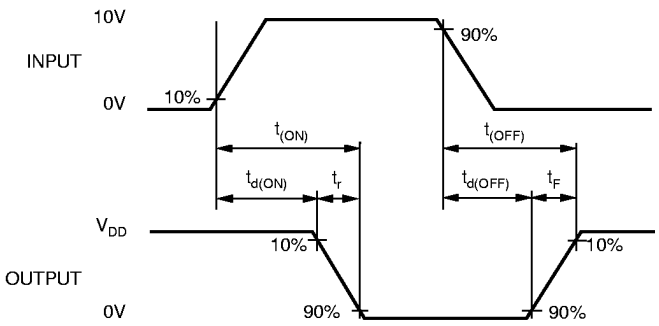
* Total for 4 die.
† Each die.

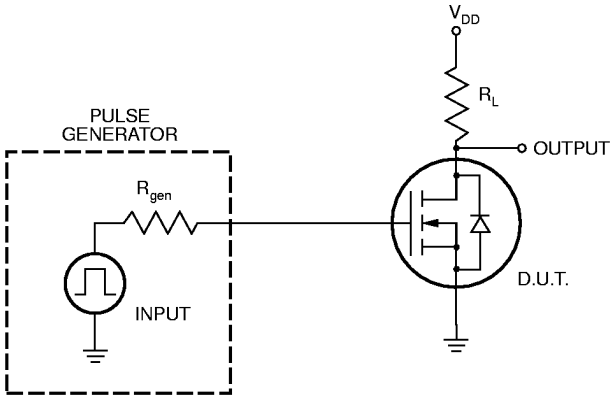
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		N-Channel Min	N-Channel Max	P-Channel Min	P-Channel Max	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VQ3001	40		-40		V	V_{GS} = 0V, I_D = 10µA
		VQ7254	20		-20			
$V_{GS(th)}$	Gate Threshold Voltage	VQ3001	0.8	2.5	-0.8	-4.5	V	V_{GS} = V_{DS}, I_D = 1mA T_A = 25°C
		VQ7254						
		VQ7254	0.65		-0.65		V	V_{GS} = V_{DS}, I_D = 1mA T_A = 85°C
I_{GSS}	Gate Body Leakage			100		-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			10		-10	µA	V_{GS} = 0V, V_{DS} = 0.8 Min. Rating
				500		-500	µA	V_{GS} = 0V, V_{DS} = 0.8 Min. Rating, T_A = 125°C
$V_{DS\ (ON)}$	Total Static Drain-to-Source ON-State Voltage	VQ3001		1.0		-2.0	V	V_{GS} = 11.4V, I_D = 1A
		TQ3001						
		VQ7254		1.0		-2.0		
$R_{DS\ (ON)}$	Total Static Drain-to-Source ON-State Resistance	VQ3001		1.0		2.0	Ω	V_{GS} = 11.4V, I_D = 1A
		TQ3001						
		VQ7254		1.0		2.0		
G_{FS}	Forward Transconductance		200		200		m℧	V_{DS} = 10V, I_D = 0.5A
C_{ISS}	Input Capacitance			190		195	pF	V_{GS} = 0V, V_{DS} = 20V f = 1Mz
C_{OSS}	Output Capacitance			110		120		
C_{RSS}	Reverse Transfer Capacitance			50		60		
$t_{(ON)}$	Turn-ON Time			30		30	ns	V_{DD} = 15V, I_D = 0.65A, R_{GEN} = 25Ω
$t_{(OFF)}$	Turn-OFF Time			30		30	ns	
V_{SD}	Forward ON Voltage	VQ7254		1.8		-2.0	V	V_{GS} = 0V, I_F = 1.5A
		VQ3001		1.8		-2.0		V_{GS} = 0V, I_F = 1.5A

Notes:
1. All D.C. parameters 100% tested (pulse test: 300µs pulse, 2% duty cycle).
2. All A.C. parameters sample tested.
3. Refer to device types TN06L and TP06L for characteristic curves.

Switching Waveforms and Test Circuit





FET polarity in test circuit is N-channel only.