CAT24C03/05

2-Kb and 4-Kb I²C Serial EEPROM with Partial Array Write Protection

FEATURES

- **Supports Standard and Fast I²C Protocol**
- **1.8 V to 5.5 V Supply Voltage Range**
- **16-Byte Page Write Buffer**
- **Hardware Write Protection for upper half of memory**
- **Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA).**
- **Low power CMOS technology**
- **1,000,000 program/erase cycles**
- **100 year data retention**
- **Industrial temperature range**
- **RoHS-compliant 8-lead PDIP, SOIC, and TSSOP, 8-pad TDFN and 5-lead TSOT-23 packages.**

For Ordering Information details, see page 17.

DEVICE DESCRIPTION

The CAT24C03/CAT24C05 is a 2-kb/4-kb CMOS Serial EEPROM device organized internally as 16/32 pages of 16 bytes each, for a total of 256x8/512x8 bits. These devices support both Standard (100kHz) as well as Fast (400kHz) I²C protocol.

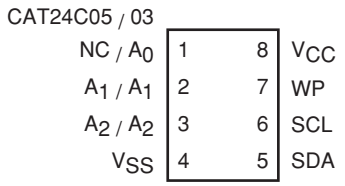
Data is written by providing a starting address, then loading 1 to 16 contiguous bytes into a Page Write Buffer, and then writing all data to non-volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

Write operations can be inhibited for upper half of memory by taking the WP pin High.

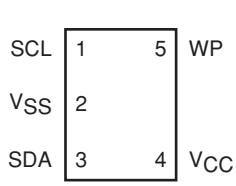
External address pins make it possible to address up to eight CAT24C03 or four CAT24C05 devices on the same bus.

PIN CONFIGURATION

PDIP (L)
SOIC (W)
TSSOP (Y)
TDFN (VP2)



TSOT-23 (TD)

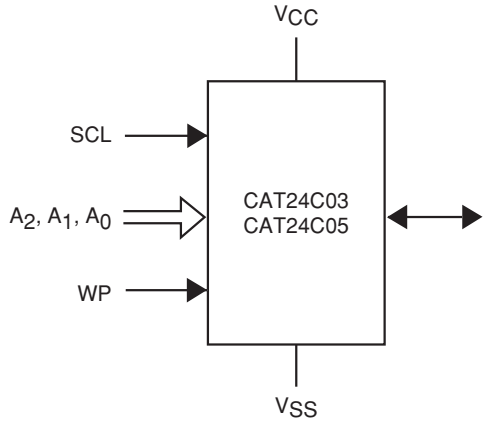


For the location of Pin 1, please consult the corresponding package drawing.

PIN FUNCTIONS

A_0, A_1, A_2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connect

FUNCTIONAL SYMBOL



* Catalyst carries the I²C protocol under a license from the Philips Corporation.

Doc. No. 1116, Rev. B

ABSOLUTE MAXIMUM RATINGS[1]

Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground[2]	-0.5 V to +6.5 V

RELIABILITY CHARACTERISTICS[3]

Symbol	Parameter	Min	Units
N_{END}[4]	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz		1	mA
I_{CCW}	Write Current	Write, f_{SCL} = 400 kHz		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		1	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		1	μA
V_{IL}	Input Low Voltage		-0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq$ 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Max	Units
C_{IN}[3]	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN}[3]	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}[5]	WP Input Current	$V_{IN} < V_{IH}$, V_{CC} = 5.5 V	200	μA
		$V_{IN} < V_{IH}$, V_{CC} = 3.3 V	150	
		$V_{IN} < V_{IH}$, V_{CC} = 1.8 V	100	
		$V_{IN} > V_{IH}$	1	

Note:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Page Mode, V_{CC} = 5 V, 25°C

(5) When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull-down reverts to a weak current source.

A.C. CHARACTERISTICS[1]

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C.

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		µs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of SCL Clock	4		0.6		µs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		µs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F[2]	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		µs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	µs
t_{DH}	Data Out Hold Time	100		100		ns
T_i[2]	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		µs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		µs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU}[2, 3]	Power-up to Ready Mode		1		1	ms

Note:

(1) Test conditions according to “A.C. Test Conditions” table.

(2) Tested initially and after a design or process change that affects this parameter.

(3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

POWER-ON RESET (POR)

The CAT24C03/05 incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The CAT24C03/05 device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

PIN DESCRIPTION

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

WP: The Write Protect input pin inhibits the write operations for upper half of memory, when pulled HIGH. When not driven, this pin is pulled LOW internally.

FUNCTIONAL DESCRIPTION

The CAT24C03/05 supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C03/05 acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

I^2C BUS PROTOCOL

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 1). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. For normal Read/Write operations, the first 4 bits of the Slave address are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices and/or as internal address bits. The last bit of the slave address, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed. The 3 address space extension bits are assigned as illustrated in Figure 2. A_2, A_1 and A_0 must match the state of the external address pins, and a_8 (CAT24C05) is internal address bit.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 3). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 4.

Figure 1. START/STOP Conditions

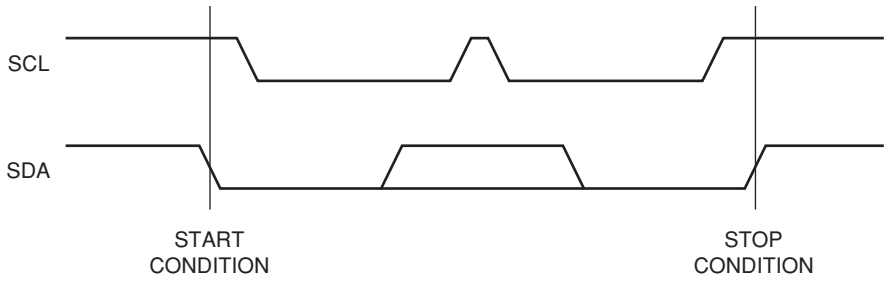


Figure 2. Slave Address Bits

1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$	CAT24C03
1	0	1	0	A_2	A_1	a_8	R/$\overline{W}$	CAT24C05

Figure 3. Acknowledge Timing

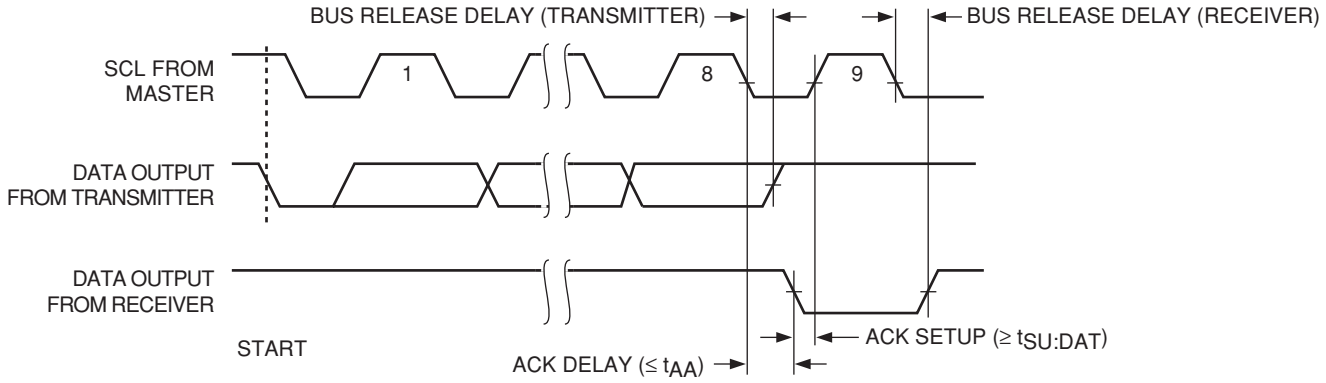
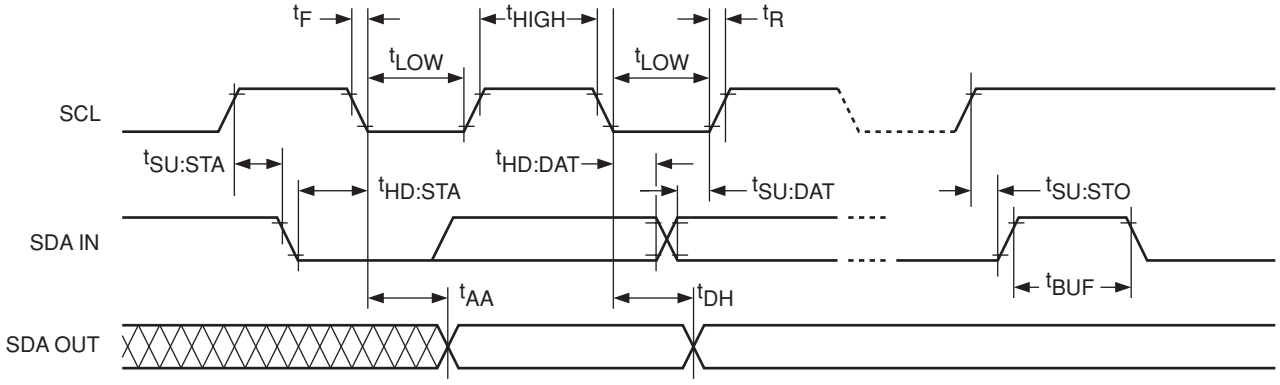


Figure 4. Bus Timing



WRITE OPERATIONS

Byte Write

In Byte Write mode, the Master sends the START condition and the Slave address with the R/$\overline{W}$ bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C03/05. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAT24C03/05 device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 5). While this internal cycle is in progress (t_{WR}), the SDA output will be tri-stated and the CAT24C03/05 will not respond to any request from the Master device (Figure 6).

Page Write

The CAT24C03/05 writes up to 16 bytes of data in a single write cycle, using the Page Write operation (Figure 7). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT24C03/05 will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter 'wraps around' to the beginning of page and previously transmitted data will be overwritten. Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAT24C03/05 in a single write cycle.

Acknowledge Polling

The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C03/05 initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C03/05 is still busy with the write operation, NoACK will be returned. If the CAT24C03/05 has completed the internal write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Hardware Write Protection

With the WP pin held HIGH, the upper half of memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C03/05. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 8). If the WP pin is HIGH during the strobe interval, the CAT24C03/05 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24C03/05 is shipped erased, i.e., all bytes are FFh.

Figure 5. Byte Write Sequence

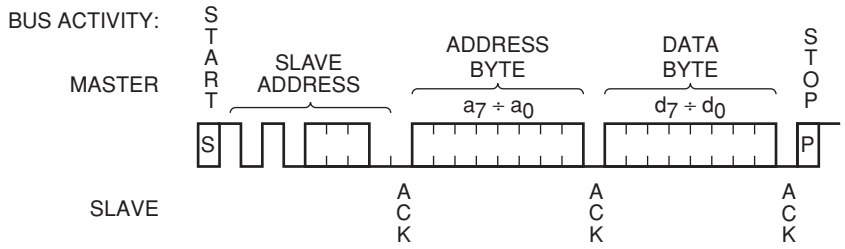


Figure 6. Write Cycle Timing

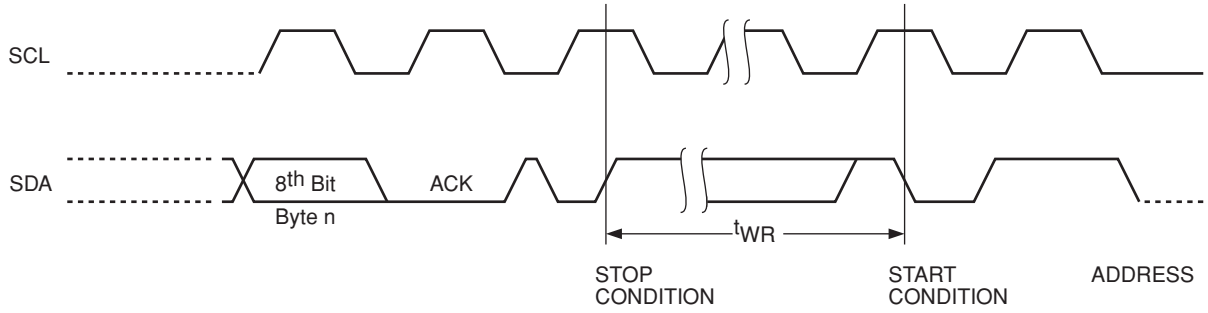


Figure 7. Page Write Sequence

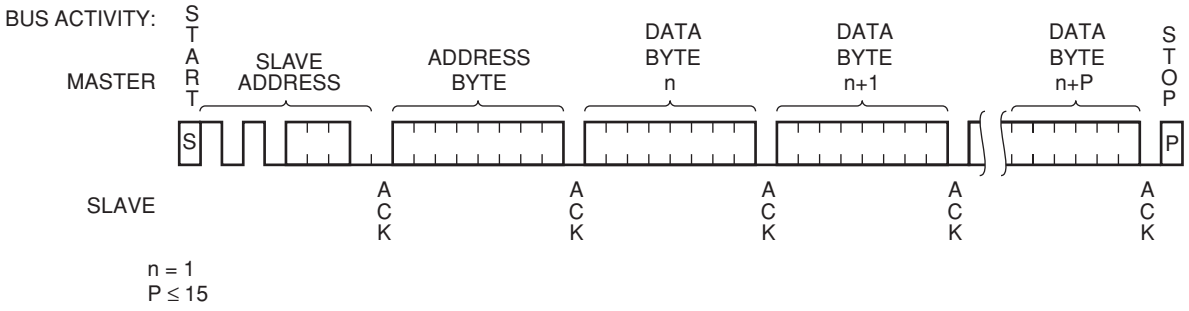
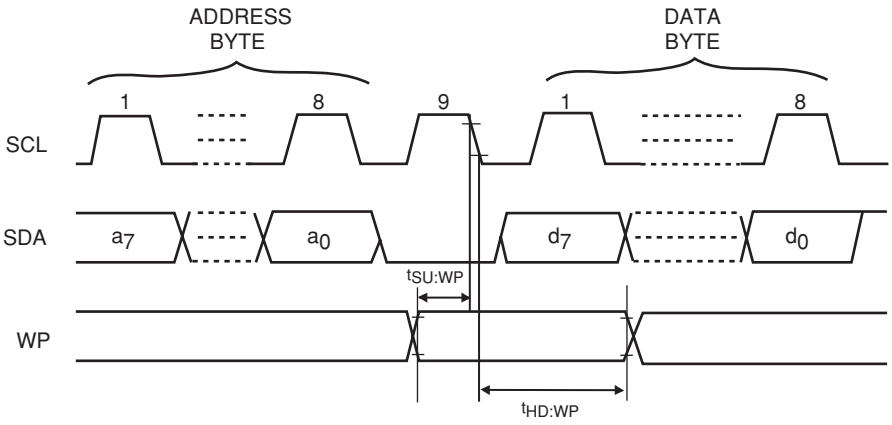


Figure 8. WP Timing



READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/$\overline{W}$ bit set to '1', the CAT24C03/05 will interpret this as a request for data residing at the current byte address in memory. The CAT24C03/05 will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 9), the CAT24C03/05 returns to Standby mode.

Selective Read

Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C03/05 acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C03/05 then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 10).

Sequential Read

If during a Read session, the Master acknowledges the 1st data byte, then the CAT24C03/05 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 11). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

Figure 9. Immediate Read Sequence and Timing

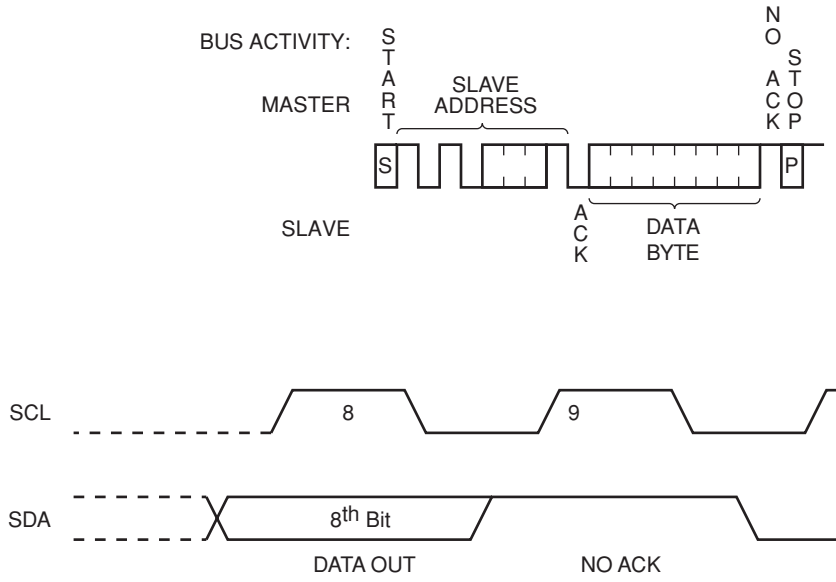


Figure 10. Selective Read Sequence

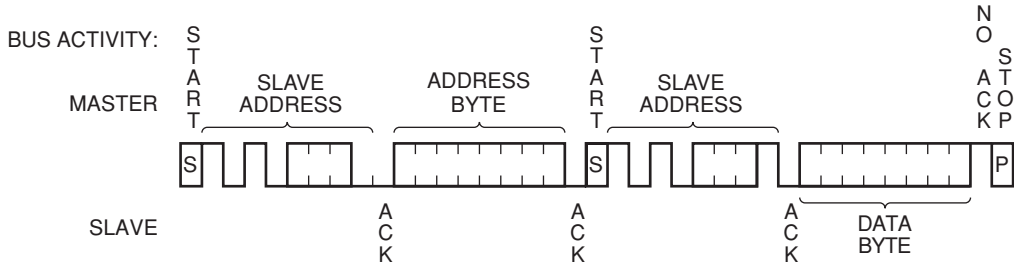
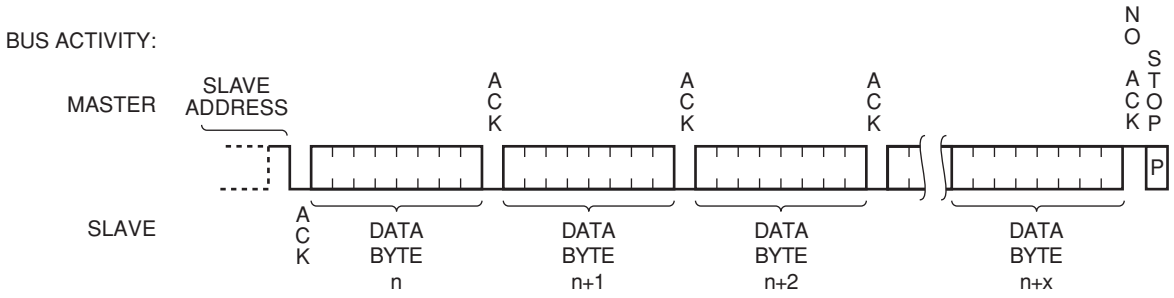
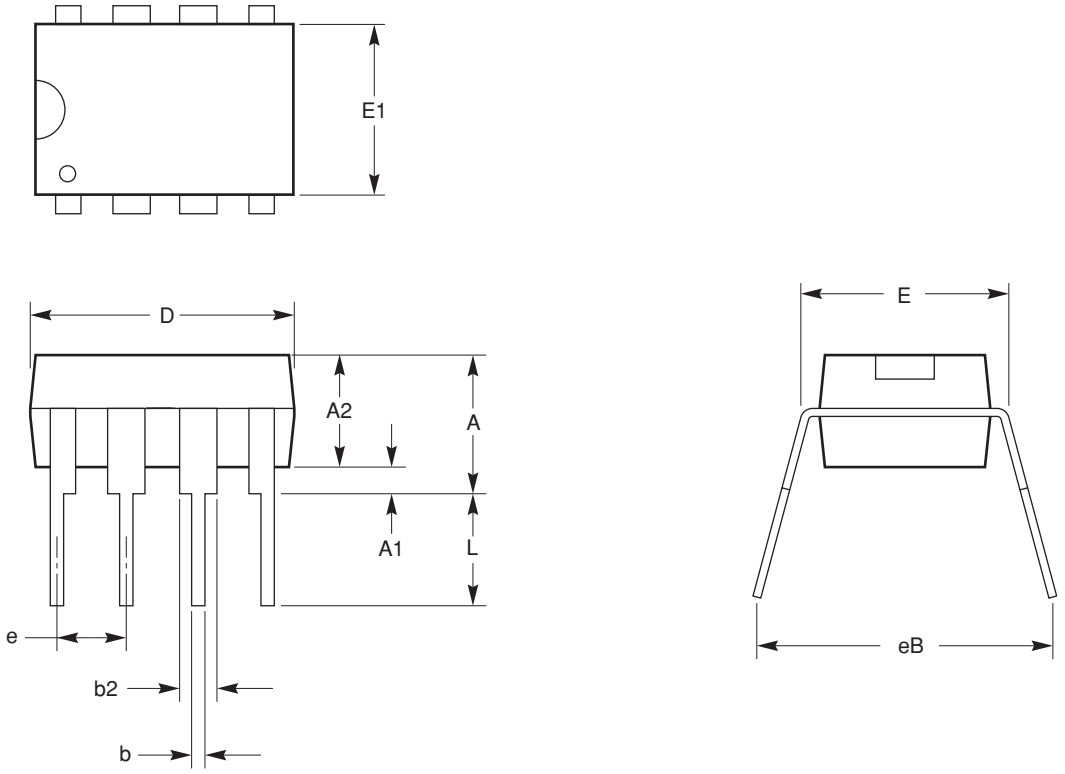


Figure 11. Sequential Read Sequence



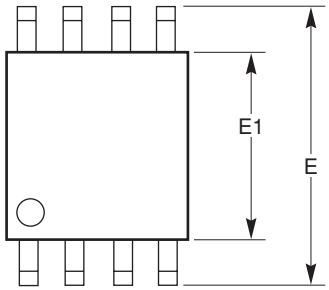
8-LEAD 300 MIL WIDE PLASTIC DIP (L)

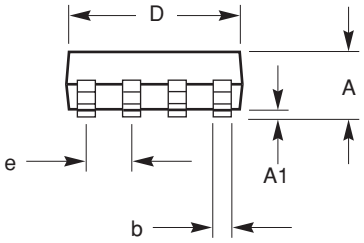


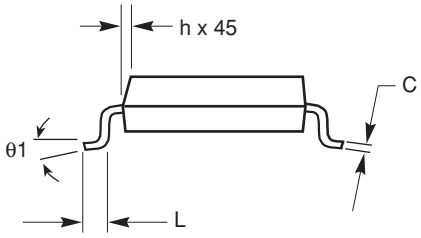
SYMBOL	MIN	NOM	MAX
A			4.57
A1	0.38		
A2	3.05		3.81
b	0.36	0.46	0.56
b2	1.14		1.77
D	9.02		10.16
E	7.62	7.87	8.25
E1	6.09	6.35	7.11
e		2.54 BSC	
eB	7.87		9.65
L	0.115	0.130	0.150

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MS001.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982

8-LEAD 150 MIL WIDE SOIC (W)





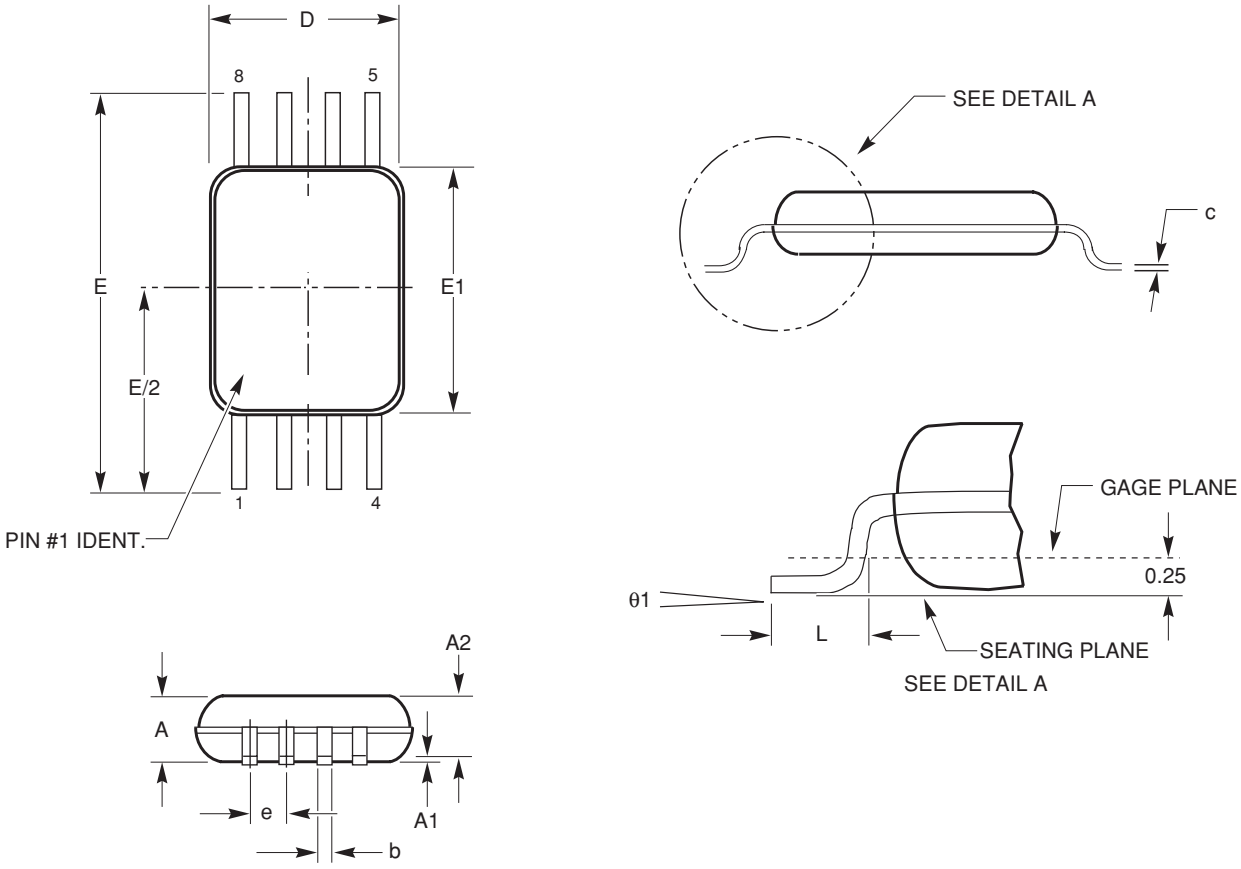


SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ1	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MS-012 dimensions.

8-LEAD TSSOP (Y)

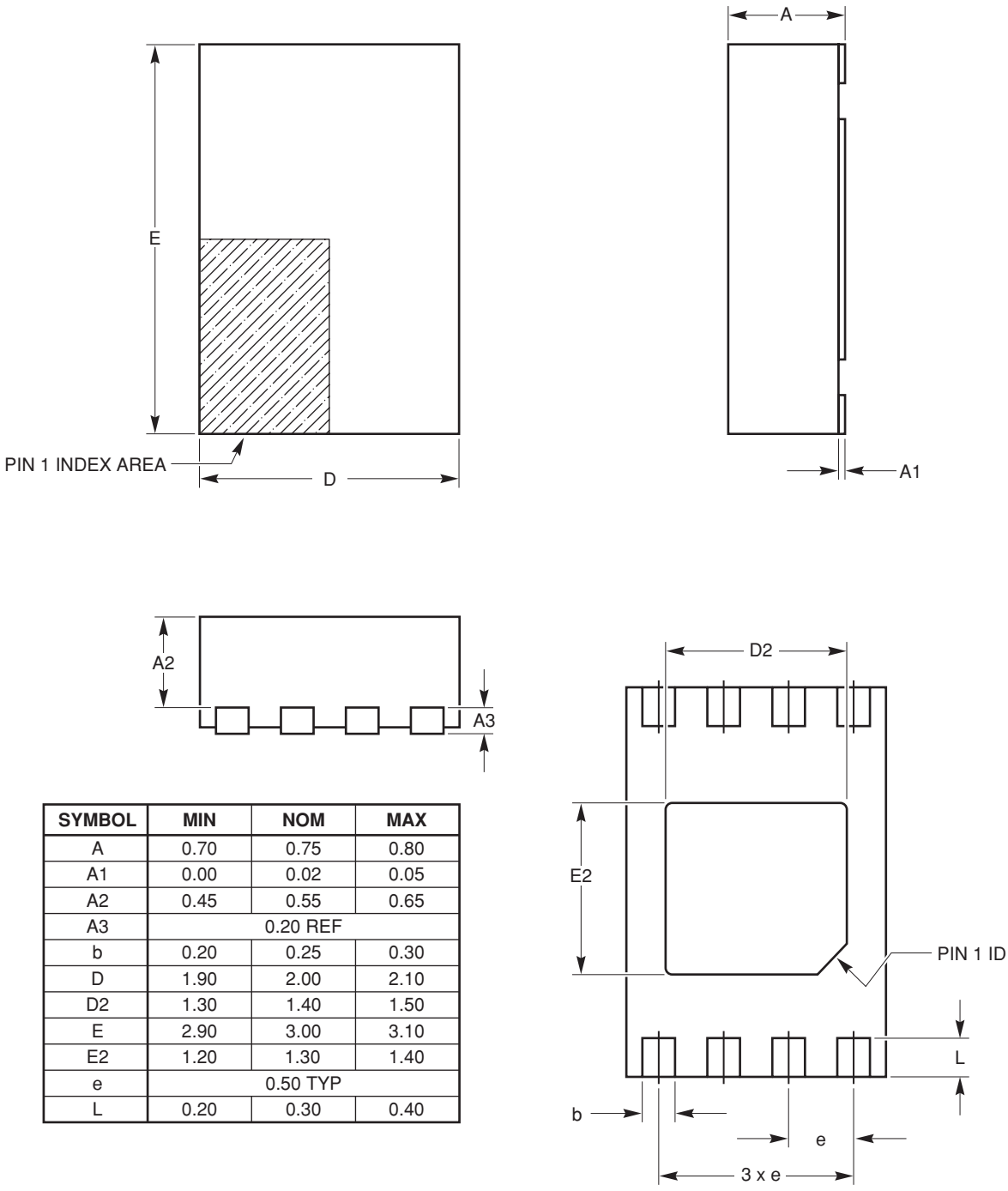


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.4	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.75
θ1	0.00		8.00

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-153.

8-PAD TDFN 2X3 PACKAGE (VP2)

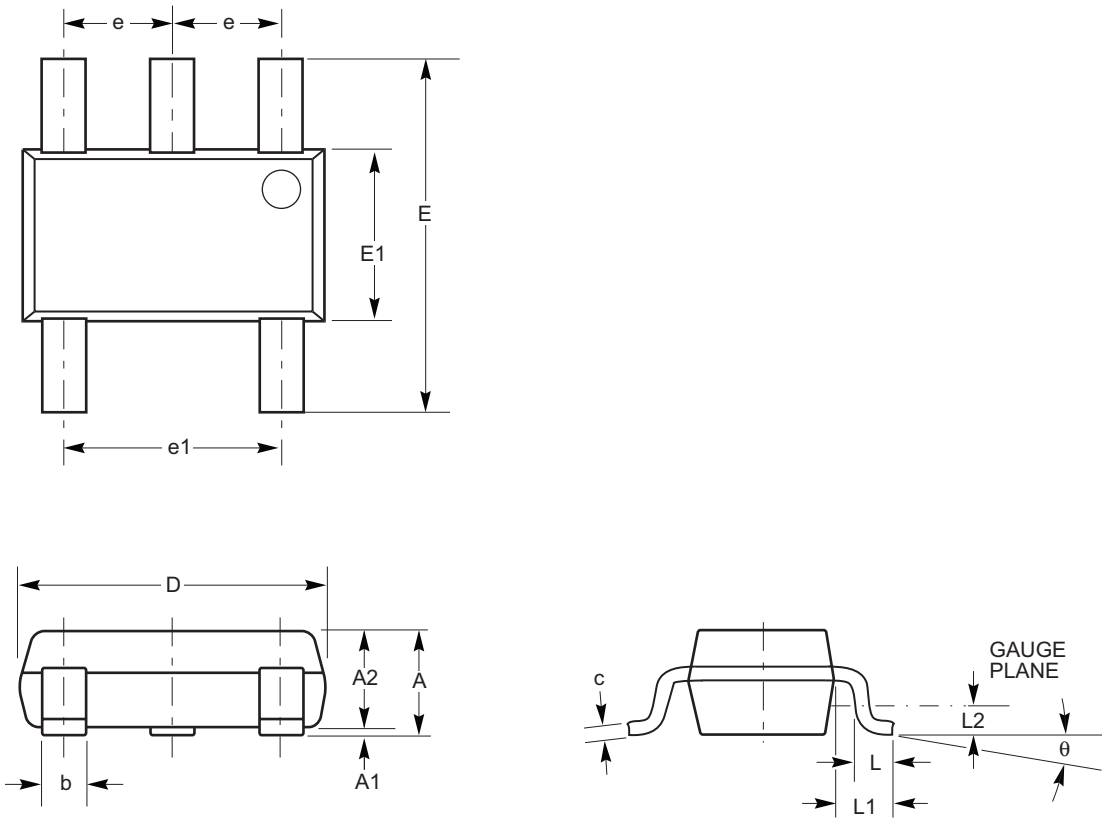


SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-229.

5-Lead TSOT-23 (TD)



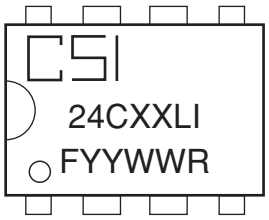
SYMBOL	MIN	NOM	MAX
A	—	—	1.0
A1	0.01	0.05	0.1
A2	0.80	0.87	0.9
b	0.30	—	0.45
c	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 BSC	
e1		1.90 BSC	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	
θ	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-193.

PACKAGE MARKING

8-Lead PDIP



CSI = Catalyst Semiconductor, Inc.
XX = Device Code (see Marking Code table below)
I = Temperature Range
YY = Production Year
WW = Production Week
R = Product Revision (see Marking Code table below)
F = Lead Finish
4 = NiPdAu
3 = Matte-Tin

8-Lead SOIC

CSI = Catalyst Semiconductor, Inc.
XX = Device Code (see Marking Code table below)
I = Temperature Range
YY = Production Year
WW = Production Week
R = Product Revision (see Marking Code table below)
F = Lead Finish
4 = NiPdAu
3 = Matte-Tin

8-Lead TSSOP

Y = Production Year
M = Production Month
R = Die Revision (see Marking Code table below)
XX = Device Code (see Marking Code table below)
I = Temperature Range
WW = Production Week
F = Lead Finish
4 = NiPdAu
3 = Matte-Tin

Marking Codes

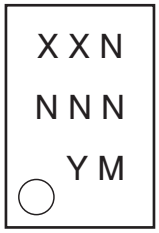
	Device Code **XX**	Product Revision **R**
24C03	03	G
24C05	05	J

Note:

(1) The circle on the package marking indicates the location of Pin 1.

PACKAGE MARKING

8-Pad TDFN



XX = Device Code

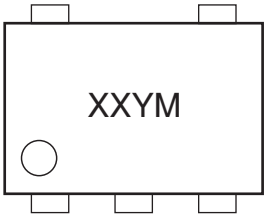
	Matte-Tin	NiPdAu
24C03 Rev. G	FA	EM
24C05 Rev. J	FB	EN

N = Traceable Code

Y = Production Year

M = Production Month

5-Lead TSOT



XX = Device Code

	Matte-Tin	NiPdAu
24C03 Rev. G	RK	RH
24C05 Rev. J	RL	RJ

Y = Production Year

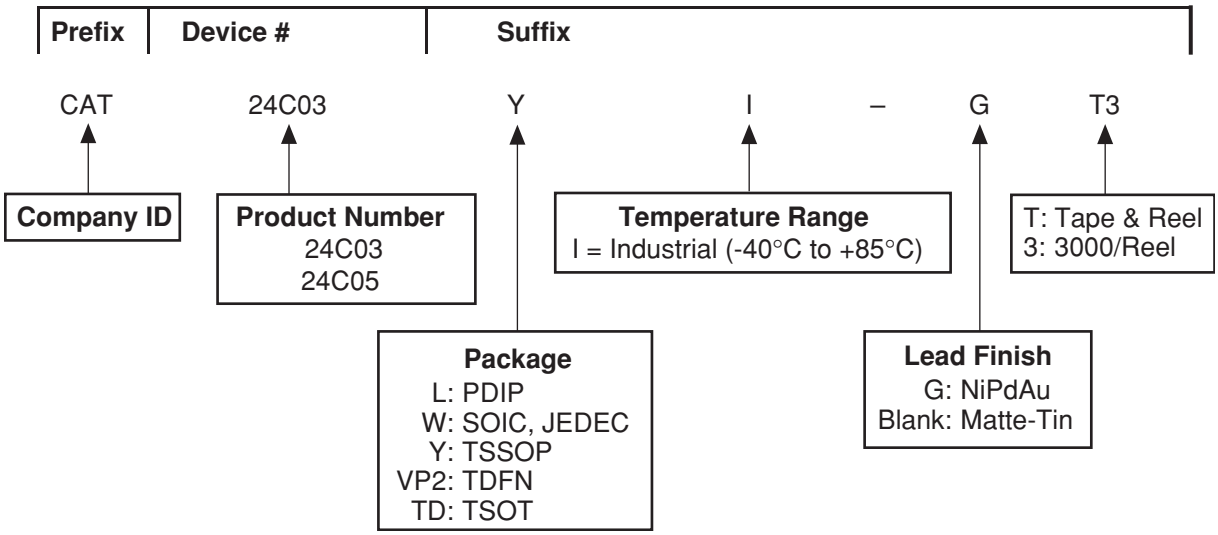
M = Production Month

Notes:

(1) The circle on the package marking indicates the location of Pin 1.

(2) For TDFN and TSOT packages, the Product Revision marking is included in the Device Code (XX).

EXAMPLE OF ORDERING INFORMATION



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu pre-plated (PPF) lead frames.

(3) The device used in the above example is a CAT24C03YI-GT3 (TSSOP, Industrial Temperature, NiPdAu, Tape & Reel).

(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Document Revision	Comments
03/08/06	Doc# 1113 Rev. A Doc# 1114 Rev. A	CAT24CAT03 Data Sheet initial issue CAT24CAT05 Data Sheet initial issue
07/24/06	Doc# 1116 Rev. A	Combine CAT24C03 and CAT24C05 data sheets into one data sheet. Update marking and ordering information.
08/01/06	Doc# 1116 Rev. B	Update Package Marking

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