AMD-766™

Peripheral Bus Controller

Data Sheet

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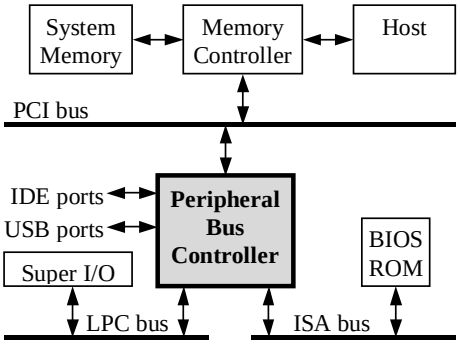
1 Overview

The AMD-766 peripheral bus controller™ is an integrated circuit (IC), developed by AMD, to be the system Southbridge component of personal computer chipsets. The AMD-766 peripheral bus controller (*the IC*) connects to a host memory controller through the PCI bus.

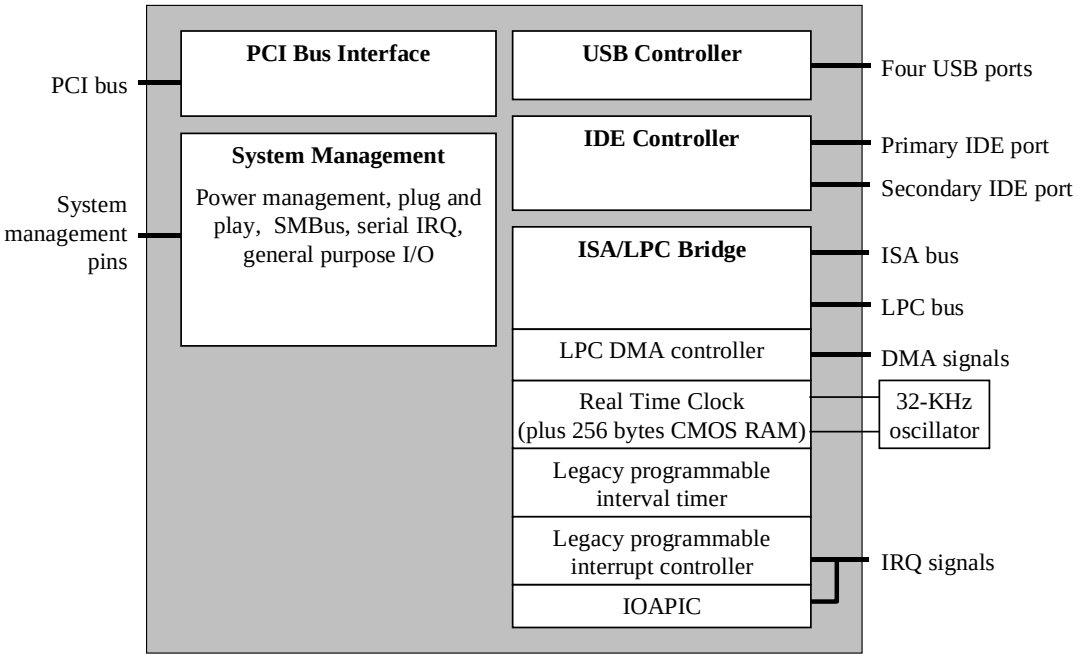
1.1 Features

- PCI interface (PCI specification revision 2.2 compliant).
- LPC bus to connect peripherals such as super IO and BIOS.
- Partial ISA bus.
  - 8 bits wide.
  - Support for Flash BIOS.
- Enhanced IDE controller.
  - Support for two dual-drive ports.
  - PIO modes 0-4.
  - Multi-word DMA.
  - UDMA modes up to ATA-100.
- OHCI-based USB host controller with support for four ports.
- Serial IRQ protocol.
- ACPI-compliant power management logic.
  - Programmable C2, C3, power-on-suspend, suspend to RAM, suspend to disk, and soft off states.
  - Throttling.
  - Hardware traps.
  - System inactivity timer.
- 32 general-purpose IO (GPIO) pins (some are multiplexed with other hard-wired functions).
- Privacy/security logic (ROM access control).
- Legacy logic.
  - Programmable interrupt controller.
  - Programmable interval timer.
  - DMA controller (for LPC bus).
  - Legacy ports.
- IOAPIC controller.
- Real-time clock.
  - 256 bytes of CMOS RAM.
  - Battery-powered.
  - ACPI-compliant extensions.
- SMBus controller with one SMBus port.
- 272-pin BGA package.
- 3.3-volt core and output drivers; 5-volt tolerant input buffers.

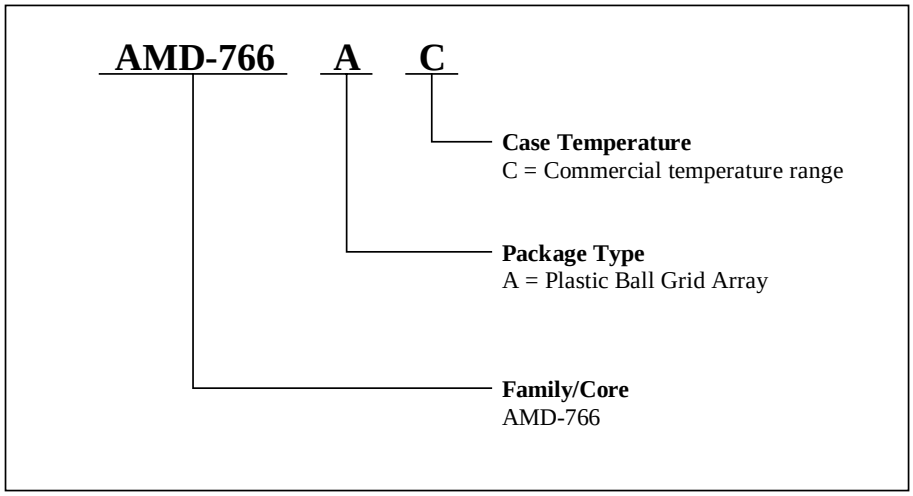
The IC is intended to fit into the traditional Southbridge position on PC-compatible platforms.



Block diagram of the IC:



2 Ordering Information



3 Signal Descriptions

3.1 Terminology

See section 5.1.2 for a description of the register naming conventions used in this document. See section 4.6.1.5 for a description of the system power states: MOFF, SOFF, STD, STR, POS, C3, C2, and FON. See section 3.9 for a description of the power planes. See section 4.1.1 for a description of the types of resets.

Signals with a # suffix are active low.

Note: All inputs are 5-volt tolerant except analog pins and as noted in the pin descriptions.

Signals described in this chapter utilize the following IO cell types:

Name	Notes
Input	Input signal only.
Output	Output signal only. This includes outputs that are capable of being in the high-impedance state.
OD	Open drain output. These pins are driven low and designed to be pulled high by external circuitry.
IO	Input or output signal.
IOD	Input or open-drain output.
w/H	With hysteresis on the input (applied with other signal types).
-PU	Pull up included (applied with other signal types). An internal pull-up resister is provided to the line. These pull-ups are enabled by C3A48. The resistors vary over process, voltage and temperature from 3400 to 7150 ohms.
-PD	Pull down included (applied with other signal types). An internal pull-down resister is provided to the line. These pull-downs are enabled by C3A48. The resistors vary over process, voltage and temperature from 3400 to 7150 ohms.
Analog	Analog signal.

The following provides definitions and reference data about each of the IC's pins. "During Reset" provides the state of the pin while the pin's power plane is being reset (while RESET# is low for the main power plane; while the internal RST_SOFT signal is asserted for the VDD_AUX power plane). "After Reset" provides the state of the pin immediately after that reset. "During POS" provides the state of the pin while in the power on suspend system sleep states. "During S3:S5" provides the state of the pin while in the suspend to disk, suspend to RAM, or soft off system sleep states. "Func" means that the signal is active or functional, operating per its defined function. "Last State" indicates that the signal remains in the state that it was in when the system entered POS.

3.2 PCI Interface

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
AD[31:0]. Address-data bus.	IO	VDD3	3-state	3-state	3-state
CBE_L[3:0]. Command-byte enable bus.	IO	VDD3	3-state	3-state	3-state
DEVSEL#. Device select.	IO-PU	VDD3	3-state	3-state	3-state
FRAME#. Frame signal.	IO-PU	VDD3	3-state	3-state	3-state
IDSEL. Identification select signal.	Input	VDD3	-	-	-
IRDY#. Master ready signal.	IO-PU	VDD3	3-state	3-state	3-state
PAR. Parity signal.	Output	VDD3	3-state	3-state	3-state
PCIRST#. PCI reset. This is the system reset signal for logic that is powered by the system's main power supplies.	Output	VDD_ SOFT	Low	High	High
PCLK. 33 MHz PCI clock. This is required to remain active during reset and when the IC enters the power-on suspend state (POS).	Input	VDD3	-	-	-
PGNT#. Master grant signal.	Input	VDD3	-	-	-
PIRQ[A, B, C, D]#. PCI interrupt requests. Only PIRQD# is an output as well as an input; it may be driven active by the USB interrupt. The other three pins are inputs only.	IOD-PU	VDD3	-	-	-
PREQ#. Master request signal.	Output	VDD3	High	High	High
SERR#. PCI system error signal. This may be asserted by the system to indicate a system error condition. If enabled by RTC70[7], an NMI interrupt may be generated.	Input-PU	VDD3	-	-	-
STOP#. Target abort signal.	IO-PU	VDD3	3-state	3-state	3-state
TRDY#. Target ready signal.	IO-PU	VDD3	3-state	3-state	3-state

3.3 Processor Interface

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
A20M#. Address bit[20] mask to the processor. This output is a logical OR of the KA20G pin from the keyboard controller and PORT92[A20EN].	OD	VDD3	3-state	3-state	3-state
CPURST#. CPURST#. Reset to the processor. This is the reset to processor(s). See sections 4.1.1 and 4.6.1.5.1.	OD	VDD3	Low	Func.	3-state
FERR#. Floating-point error from the processor. The processor asserts this signal to indicate a floating-point error has occurred. This is used to create IRQ13 to the PIC and IOAPIC.	Input w/H	VDD3	-	-	-
IGNNE#. Ignore numeric error to the processor.	OD	VDD3	3-state	3-state	3-state
INIT#. Initialization interrupt to the processor.	OD	VDD3	3-state	3-state	3-state
INTR. Interrupt request to the processor.	OD	VDD3	Low	Low	low
NMI. Non-maskable interrupt request to the processor.	OD	VDD3	Low	Low	Low
PICCLK. Interrupt message bus clock for the IOAPIC. This is controlled through C0Ax4B[APICCKS]. During POS, PICCLK may be selected to either be active or forced low by C3A50[APIC_POSEN].	IOD	VDD3	Func.	Func.	
PICD0# and PICD1#. Interrupt message bus data bits 1 and 0 for the IOAPIC.	IOD	VDD3	3-state	3-state	3-state
SMI#. System management interrupt to the processor.	OD	VDD3	3-state	3-state	3-state
STPCLK#. Processor stop-grant request.	OD	VDD3	3-state	3-state	Active
WSC#. Write snoop complete. This signal is used to guarantee the most recent PCI bus writes from the IC to system memory are visible to the host. See section 4.3.2 for more details. This signal requires an external pull-up resistor with a value between 10K to 200K ohms.	IOD	VDD3	3-state	3-state	3-state

3.4 ISA/LPC Bus and Legacy Support Signals

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
BCLK. ISA bus clock. This is the approximately 8 MHz ISA-bus clock. It is the frequency of PCLK divided by four.	Output	VDD3	Func.	Func.	Func.
EKIRQ1. External keyboard controller IRQ1. This is designed to be connected to the keyboard controller's IRQ1 for the internal interrupt controller logic.	Input	VDD3	Input	Input	Func.
EKIRQ12. External keyboard controller IRQ12 mouse interrupt. This is designed to be connected to the keyboard controller's IRQ12 for the internal interrupt controller logic. See C3A46[10:9] for information on how the IRQ12 pin and the mouse interrupt are combined.	Input	VDD3	Input	Input	Func.
IOCHK#. ISA bus IO channel check signal. The assertion of this signal controls PORT61[IOCHK].	Input-PU	VDD3	-	-	-
IOCHRDY. ISA bus IO channel ready signal. This is deasserted by ISA bus slaves to extend the duration of the cycle.	Input-PU	VDD3	3-state	3-state	3-state
IOR#. ISA bus IO read signal.	Output	VDD3	High	High	High
IOW#. ISA bus IO write signal.	Output	VDD3	High	High	High
IRQ[11:9,7:3]. ISA bus interrupt request signals. REQ[7:0]#. PCI bus master request pins (alternate function to IRQ[11:9, 7:3]; selected by PMF5). These pins may be used to set PM00[BM_STS].	Input-PU	VDD3	-	-	-
IRQ12. ISA bus interrupt request 12. SMBALERT#. SMBus alert (alternate function to IRQ12; selected by C3A46[10:9]). When enabled to do so, this may be used to generate an SMI or SCI interrupt associated with the SMBus logic. USBOC1#. USB over current detect 1 (alternate function to IRQ12; selected by C3A46[10:9]). When enabled to do so, this may be routed to the USB block to be a second source of USB port over-current detection.	Input	VDD3	-	-	-
IRQ[15,14]. Input; ISA bus interrupt request signals. NMPIRQ. Native mode primary IDE port IRQ (alternate function to IRQ14; selected by C1A08[8]). When C1A08[8] is high, this pin becomes an active-high, shared interrupt that is logically combined with PIRQA# such that it may be shared with other PCI devices. This is in support of native mode as defined by the *PCI IDE Controller Specification*. NMSIRQ. Native mode secondary IDE port IRQ (alternate function to IRQ15; selected by C1A08[10]). When C1A08[10] is high, this pin becomes an active-high, shared interrupt that is logically combined with PIRQA# such that it may be shared with other PCI devices. This is in support of native mode as defined by the *PCI IDE Controller Specification*.	Input-PU	VDD3	-	-	-
ISABIOS. Direct BIOS accesses to the ISA bus versus the LPC bus. The state of this pin may be accessed in C3A48[ISABIOS]. 1=The ISA bus. 0=The LPC bus.	Input	VDD3	Input	Input	Input
KA20G. Keyboard A20 gate. This is designed to be the gate A20 signal from the system keyboard controller. It affects A20M#.	Input	VDD3	Input	Input	Func.
KBRC#. Keyboard reset command. This is designed to be the processor	Input	VDD3	Input	Input	Func.

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
reset signal from the system keyboard controller. When asserted, an INIT interrupt to the processor is generated.					
LA[23:17]. ISA system address bus bits[23:17]. LA[23:17] and SA[16:0] combine to for the 24-bit ISA address bus.	Output	VDD3	Low	Low	Last state
LAD[3:0]. LPC address-data bus.	IO	VDD3	3-state	3-state	3-state
LDRQ0# and LDRQ1#. LPC DMA request signals.	Input	VDD3	-	-	-
LFRAME#. LPC frame signal.	IO	VDD3	High	High	High
MEMR#. ISA bus memory cycle read command.	Output	VDD3	High	High	High
MEMW#. ISA bus memory cycle write command.	Output	VDD3	High	High	High
OSC. 14.31818 MHz. clock. This is used for the programmable interval timer and various power management timers.	Input	VDD3	-	-	-
ROM_KBCS#. ROM chip select and keyboard chip select. This is designed to be connected to both the ISA-bus system ROM BIOS and the keyboard controller. During ISA bus memory accesses this pin decodes ROM BIOS memory space, as defined by C0A43 (if the ISABIOS pin is high). During ISA bus IO cycles to the legacy keyboard controller, this pin decodes accesses to the keyboard controller. The state of this bit is captured during reset in C3A48[3].	IO	VDD3	Input	High	High
SA[16:0]. ISA system address bus bits[16:0]. LA[23:17] and SA[16:0] combine to for the 24-bit ISA address bus.	Output	VDD3	Low	Low	Last state
SD[7:0]. ISA data bus.	IO-PU	VDD3	3-state	3-state	3-state
SPKR. Speaker driver from the programmable interval timer. This pin is an input while PWRGD is low; it is used to select the default state of C3A48[ENIDE, ENPCI, ENISA] (the internal pull-up-pull-down IO pin resister enables).	IO	VDD3	Input	Low	Last state

3.5 Ultra DMA Enhanced IDE Interface

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
DADDR[P,S][2:0]. IDE controller [primary, secondary] port address.	Output	VDD3	Low	Low	Low
DCS1P#. IDE controller primary port chip select 1. This is active during accesses to the IO address space 1F7h – 1F0h.	Output	VDD3	High	High	High
DCS1S#. IDE controller secondary port chip select 1. This is active during accesses to the IO address space 177h – 170h.	Output	VDD3	High	High	High
DCS3P#. IDE controller primary port chip select 3. This is active during accesses to the IO address space 3F7h – 3F4h.	Output	VDD3	High	High	High
DCS3S#. IDE controller secondary port chip select 3. This is active during accesses to the IO address space 377h – 374h.	Output	VDD3	High	High	High
DDACK[P,S]#. IDE controller [primary, secondary] port DMA acknowledge signal.	Output	VDD3	High	High	High
DDATA[P,S][15:0]. IO; IDE controller [primary, secondary] port data bus.	IO	VDD3	3-state	3-state	3-state
DDRQ[P,S]. Input; IDE controller [primary, secondary] port DMA request signal.	Input-PD	VDD3	-	-	-
DIOR[P,S]#. Output; IDE controller [primary, secondary] port IO read command.	Output	VDD3	High	High	High
DIOW[P,S]#. Output; IDE controller [primary, secondary] port IO write command.	Output	VDD3	High	High	High
DRDY[P,S]. Input; IDE controller [primary, secondary] port ready strobe.	Input	VDD3	-	-	-

3.6 System Management Signals

This group includes all the GPIO pins, many of which are multiplexed with other functions. The default function of GPIO pins after reset is specified by PM[FF:F4 and D3:C0]. When programmed as GPIOs, these pins are capable of being programmed to be inputs or push-pull outputs. GPIO pins remain functional during sleep states (if they are powered).

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
C32KHZ. 32.768 kHz clock output. This pin may also be configured as GPIO15 by PMCF.	Output, IO	VDD3	Low	Low	Func.
CACHE_ZZ. Level 2 cache sleep mode output. This is designed to be connected to the power-control input to the second level cache to place it into low-power mode. It is controlled by C3A50. This pin may also be configured as GPIO8 by PMC8.	Output, IO	VDD3	Low	Low	Func.
CPUSLEEP#. Processor non-snoop sleep mode output. This may be connected to the sleep pin of the processor to place it into a non-snoop-capable low-power state. It is controlled by C3A50. This pin may also be configured as GPIO5 by PMC5.	Output, IO	VDD3	High	High	Func.
CPUSTOP#. Processor clock stop output. This may be connected to the system clock chip to control the host clock signals. It is controlled by C3A50. This pin may also be configured as GPIO6 by PMC6.	Output, IO	VDD3	High	High	Func.
DCSTOP#. DRAM controller stop output. This may be connected to the system memory controller to indicate that its clock is going to stop (so that an alternative DRAM refresh scheme may start). It is controlled by C3A50. This signal is also functional during STD, STR and SOFF.	Output, IO	VDD_ AUX	Active	High	Func.
EXTSMI#. External SMI input. This pin may be used to generate SMI or SCI interrupts and resume events. This pin may also be configured as GPIO12 by PMCC.	Input, IO	VDD_ AUX	-	-	-
FLAGRD#. Flag read output. This may be connected to the output-enable input of external buffers with the buffer outputs on the SD pins. Therefore, the inputs to the buffers may be software-readable flags. FLAGRD# is asserted during reads of PM1A. This pin may also be configured as GPIO11 by PMCB.	Output, IO	VDD3	High	High	High
FLAGWR. Flag write output. This may be connected to the latch-enabled input of external latches with the latch inputs on the SD pins. Therefore, the outputs of the latches may be software-controlled flags. FLAGWR is asserted during writes to PM18. This pin may also be configured as GPIO10 by PMCA.	Output, IO	VDD3	Low	Low	Low

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
GPIO[31:17, 9, 2]. General purpose IO pins. See section 4.6.5 for details about these pins. All GPIO pins are configured by PM[FF:F4 and D3:C0] where the default function is specified. GPIO pins remain functional during sleep states. MSIRQ. Mouse interrupt request output (alternate function to GPIO17; selected by PMD1). This is the mouse IRQ from the USB keyboard emulation logic. PNPIRQ[2:0]. Plug and play interrupt request [2:0] inputs (alternate function to GPIO[20:18]; selected by PM[F4, D3, D2]). These may be assigned to control the IRQ signals to the interrupt routing table shown in section 4.3.2. They are controlled by C3A44. BMREQ#. PCI bus master request input (alternate function to GPIO21; selected by PMF5). This is intended to be the OR of the external PCI bus request signals. If this function is selected by PMF5, then it controls the PM00[BM_STS] status bit (if not, then IRQ[11:9, 7:3] are selected to be the PCI REQ# signals). BMREQ# is treated as an asynchronous input. PNPCS[1:0]#. Plug and play chip select [1:0] outputs (alternate function to GPIO[23:22]; selected by PM[F7:F6]). These are programmable chip select for external ISA bus devices. They becomes active during ISA bus cycles to memory space or IO space as specified by C3A46[CS[1:0]MEM and CS[1:0]IO]. They are valid for at least 1 PCLK cycle before and after the ISA-bus command signal (IOR#, IOW#, MEMR#, or MEMW#). PNPCS1#. Output; plug and play chip select 1 (alternate function to GPIO23; selected by PMF7). This is designed to be a programmable chip select to external ISA bus devices. It becomes active during ISA bus cycles to memory space or IO space as specified by C3A46[CS1MEM and CS1IO]. It is guaranteed to be valid before and after the ISA-bus command signal.	IO	VDD3	-	-	Functional
INTIRQ8#. Real time clock interrupt output. This is the interrupt output from the IC's real-time clock. This pin may also be configured as GPIO16 by PMD0. SQWAVE. Square wave clock output (alternate function to INTIRQ8#; selected by PMD0). This is a square wave output, the frequency for which is specified by C3A4E.	Output, IO	VDD3	High	High	Func.
INTRUDER#. Intruder detection. This controls PM46[INTRDR_STS]. This pin is not 5-volt tolerant.	Input	VDD_AL	Input	Input	Input
PCISTOP#. PCI bus clock stop output. This may be used to control the system clock chip to control the PCI bus clock signals. It is controlled by C3A50. This pin may also be configured as GPIO7 by PMC7.	IO	VDD3	High	High	Func.
PME#. Power management interrupt. This pin may be used to generate SMI or SCI interrupts and resume events. It controls PM20[PME_STS].	Input	VDD_AUX	-	-	-
PRDY. Processor ready. When this is asserted, the IC freezes the timers specified by C3A4C.	Input, IO	VDD3	-	-	-
PWRBTN#. Power button. This may be used to control the automatic transition from a sleep state to FON. It controls PM00[PWRBTN_STS]. Also, if it is asserted for four seconds from any state other than SOFF, then	Input	VDD_AUX	-	-	-

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
a power button override event is generated. A power button override event causes the PWRON# pin to be driven high and PM00[PBOR_STS] to be set high. The logic for this pin includes a 16 millisecond debounce circuit; the signal must be stable for about 16 milliseconds before it is detected by the rest of the internal logic.					
PWRGD. Power good. This is required to be low while the VDD3 power plane is not valid, stay low for at least 50 milliseconds after it becomes valid, and then go high. It is the reset source for the VDD3 logic in the IC. The rising edge of this pin is debounced for one to two 32 kHz (RTC) clocks before it is internally detected as being high.	Input w/H	VDD_ AUX	-	-	-
PWRON#. Main power on. This is designed to control the main power supplies to the system board, including the IC's VDD3 plane. It is asserted during the FON, C2, C3, and POS states; it is deasserted during the STR, STD and SOFF states. See section 4.6.1.5 for more details.	OD	VDD_ AUX	Low	Low	Low
RI#. Ring indicate. This pin may be used to generate SMI or SCI interrupts and resume events. It controls PM20[RI_STS]. This pin may also be configured as GPIO14 by PMCE.	Input, IO	VDD_ AUX	-	-	-
RPWRON. RAM power on. This is designed to control power to the system memory power plane. When high, it is expected that power to system memory is enabled. When low, it is expected that power to system memory is disabled. This pin is low during STD and SOFF and high in all other states. See section 4.6.1.5 for more details.	OD	VDD_ AUX	High	High	High
RTCX_IN. Real time clock 32.768 kHz crystal input. This pin is designed to be connected through a crystal oscillator to RTCX_OUT.	Analog	VDD_ AL	Func.	Func.	Func.
RTCX_OUT. Real time clock 32.768 kHz crystal output.	Analog	VDD_ AL	Func.	Func.	Func.
SERIRQ. Serial IRQ function. This pin supports the serial IRQ protocol. Control for this is in C3A4A.	IO	VDD3	-	-	Func.
SLPBTN#. Sleep button. This may be used to control the automatic transition from a sleep state to FON. It controls PM00[SLPBTN_STS]. Also, if it is asserted for four seconds from any state other than SOFF, then a power button override event is generated. A power button override event causes the PWRON# pin to be driven high and PM00[PBOR_STS] to be set high. The logic for this pin includes a 16 millisecond debounce circuit; the signal must be stable for about 16 milliseconds before it is detected by the rest of the internal logic. This pin may also be configured as GPIO3 by PMC3.	Input, IO	VDD_ AUX	-	-	-
SMBUSC. System management bus (SMBus) clock. This pin may also be configured as GPIO0 by PMC0.	I w/H / OD	VDD_ AUX	3-state	3-state	Func.
SMBUSD. System management bus (SMBus) data. This pin may also be configured as GPIO1 by PMC1.	I w/H / OD	VDD_ AUX	3-state	3-state	Func.
SUSPEND#. Suspend output. This may be used during the POS state to control an external power planes. It is controlled by C3A50.	IO	VDD3	High	High	Func.
THERM#. Input; thermal warning detect. This may be used to automatically enable processor throttling as specified by C3A50[TTH_EN, TTH_RATIO]. See section 4.6.1.4 for more details.	IO	VDD3	-	-	Func.

3.7 Universal Serial Bus Interface

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
USBCLK. 48 MHz USB clock.	Input	VDD3	-	-	-
USBOC0#. USB over current detect 0. This is expected to become active to report the occurrence of an over-current condition on the voltage supplied to the USB ports.	Input	VDD3	-	-	-
USBP[3:0], USBN[3:0]. Analog; USB ports. These are four pairs of differential USB signals. USBP[3:0] are the positive signals and USBN[3:0] are the negative signals. These signals go into the high-impedance state during sleep states; internal logic may detect USB resume events while in these states and set the status bit, PM20[USB_RSM_STS].	Analog	VDD_ USB	3-state	3-state	3-state

3.8 Miscellaneous Signals

Pin name and description	IO cell type	Power plane	During Reset	Post Reset	POS
STRAPH[2:0]. These pins should be tied high through a pull-up resistor (to VDD_AUX).	Input	VDD_ AUX	-	-	-
STRAPL[3:0]. These should be grounded on the system board.	Input	VDD3	-	-	-
TEST#. Scan, NAND tree, and high-impedance mode enable. See section 9 for details.	Input	VDD3	-	-	-

3.9 Power And Ground

See section 4.6.1.5 for a description of the system power states. The following power and ground planes are connected to the IC through BGA pins.

VDD3. Main 3.3 volt supply. This plane is required to be valid in the FON and POS power states.

VDD_AUX. Auxiliary 3.3 volt plane. This plane is required to be valid in all system power states except MOFF. The pins powered by these planes are: PWRBTN#, PWRON#, PME#, SMBUS[C,D], EXTSMI#, SLPBTN#, RI#, PWRGD, PCIRST#, RPWRON, DCSTOP#, STRAPH[2:0], STRAPL1. All register bits that are on the VDD_AUX plane are reset by the internal RST_SOFT pulse that is generated for about 30 milliseconds after VDD_AUX becomes valid.

VDD_REF. 5.0 volt reference supply. This plane is required to be valid in all power states except MOFF. It is expected that this plane is connected to a 5-volt power supply that is active in the SOFF (soft off) power state, i.e., the 5-volt version of VDD_AUX from the power supply is required for this pin.

VDD_RTC. Real-time clock 3.3 volt supply. This plane is required to be valid in all power states. It is typically powered by a battery. It supplies power for the internal VDD_AL power plane when VDD_AUX is not valid.

VDD_USB. 3.3 volt supply filtered for the USB transceivers. This plane is required to be valid in all power states except MOFF.

VSS. Main ground plane.

VSS_USB. Ground plane filtered for the USB transceivers.

The IC also includes the following internal power plane.

VDD_AL. VDD always. This is an internal plane. It is supplied by VDD_AUX when that plane is valid or by VDD_RTC when VDD_AUX is not valid. VDD_AL powers the real-time clock and some system management circuitry. The pins powered by VDD_AL are: RTCX_IN, RTCX_OUT, INTRUDER#.

4 Functional Operation

The IC connects to the host memory controller through PCI bus interface as described in section 1.1.

The IC supports processor accesses to BIOS on either the ISA bus or the LPC bus as specified by the ISABIOS pin.

See section 5.1 for details about the software view of the IC. See section 5.1.2 for a description of the register naming convention.

4.1 Overview

4.1.1 Resets

The IC generates an internal reset for the VDD_AUX power plane called RST_SOFT. RST_SOFT lasts for about 30 milliseconds after the VDD_AUX plane is greater than 2.5 volts. See section 4.6.1.5.1 for details.

PWRGD is the source of reset for some of the IC's VDD3 logic. From this signal, RESET# and CPURST# are derived. See section 4.6.1.5.1 for details.

It is possible to generate system resets via C0A47[SWPCIR].

Various system resets may be initiated through PORTCF9.

It is also possible to reset the processor (without clearing the cache) with an INIT interrupt through the keyboard controller via KBRC#, the PORT92 register, or from a PCI-defined shutdown special cycle from the host.

4.2 PCI Interface

The IC connects to the host through a 32-bit, 33 MHz PCI interface.

4.2.1 Subtractive Versus Medium Decoding

PCI target accesses to the IC are acknowledged with DEVSEL# using either PCI-defined *medium* or *subtractive* decoding. The following equation specifies the timing based on the address space and configuration. See section 10.3 for a description of the logic convention.

```
START_OF_DEVSEL = (PCI_COMMAND != SPECIAL_CYCLE) &
   (  FRAME3 & ~DEVSEL & (PCI_COMMAND == 2, 3, 6, 7, 12, 14, or 15) &    // subtractive window
              (C0A48[SUB] != 1Xb)
   |  FRAME1 & ~DEVSEL &                                                 // medium window
              ( (PCI_COMMAND == INTERRUPT_ACKNOWLEDGE)
              | ISA_HIT
              | DMAC_HIT       & ~C0A48[DMAEN#]
              | IDE_HIT        & ~C0A48[IDEEN#]
              | USB_HIT        & ~C0A48[IUSBEN#] | CONFIG_SPACE_0
              | CONFIG_SPACE_1 & ~C0A48[IDEEN#]
              | CONFIG_SPACE_4 & ~C0A48[IUSBEN#] | CONFIG_SPACE_3
              | BIOS_ADDR_SPACE) );
```

Where the following are defined:

`CMD2:`	CBE_L[2] after being latched during the address phase of the PCI cycle.
`CONFIG_SPACE[4:0]:`	The latched address for a Config cycle matches the device and function number for one of the IC's configuration spaces, functions 0, 1, 3, and 4.
`FRAME1:`	The pulse after FRAME# is asserted used for medium decoding.
`FRAME3:`	The pulse after FRAME# is asserted used for subtractive decoding.
`IDE_HIT`	PCI address and command targets the IDE controller.
`ISA_HIT`	PCI address and command targets the an internal ISA bus device including the RTC, the PIT, the PIC, the IOAPIC, LPC-decoded addresses, or a legacy register.
`DMAC_HIT`	PCI address and command targets the legacy DMA controller.
`PCI_COMMAND:`	The latched state of the CBE_L[3:0] signals during the address phase of the cycle. 2=IO read; 3=IO write; 6=memory read; 7=memory write; 12=memory read multiple; 14=memory read line; 15=memory write and invalidate; any of these commands may be valid to enable the first term of the equation.
`USB_HIT`	PCI address and command targets the IC's USB controller.
`BIOS_ADDR_SPACE:`	BIOS space is defined by C0A43.

4.3 ISA/LPC Bridge And Legacy Logic

4.3.1 ISA Bus

The IC's ISA interface includes a 24-bit address bus and an 8-bit data bus. Only target cycles to the ISA bus are supported; master and DMA cycles are not supported. Memory and IO accesses are supported. Target transactions to the IC may be routed to the ISA bus if ISABIOS specifies that the BIOS address space specified by C0A43 is on the ISA bus or if C0A48[SUB] specifies that the ISA bus is the default path for unclaimed transactions.

Default path memory accesses to greater than the 16-megabyte address space result in ISA bus cycles, but MEMR# and MEMW# pulses are not generated for these cycles. MEMR#/MEMW# pulses are always generated for BIOS-address transactions as specified by C0A43.

The default pulse width for 8-bit IO commands to the ISA bus is 6 BCLKs. The default pulse width for 16-bit IO commands to the ISA bus is 3 BCLKs.

The inactive time between IO commands is specified by C0A40[IORT] to be either 5.5 or 13.5 BCLK cycles. However, if there is a multi-byte PCI cycle that is converted into multiple ISA cycles, then there is only 1.5 BCLK cycles between each of these, regardless as to the state of C0A40[IORT].

4.3.2 LPC Interface

The IC includes a standard LPC controller with two DMA request pins. The LPC bus may be the default path for subtractive cycles based on the state of C0A48[SUB]. The LPC bus may be the path for ROM BIOS transactions based on the state of C0A43 and the ISABIOS pin. Additional LPC address space is specified by C3A[5C:51].

All LPC master and DMA cycles are routed to the PCI interface. LPC does not support peer-to-peer transfers to internal or external LPC devices.

The IC supports LPC DMA cycle sizes of 8- and 16-bits and master cycle sizes of 8-, 16-, and 32- bits. The IC supports LPC DMA cycles with addresses of up to 16MB (24 address bits) and LPC master cycles with addresses of up to 4GB (32 address bits). LPC master cycles must be naturally aligned (i.e., 16-bit master cycles must start at an address where A[0]=0b and 32-bit master cycles must start at an address where A[1:0]=00b).

The inactive time between IO commands is specified by C0A40[IORT] to be either 22 or 54 PCLK cycles. However, if there is a multi-byte cycle that is converted into multiple LC cycles, then there is only 2 PCLK cycles between each of these, regardless as to the state of C0A40[IORT].

Any LPC target cycles in which there is no response on the LPC bus are responded to as follows: writes are dropped (PCI cycle ends normally); reads return all 1's.

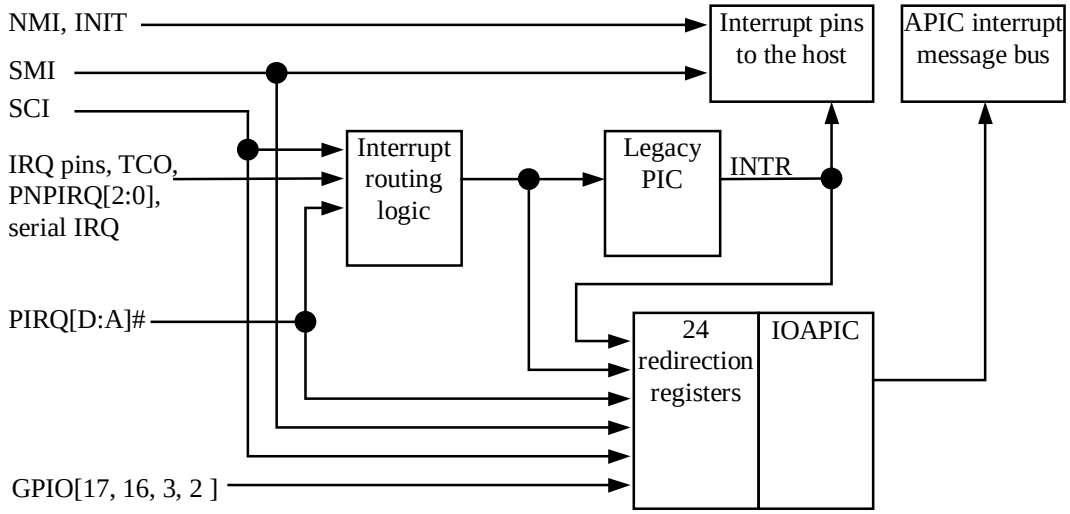
4.3.3 Legacy and Miscellaneous Support Logic

The IC includes the following legacy support logic:

- PORT61 and PORT92 legacy registers.
- FERR# and IGNNE interrupt logic.
- PORT4D0 legacy interrupt edge-level select logic.
- PORTCF9 reset logic.
- Legacy DMA controller.
- Legacy programmable interval timer.

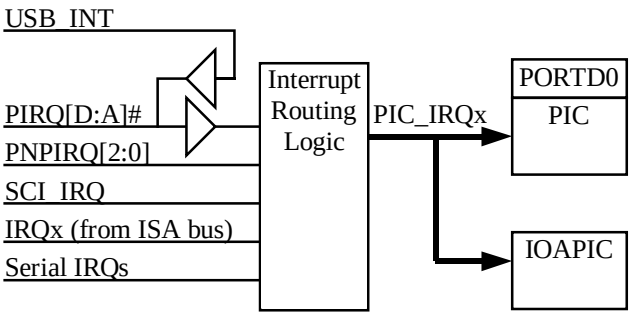
4.3.4 Interrupt Controllers

The IC includes two interrupt controllers: the legacy PIC and an IOAPIC. Interrupt sources are routed to the interrupt controllers as shown in the following diagram.



4.3.4.1 Interrupt Routing Logic

Vectored interrupt requests are routed to the legacy PIC and APIC as shown. The interrupt signals to the PIC may be either rising-edge triggered or active-low level triggered. It is expected that edge-triggered interrupts such as IRQ14 from the IDE controller rise into the PIC to indicate the presence of an interrupt. Conversely, level-sensitive interrupts are low into the PIC to indicate the presence of an interrupt. Edge and level sensitivity for each IRQ are programmed into the PIC through PORT4D0.



The internal USB interrupt signal drives the PIRQD# pin low as an output; when the USB interrupt is deasserted, PIRQD# is left in the high impedance state. So the USB interrupt is wired-ORed into the active state with external interrupts on PIRQD#. The result enters the IC and goes to the interrupt routing logic.

The following are the interrupt routing logic equations:

```
PIRQ_POLA =  C3A54[EDGEPIA] &   PIRQA#
          | ~C3A54[EDGEPIA] & (~PIRQA# | SERINTA | (C1A08[8] & IRQ14) | (C1A08[10] & IRQ15) );
PIRQ_POLB =  C3A54[EDGEPIB] &   PIRQB#
          | ~C3A54[EDGEPIB] & (~PIRQB# | SERINTB);
PIRQ_POLC =  C3A54[EDGEPIC] &   PIRQC#
          | ~C3A54[EDGEPIC] & (~PIRQC# | SERINTC);
PIRQ_POLD =  C3A54[EDGEPID] &   PIRQD#
          | ~C3A54[EDGEPID] & (~PIRQD# | SERINTD);
PCI_IRQx  = PIRQ_POLA & (C3A56[3:0]  == 4'hx) | PIRQ_POLB & (C3A56[7:4]   == 4'hx)
          | PIRQ_POLC & (C3A56[11:8] == 4'hx) | PIRQ_POLD & (C3A56[15:12] == 4'hx);

PNP_IRQx  = PNPIRQ2 & (C3A44[11:8] == 4'hx) | PNPIRQ1 & (C3A44[7:4] == 4'hx)
          | PNPIRQ0 & (C3A44[3:0] == 4'hx);

SCI_IRQx  = SCI_IRQ & (C3A42[3:0] == 4'hx) & ~C0A4B[SCI2IOA];

TCO_IRQx  = TCO_IRQ & (C3A44[2:0] == IRQ[11,10,or 9]) & C3A44[3]; // only applies to IRQs[11:9]

KIRQ1     = EKIRQ1  & SERIRQ1;  // to the USB keyboard emulation logic
KIRQ12    = EKIRQ12 & SERIRQ12; // to the USB keyboard emulation logic

USB_IRQ1  = ~ExternalIRQEn & KIRQ1                 // signal names from USB OHCI spec
          |  EmulationEnable & IRQEn & OutputFull & ~AuxOutputFull;
USB_IRQ12 = ~ExternalIRQEn & KIRQ12                // signal names from USB OHCI spec
          |  EmulationEnable & IRQEn & OutputFull &  AuxOutputFull;

ISA_IRQx  = ~(IRQx  & SERIRQx ) &  // ISA_IRQ[15, 14, 12, 1] not included; these eqns are below
            ~( (C3A56[3:0]   == 4'hx) | (C3A56[7:4]  == 4'hx) | (C3A56[11:8] == 4'hx)
             | (C3A56[15:12] == 4'hx) | (C3A44[11:8] == 4'hx) | (C3A44[7:4]  == 4'hx)
             | (C3A44[3:0]   == 4'hx) | (C3A42[3:0]  == 4'hx);

ISA_IRQ1  = ~(USB_IRQ1) &
            ~( (C3A56[3:0]   == 4'h1) | (C3A56[7:4]  == 4'h1) | (C3A56[11:8] == 4'h1)
             | (C3A56[15:12] == 4'h1) | (C3A44[11:8] == 4'h1) | (C3A44[7:4]  == 4'h1)
             | (C3A44[3:0]   == 4'h1) | (C3A42[3:0]  == 4'h1);

ISA_IRQ12 = ~({C3A46[IRQ12_SEL] == 2'b00) ? IRQ12 : USB_IRQ12) &
            ~( (C3A56[3:0]   == 4'hC) | (C3A56[7:4]  == 4'hC) | (C3A56[11:8] == 4'hC)
             | (C3A56[15:12] == 4'hC) | (C3A44[11:8] == 4'hC) | (C3A44[7:4]  == 4'hC)
             | (C3A44[3:0]   == 4'hC) | (C3A42[3:0]  == 4'hC);

ISA_IRQ14 = ~(IRQ14  & SERIRQ14 ) &
            ~( (C3A56[3:0]   == 4'hE) | (C3A56[7:4]  == 4'hE) | (C3A56[11:8] == 4'hE)
             | (C3A56[15:12] == 4'hE) | (C3A44[11:8] == 4'hE) | (C3A44[7:4]  == 4'hE)
             | (C3A44[3:0]   == 4'hE) | (C3A42[3:0]  == 4'hE) | C1A08[8]);

ISA_IRQ15 = ~(IRQ15  & SERIRQ15 ) &
            ~( (C3A56[3:0]   == 4'hF) | (C3A56[7:4]  == 4'hF) | (C3A56[11:8] == 4'hF)
             | (C3A56[15:12] == 4'hF) | (C3A44[11:8] == 4'hF) | (C3A44[7:4]  == 4'hF)
             | (C3A44[3:0]   == 4'hF) | (C3A42[3:0]  == 4'hF) | C1A08[10]);

PIC_IRQx  = ~(ISA_IRQx | PCI_IRQx  | PNP_IRQx  | SCI_IRQx | TCO_IRQ);
```

Where:

x	The PIC IRQ number, 1, 3 through 7, 9 through 12, 14, and 15.
PIRQ[A,B,C,D]#	The input PCI interrupts (with the polarity of the external signals).
SERINT[y]	The PCI interrupts captured from the SERIRQ pin (with the same polarity as the SERIRQ pin).
SERIRQ[x]	The ISA interrupts captured from the SERIRQ pin (with the same polarity as the SERIRQ pin).
USB_IRQ[12,1]	Outputs of the USB keyboard emulation logic from the USB controller.
PNPIRQ[2:0]	PNP IRQ pins (with the polarity specified by the associated GPIO register).
SCI_IRQ	Active-high SCI interrupt.
TCO_IRQ	TCO interrupt; PM20[TCOSCI_STS].
IRQx	External interrupt pin (with the polarity of external signals).
PIC_IRQx	The interrupt signals that go to the PIC.

From the above equations, a few details can be derived:

- When a PCI, PNP, or SCI interrupt is enabled onto a PIC_IRQ, then the ISA and serial IRQ capability for the IRQ is disabled.
- External IRQs and serial IRQs are designed to be edge triggered.

- PCI and SCI interrupts are designed to be level triggered.
- PNP interrupts may be level or edge triggered. The inverter available in the GPIO register must be employed to preserve the polarity from the external signal to the PIC; if this inverter is not selected, then there is an inversion from the external signal to the PIC.
- IRQ14 and IRQ15 change from external interrupts to native mode interrupts driven by the IDE drives if C1A08[8 and 10] are set respectively. As native mode interrupts, they are still required to be active high (externally); they are combined with PIRQA# logic to become level-triggered, active low signals into the PIC.
- The keyboard and mouse interrupts, EKIRQ1 and EKIRQ12, are ANDed with the serial IRQ versions to go to the USB keyboard emulation logic. The outputs of this logic enter the routing equations.
- In order for the USB keyboard and mouse emulation interrupts to function properly, either EKIRQ1 and EKIRQ12 must be strapped low or the keyboard controller must keep the serial IRQ slots for IRQ1 and IRQ12 low.

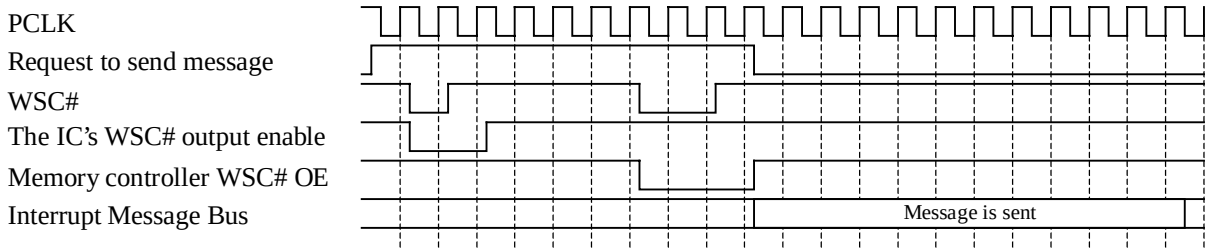
4.3.4.2 IOAPIC

The IOAPIC supports 24 interrupt signals which come from the interrupt routing logic, the PCI interrupts, GPIOs, the SCI interrupt, the SMI interrupt, and internal signals. Each interrupt corresponds with a redirection register that specifies the IOAPIC behavior for the interrupt. When the IOAPIC is enabled, it transmits interrupt messages to the processor through the 3-signal interrupt message bus (IMB), PICCLK and PICD[1:0]#.

4.3.4.2.1 WSC#

The WSC# signal is used to allow upstream posted writes to be visible to the host prior to interrupt message transmission over the IMB. It connects between the IC and the system memory controller. It is enabled when the IOAPIC is enabled (C0A4B[APICEN]).

The IC requests that the memory controller guarantee that the upstream posted write transactions in its data buffers are visible to the host by placing a single-PCLK pulse on WSC#. When all the posted writes that were in the memory controller when the first pulse was detected are visible to the host, then the memory controller responds with a two-PCLK pulse back to the IC. After this is received, the IC transmits the interrupt message over the IMB.



The IC enables WSC# during the PCLK cycle in which it drives WSC# low and the following cycle in which WSC# is driven high. It is expected that the memory controller enables the line for three PCLK cycles. WSC# is required to be driven high for at least one clock before it is allowed to be driven low again.

4.3.4.2.2 The IRQ lines

The IOAPIC supports 24 interrupt request signals. Each interrupt request input is combined with its corresponding redirection register to specify the behavior of the interrupt. These interrupt request signals are connected to redirection registers (APIC IRQs) as shown in the following table.

APIC IRQ	Connection	APIC IRQ	Connection
0	PIC INTR output	12	PIC_IRQ12
1	PIC_IRQ1	13	PIC_IRQ13 (floating point error)
2	PIC_IRQ0 (PIT)	14	PIC_IRQ14
3	PIC_IRQ3	15	PIC_IRQ15
4	PIC_IRQ4	16	PIRQA#
5	PIC_IRQ5	17	PIRQB#
6	PIC_IRQ6	18	PIRQC#
7	PIC_IRQ7	19	PIRQD#
8	PIC_INT8 (RTC)	20	GPIO2 (see PMC2)
9	PIC_IRQ9	21	GPIO3 (see PMC3)
10	PIC_IRQ10	22	SCI or GPIO16 (see C0A4B and PMD0)
11	PIC_IRQ11	23	SMI or GPIO17 (see C0A4B and PMD1)

Note: APIC IRQs [23:20] may also be ORed with the TCO IRQ as specified by C3A44[TCO_INT_SEL]. Note: PIC_IRQx is specified in section 4.3.4.1.

4.3.5 Real-Time Clock (Logic Powered by VDD_AL)

The real-time clock logic requires an external 32 kHz oscillator connected to RTCX_IN and RTCX_OUT. It includes a clock and calendar timer, an alarm (which generates an interrupt), and 256 bytes of non-volatile RAM. It is register compatible with the legacy PC real-time clocks. It meets ACPI real-time clock requirements. The real-time clock resides on the VDD_AL power plane.

4.4 Enhanced IDE Controller

The enhanced IDE controller support independent primary and secondary ports. Each port supports two drives. Supported protocols include PIO modes 0-4, multi-word DMA, and ultra DMA modes through to ATA-100. Each of the four possible drives may be programmed to operate in any mode independent of the other drives.

The enhanced IDE controller is accessed through function 1 PCI configuration registers (C1Axx).

4.5 USB Controller

The USB Controller is an implementation of the Open Host Controller Interface 1.0a specification containing a host controller core, a 4-port root hub, and hardware traps for legacy keyboard and mouse emulation.

4.5.1 USB Interrupts

The USB interrupt signal is drive low the PCI interrupt, PIRQD#. However, it may be diverted to SMIs by the OHCI-defined register HcControl_InterruptRouting. See section 4.3.4.1 for data on routing keyboard and mouse emulation interrupts. SMI interrupts are also generated in response to accesses to IO ports 60h and 64h and to IRQ1 and IRQ12 in support of the emulation logic.

4.6 System Management Logic

System management includes logic for most of the multiplexed-function pins—such as general-purpose IO (GPIO) pins, the power management (PM) pins, system management bus (SMBus) pins, the processor interface pins, and the plug and play (PNP) interrupt pins—as well as the logic required for ACPI-compliant power management for desktop and mobile systems. Programmable register access to most of this logic is contained in the C3Axx configuration space and the PMxx IO space. Here are the major functions:

- ACPI interrupt (SCI or SMI based on the state of PM04[SCI_EN] status bits and enables.
- SMI status bits and enables.
- System power state machine (SPSM).
- Resume event logic (to place the SPSM into the full-on state).
- SMBus.
- System power state control pins and general purpose pins.
- Hardware traps.
- System inactivity timer.
- Serial IRQ logic.

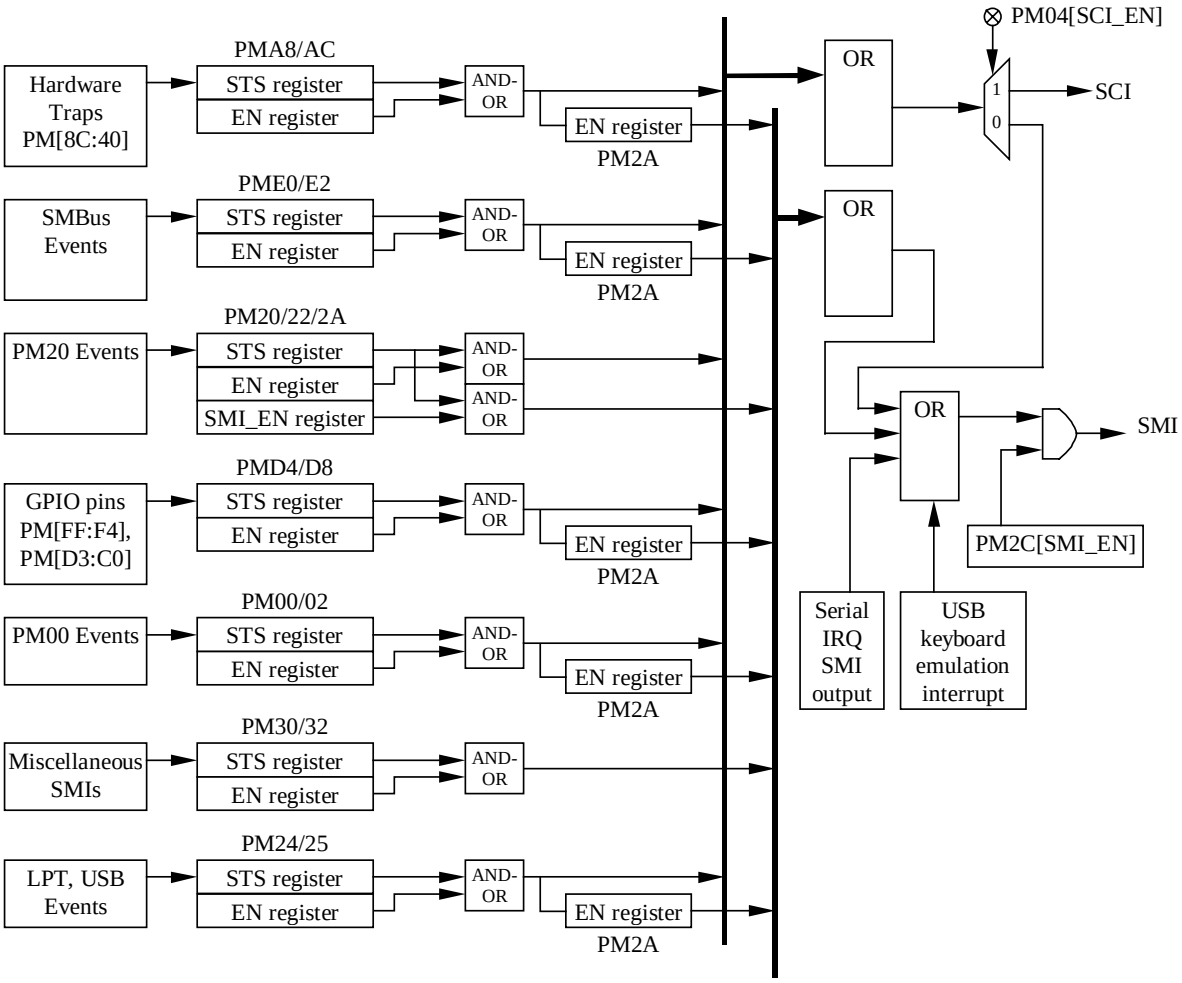
4.6.1 Power Management

The following table summarizes all the system management events that are detected by the system management logic and the hardware response enable registers. The columns are STS, where the status bits are accessible, EVT, where the grouped status bits may be read, SCI/SMI EN, where ACPI interrupts may be enabled, SMI_EN, where the SMI interrupts may be enabled, SIT_EN, where the events may be enabled to reload the system inactivity timer, and the resume columns which show where the registers to enable the resume events from C2, C3, POS, STD, STR, and SOFF to FON.

Events	STS	Event EVT in PM28	SCI/SMI EN	SMI only SMI_EN in PM2A	Reload SIT_EN	Resume POS EN	Resume C2-C3 EN	Resume STD, STR, SOFF EN
SMBus host complete/error	PME0	SMB_EVT	PME2	SMBUS_EN				
SMBus host as slave transfer	PME0		PME2				PM16	PM26
SMBus snoop match	PME0		PME2				PM16	PM26
SMBALERT# pin	PME0		PME2				PM16	
IRQ[15:0]					PMB4			
INTR (unmasked IRQs)					PMB4[2]		PM16	
PCI bus masters	PM00				PMB4		PM04[1] (C3)	
20 Hardware traps	PMA8	TRP_EVT	PMAC	TRPSMI_EN	PMB0			
Parallel port hardware traps	PM24		PM25		PMB0			
System inactivity timer time out	PM20		PM22	SITSMI_EN			PM16	
TCO IRQ interrupts	PM20		PM22					
TCO SMI interrupt	PM44	TCO_EVT		TCO_EN				
Sleep command	PM30	MISC_EVT		PM32				
BIOS write enable 0-to-1	PM30			PM32				
Serial IRQ SMI	PM30			PM32				
1 minute timer	PM30			PM32				
64 millisecond timer	PM30			PM32				
USB bus resume event	PM20	LPTUSB_EVT	PM22	USBSMI_EN			PM16	PM26
4 USB transaction types	PM24		PM25					
ACPI timer overflow	PM00	PM1_EVT	PM02 (SCI only)	PM1SMI_EN				
Power button override	PM00							PM26 (off)
OS release (GBL_RLS)	PM04, 28			BIOSSMI_EN				
BIOS release (BIOS_RLS)	PM00, 2C	PM1_EVT	PM02 (SCI only)	PM1SMI_EN				
Software SMI (PM1E/2F)	PM28			SWISMI_EN				
GPIO inputs	PMD4	GPIO_EVT	PMD8	GPIOSMI_EN				
Real time clock IRQ	PM00	PM1_EVT	PM02	PM1SMI_EN			PM16	PM26
PWRBTN# pin	PM00		PM02	PM1SMI_EN, PWRBTN_EN			PM16	PM26
EXTSMI# pin	PM20		PM22	EXTSMI_EN			PM16	PM26
PME# pin	PM20		PM22	PMESMI_EN			PM16	PM26
RI# pin	PM20		PM22	RI_SMI_EN			PM16	PM26
SLPBTN# pin	PM00	PM1_EVT	PM02	PM1SMI_EN, SLPBTN_EN			PM16	PM26
THERM# pin	PM20		PM22	THMSMI_EN				

4.6.1.1 SCI And SMI Control

System management events cause corresponding STS registers to be set. STS registers may be enabled to generate SCI and SMI interrupts. The following diagram shows how the STS registers are routed to the interrupts.



The "AND-OR" boxes in the middle of the diagram specify the logical AND of the STS and EN registers (or STS and SMI_EN registers, as the case may be) the results of which are logically ORed together; for example: (STS1 & EN1) | (STS2 & EN2)... All enabled ACPI interrupts may be routed to either SCI or SMI interrupts by PM04[SCI_EN]. Or these STS registers may be routed directly to SMI through the SMI_EN registers, regardless of the state of PM04[SCI_EN]. The USB controller and serial IRQ logic also provide sources of SMI that is ORed into the logic. SMI and SCI are inputs to the interrupt logic; see section 4.3.4.

4.6.1.2 Traps

Configuration registers C3A[D8:A0] specify several traps for programmable memory and IO space address ranges. PMA8 provides the status registers for these and several fixed-address traps. These traps are generated for the specified transactions that are presented to the host PCI bus. They may be enabled to generate ACPI interrupts through PMAC or SMI interrupts through PM2A.

4.6.1.3 System Inactivity Timer

The system inactivity timer is an 8-bit down counter that is controlled through PM98. Any of the hardware traps, IRQ lines, or PCI bus master activity may be enabled to reload the system inactivity timer through PMB0 and PMB4. If the timer decrements to zero, then, if enabled by PM22 or PM2A, an interrupt is generated.

4.6.1.4 Throttling logic

When throttling, the IC repetitively places the processor into the stop-grant state for a specified percentage of time in order to reduce the power being consumed by the processor. STPCLK# is used to control the processor stop-grant state with a period of 244 microseconds (based on 8 cycles of the 32.768 kHz clock) and a duty cycle as specified by control registers C3A50 and PM10.

Two types of throttling are possible: normal and thermal. Normal throttling is controlled by software. Thermal throttling is controlled by the THERM# pin (see also C3A40[TH2SD]). If both are enabled simultaneously, then the duty cycle specified for thermal throttling is employed. Throttling is only possible when in the FON state. If throttling is enabled when entering other states, then it stops; after exiting the state, throttling resumes.

4.6.1.5 System Power State Controller (SPSC)

The system power state controller (SPSC) supports the following system power states:

State	VDD3	VDD_AUX	VDD_RTC, VDD_AL
Full on (FON)	On	On	On
C2; C3	On	On	On
Power on suspend (POS; S1)	On	On	On
Suspend to RAM (STR; S3)	Off	On	On
Soft off (SOFF; S5); suspend to disk (STD; S4)	Off	On	On
Mechanical off (MOFF; G3)	Off	Off	On

Mechanical off (MOFF or ACPI G3 state). MOFF is the state when only VDD_AL is powered. This may happen at any time, from any state, due to the loss of power to the VDD_AUX plane (e.g., a power outage, the power supply is unplugged, or the power supply's mechanical switch). When power is applied to VDD_AUX, then the system transitions to either FON or SOFF.

Soft off (SOFF or ACPI G2/S5 states). In the SOFF state, the system appears to the user to be off. The IC's VDD_AUX plane is powered, but the main supplies are not; RPWRON is low to disable power system DRAM. The system normally uses PWRBTN# to transition from SOFF to FON. The IC also allows SMBus activity, USB resume events, the real-time clock alarm, the EXTSMI# pin, the SLPBTN# pin, the RI# pin and the PME# pin to be enabled to cause this transition.

Suspend to disk (STD or ACPI S4 state). The IC's behavior in this state is equivalent to SOFF.

Suspend to RAM (STR or ACPI S3 state). In the STR state, the system's context is stored in system memory (which remains powered; RPWRON is high) and the main power supplies are shut off (PWRON# high). The IC's behavior in the STR state is similar to SOFF; the main difference is that RPWRON is asserted in STR.

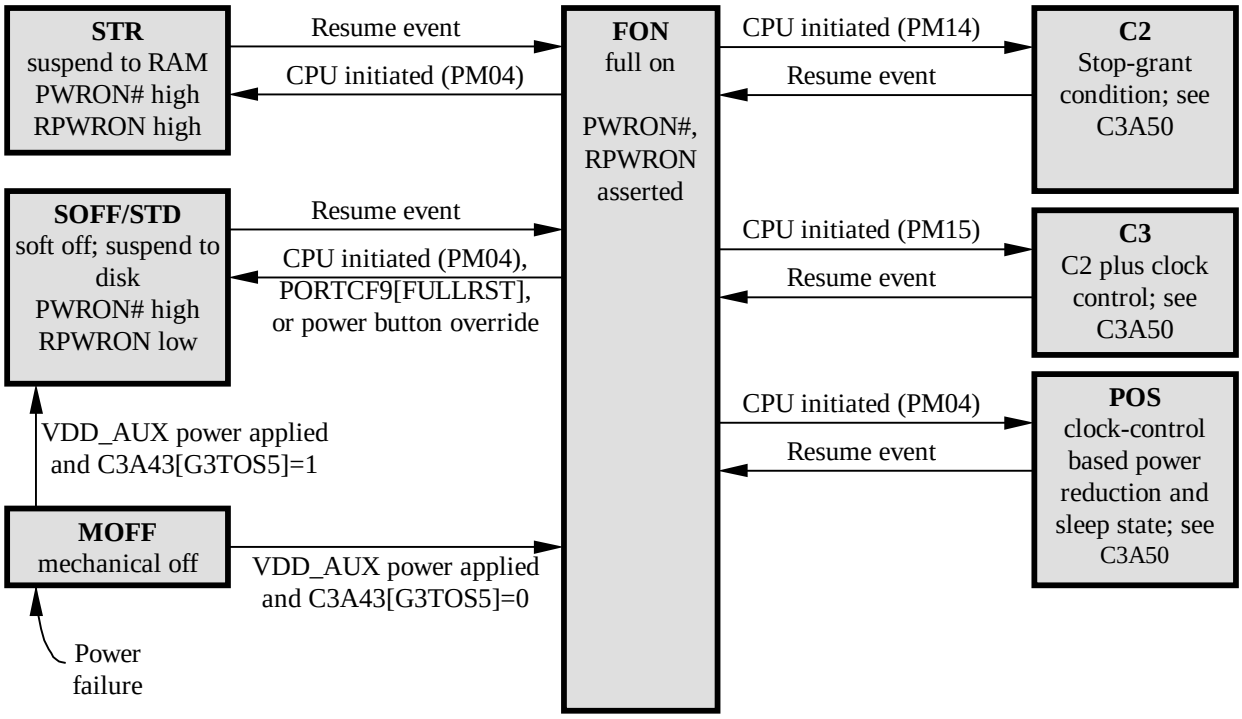
Power on suspend (POS or ACPI S1 state). All power planes to the IC are valid in POS. Signal control during POS is specified by C3A50.

Snoop-capable clock control (C2). In C2, the processor is placed into the stop-grant state. Signal control during C2 is specified by C3A50. It is expected that the processor's cache may be snooped while in this state.

Snoop-disabled clock control (C3). In C3, the processor is placed into the stop-grant state such that the processor's cache cannot be snooped; PCI master requests result in resume events (see PM04[BM_RLD]). Signal control during C3 is specified by C3A50.

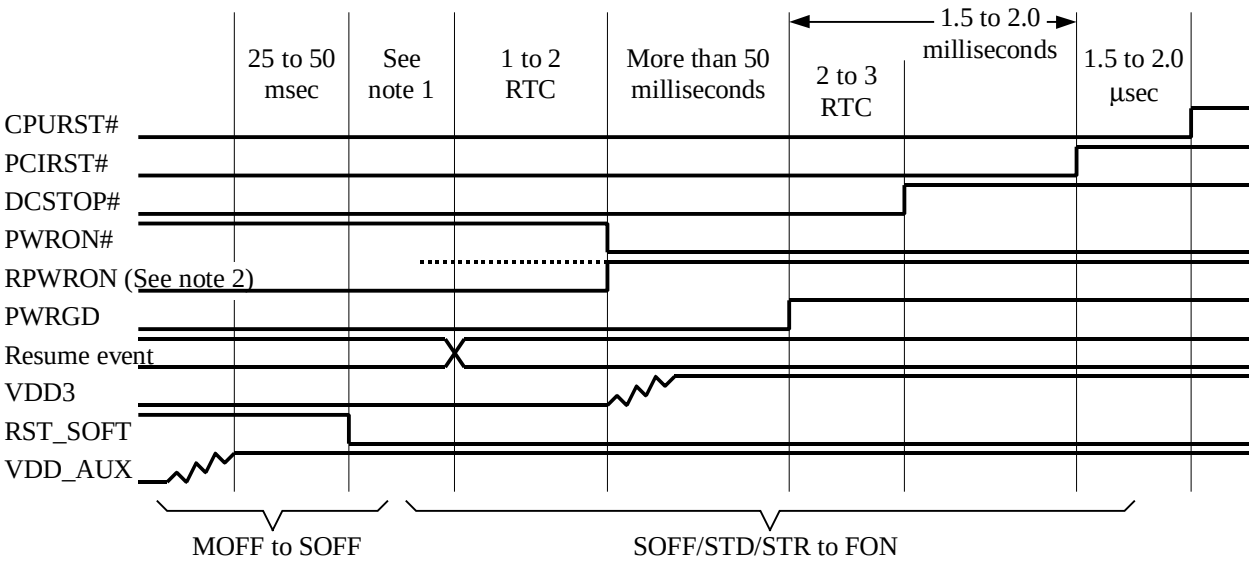
Full on (FON). In FON, all the power planes are powered and the processor is not in the stop-grant state.

The following figure shows the system power state transitions.



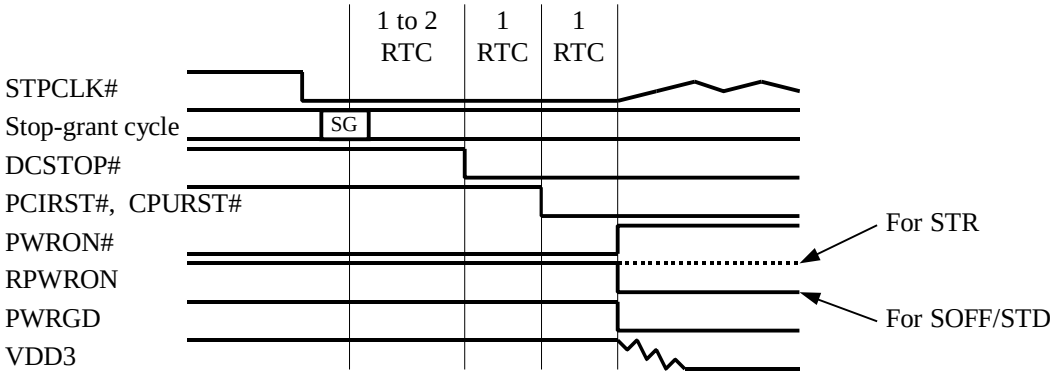
4.6.1.5.1 Transitions Between MOFF/SOFF/STD/STR and FON

In the timing diagrams, RTC refers to 32 kHz clocks cycles.



MOFF to SOFF/STD/STR to FON

Note 1: If C3A43[G3TOS5] = 0, then the time from the end of RST_SOFT to PWRON# assertion is 1 to 2 RTC clocks. If C3A43[G3TOS5] = 1, then the resume event must occur before PWRON# is asserted.
Note 2: RPWRON# is high during STR and low during STD and SOFF.



FON to SOFF/STD/STR

For transitions to SOFF that are initiated by a power/sleep button override event or by PORTCF9[FULLRST], the STPCLK# assertion and stop-grant cycles are skipped; the sequence starts with the assertion of DCSTOP#.

4.6.1.5.2 Transitions From FON To C2, C3 And POS

C3A50 specifies the definition of these transitions as enables for the following signals: CPURST#, SUSPEND#, CPUSLEEP#, PCISTOP#, CPUSTOP#, DCSTOP#, CACHE_ZZ. Any of these signals may be enabled for the transition to any of C2, C3 or POS. The transition to C2, C3, or POS occurs as follows, for each of the enabled pin controls:

- Processor initiation. The transition to C2 is initiated by reading PM14; the transition to C3 is initiated by reading PM15; the transition to POS is initiated by writing the appropriate value to PM04[SLP_EN, SLP_TYP].
- Stop-grant. The IC asserts STPCLK# and waits for the stop-grant cycle from the host (a PCI special cycle as specified by C3A41[STPGNT]) to complete.
- PICCLK. If going into POS and C3A50[APIC_POSEN] is low, then PICCLK held low after stop-grant.
- CACHE_ZZ. At least four PCLK cycles after stop-grant, CACHE_ZZ is asserted.
- DCSTOP#. At least eight PCLK cycles after stop-grant, DCSTOP# is asserted.
- CPUSLEEP#. At least 64 PCLK cycles after stop-grant, CPUSLEEP# is asserted.
- CPUSTOP# and PCISTOP#. At least 68 PCLK cycles after stop-grant, CPUSTOP# and PCISTOP# are asserted.
- SUSPEND#. At least 80 PCLK cycles after stop-grant, SUSPEND# is asserted.

4.6.1.5.3 Transitions From C2, C3 And POS To FON

The following is the resume sequence from C2, C3, and POS, once an enabled resume event occurs. These resume events are enabled by PM16 and, in the case of C3, PM04[1]. Here is the resume sequence, once an enabled resume event occurs, if the SUSPEND# pin is enabled in C3A50:

- SUSPEND#. Immediately after the resume event, SUSPEND#, CPUSLEEP# and STPCLK# are deasserted within 100 nanoseconds of each other. If CPURST# is enabled to be asserted by C3A50, it is asserted as well. If resuming from POS and C3A50[APIC_POSEN] is low, then PICCLK becomes active at this time.
- CPUSTOP# and PCISTOP#. 17 to 18 milliseconds after SUSPEND#, CPUSTOP# and PCISTOP# are deasserted.
- DCSTOP#. 700 to 800 microseconds after CPUSTOP# and PCISTOP#, DCSTOP# is deasserted.
- CACHE_ZZ. 240 to 250 microseconds after DCSTOP#, CACHE_ZZ is deasserted.
- CPURST#. 4 to6 PCLK cycles after CACHE_ZZ, CPURST# is deasserted (if it was asserted).

The following is the resume sequence, once an enabled resume event occurs, if the SUSPEND# pin is not enabled, but any of DCSTOP#, PCISTOP#, CPUSLEEP, and CPUSTOP# are enabled in C3A50:

- CPUSTOP# and PCISTOP#. CPUSTOP# and PCISTOP# are deasserted immediately after the resume event. If resuming from POS and C3A50[APIC_POSEN] is low, then PICCLK becomes active at this time.
- DCSTOP#. 700 to 800 microseconds after the resume event, DCSTOP# and CPUSLEEP# are deasserted.
- CACHE_ZZ. 240 to 250 microseconds after DCSTOP#, CACHE_ZZ is deasserted.
- STPCLK#. 4 to 6 PCLK cycles after CACHE_ZZ, STPCLK# is deasserted.

The following is the resume sequence, once an enabled resume event occurs, if the SUSPEND#, PCISTOP#, CPUSTOP#, CPUSLEEP, and DCSTOP# pins is not enabled in C3A50:

- CACHE_ZZ. At least 4 PCLK cycles after the resume event, CACHE_ZZ is deasserted. If resuming from POS and C3A50[APIC_POSEN] is low, then PICCLK becomes active at this time.
- STPCLK#. 4 to 6 PCLK cycles after CACHE_ZZ, STPCLK# is deasserted.

4.6.2 Serial IRQ Protocol

The IC supports the serial IRQ protocol. This logic controls the SERIRQ pin and outputs IRQs to the legacy PIC and IOAPIC blocks. This logic is synchronous with PCLK. It is specified by C3A4A. The IC does not provide support for generating IRQ0, IRQ2, IRQ8, or IRQ13 via SERIRQ. In order to use a serial IRQ interrupt, the corresponding external IRQ pin, EKIRQ[1, 12], IRQ[15, 14, 11:9,7:3], must be pulled high. See section 4.3.4.1 for more details.

4.6.3 SMBus Controller

The IC includes a system management bus, SMBus, controller. SMBus is a two-wire serial interface typically used to communicate with system devices such as temperature sensors, clock chips, and batteries. The control registers for this bus are PME0 through PMEF.

The SMBus controller includes a host controller and a host-as-slave controller.

Host controller. The host controller is used to generate cycles over the SMBus as a master. Software accomplishes this by setting up PME2[CYCTYPE] to specify the type of SMBus cycle desired and then (or concurrently) writing a 1 to PME2[HOSTST]. This triggers an SMBus cycle with the address, command, and data fields as specified by the registers called out in PME2[CYCTYPE].

Writes to the host controller registers PME2[3:0], PME4, PME8, and PME9 are illegal while the host is busy with a cycle. If a write occurs to PME2 while PME0[HST_BSY] is active, then the four LSBs be ignored. Writes to PME4, PME8, and PME9 while PME0[HST_BSY] is active are ignored (the transaction is completed, but no data is transferred to the SMBus controller).

If an SMBus-defined time out occurs while the host is master of the SMBus, then the IC attempts to generate a SMBus stop event to clear the cycle and PME0[TO_STS] is set.

The host controller is only available in the FON state.

Host-as-slave controller. The host-as-slave controller responds to word-write accesses to either the host address specified by PMEE or the snoop address specified by PMEF. In either case, if the address matches, then the subsequent data is placed in PMEC and PMEA. In the case of snoop accesses, the command information is stored in PMEC[7:0] and the data is stored in PMEA[15:0]. In the case of addresses that match the PMEE host-as-slave address register, then the address is stored in PMEC[7:1]—if the transaction includes a 7-bit address—or PMEC[15:1]—if the transaction includes a 10-bit address. After the address match is detected, the IC waits for the subsequent stop command before setting the appropriate status bits in PME0[HSLV_STS, SNP_STS]; however, if a time out occurs during the cycle, after the address match is detected, then the appropriate bit in PME0[HSLV_STS, SNP_STS] are set.

If one of the slave status bits, PME0[HSLV_STS, SNP_STS], is set and another access to the host slave controller is initiated, then it is not acknowledged via the first SMBus acknowledge cycle until the status bit is cleared.

The host-as-slave controller operates in all system power states except MOFF. It may be used to generate interrupts and resume events.

SMBALERT. The host controller includes support for the SMBALERT# signal. If this signal is asserted, then it is expected that software determines the source by generating a host read cycle to the alert response address, 0001100b. If the SMBus host controller detects this address for a read cycle with PME2[CYCTYPE] set to receive byte (001b), then it stores the address returned by the SMBALERT# slave in PME6[7:0]. If bits[7:1] of this address are 1111_0xxb, indicating a 10-bit address, then it stores the next byte from the slave in PME6[15:8].

4.6.4 Plug And Play

The IC supports three PNP IRQs and two PNP chip selects. The registers that specify these are C3A44 and C3A46. The PNP pins are multiplexed with other functions. The control registers that specify the functions (the GPIO control registers PM[D3:C0], PM[FF:F4]) must be set up appropriately for the PNP functions to operate.

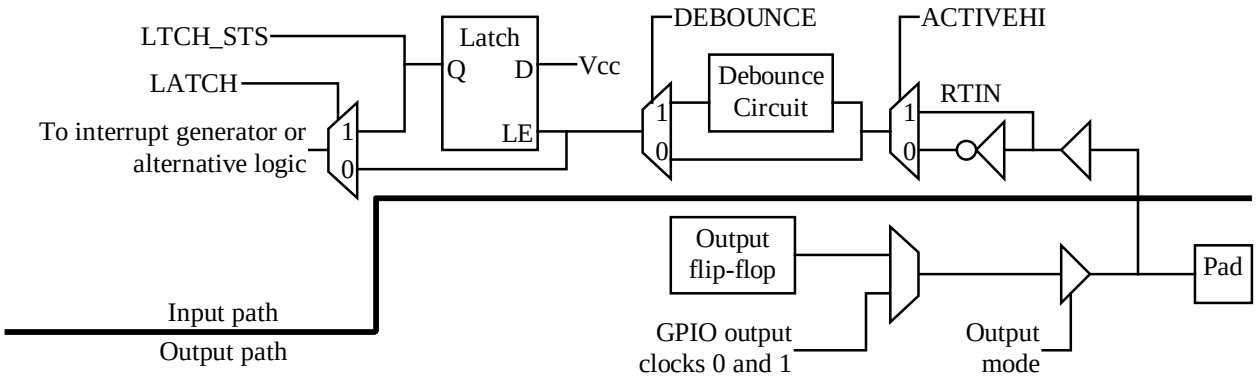
4.6.5 General Purpose IO

The general-purpose IO pins, GPIO[31:0], may be assigned to be inputs, outputs, interrupt generators, or bus controls. These pins may be programmed to be general-purpose IO or to serve alternate functions; see the PM[FF:F4, D3:C0] register definitions. Many of these pins are named after their alternate functions. There is one control register for each pin, PM[FF:F4, D3:C0]. IRQ status and enables are available for each pin in registers PMD4 and PMD8.

General-purpose IO functions. When programmed as a GPIO pin, the following functions are available:

- Outputs.
  - May be set high or low.
  - May be controlled by GPIO output clocks 0 or 1 (see PMDC).
- Inputs.
  - Active high or active low programmable.
  - SCI or SMI IRQ capable.
  - May be latched or not latched.
  - Inputs may be debounce protected.

The following diagram shows the format for all GPIO pins. The input path is not disabled when the output path is enabled or when the pin is used for an alternate function. In order for the latch to be set, the LE input must go high.



Debounce. The input signal must be active and stable for 12 to 16 milliseconds before the output signal is asserted.

GPIO output clocks. There are two GPIO output clocks (numbered 0 and 1). They are specified by PMDC. Each output clock includes a 7-bit programmable high time, a 7-bit programmable low time, and the counter may be clocked by one of four frequencies. Here are the options:

PMDC[CLK[1,0]BASE]	Base clock period	Output high time range	Output low time range
00b	250 microseconds	250 µs to 32 ms	250 us to 32 ms
01b	2 milliseconds	2 ms to 256 ms	2 ms to 256 ms
10b	16 milliseconds	16 ms to 2 seconds	16 ms to 2 seconds
11b	128 milliseconds	128 ms to 16.4 seconds	128 ms to 16.4 seconds

The output of the two GPIO output clocks may be selected to drive the output of any of the GPIO pins. They may be used to blink LEDs or for other functions.

5 Registers

5.1 Register Overview

The IC includes several sets of registers accessed through a variety of address spaces. IO address space refers to register addresses that are accessed via x86 IO instructions such as IN and OUT. PCI configuration space is typically accessed via PCI-defined IO cycles to CF8h and CFCh in the host. There is also memory space and indexed address space in the IC.

5.1.1 Configuration Space

The address space for PCI configuration registers is broken up into busses, devices, functions, and, offsets, as defined by the PCI specification. Configuration registers within the IC are accessed by type 0 configuration cycles. The IDSEL pin specifies the IC as the targeted device. The function number is mapped into bits[10:8] of the configuration address. The offset is mapped to bits[7:2] of the configuration address.

5.1.2 Register Naming And Description Conventions

Each register location has an assigned mnemonic that specifies the address space and offset. These mnemonics start with two to four characters that identify the space followed by characters that identify the offset within the space. Register fields within register locations are also identified with a name or bit group in brackets following the register location mnemonic. For example, the ACPI sleep type register field, which is located at offset 04h of PMxx space, bits10, 11, and 12, is referenced as PM04[SLP_TYP] or PM04[12:10].

PCI configuration spaces are referenced with mnemonics that takes the form of C[4:0]A[FF:0], where the first bracket contains function number and the last bracket contains the offset.

PCI configuration spaces.

Function	Mnemonic	Function
0	C0Axx	PCI-ISA/LPC bridge
1	C1Axx	IDE controller
2	C2Axx	Not used
3	C3Axx	System management registers
4	C4Axx	USB controller

Fixed address spaces.

Port(s)	Mnemonic	Type	Function
00-0F	PORTxx	IO mapped	Slave DMA controller
20-21	PORTxx	IO mapped	Master interrupt controller
40-43	PORTxx	IO mapped	Programmable interval timer
60, 64	PORTxx	IO mapped	USB keyboard emulation address
61	PORT61	IO mapped	AT Compatibility Register
70-73	RTCxx	IO mapped	Real-time clock and CMOS RAM
80-8F	PORTxx	IO mapped	DMA page registers
92	PORT92	IO mapped	System control register
A0-A1	PORTxx	IO mapped	Slave interrupt controller
C0-DF	PORTxx	IO mapped	Master DMA controller
F0-F1	PORTxx	IO mapped	Floating point error control
170-177, 376	PORTxxx	IO mapped	Secondary IDE drives (not used when in native mode)
1F0-1F7, 376	PORTxxx	IO mapped	Primary IDE drives (not used when in native mode)
4D0-4D1	PORT4D0	IO mapped	EISA-defined level-triggered interrupt control registers
CF9	PORTCF9	IO mapped	System reset register
FEC0_0000 to FEC0_001F	IOAxx	Memory mapped	IOAPIC register set

Relocatable address spaces.

Base address register	Mnemonic	Type	Size (bytes)	Function
C1A10	None	IO mapped	8	Pointer to primary port IDE command space
C1A14	None	IO mapped	4	Pointer to primary port IDE control space
C1A18	None	IO mapped	8	Pointer to secondary port IDE command space
C1A1C	None	IO mapped	4	Pointer to secondary port IDE control space
C1A20	IBMx	IO mapped	16	IDE controller bus master control registers
C3A58	PMxx	IO mapped	256	System management IO register space
C4A10	USBxxx	Memory mapped	4K	USB IO register space

Note: C1A10, C1A14, C1A18, and C1A20 are only used when the IDE controller is in native mode as specified by C1A08.

The following are register behaviors found in the register descriptions.

Type	Description
Read or read only	Capable of being read by software. Read only implies that the register cannot be written to by software.
Write	Capable of being written by software.
Set by hardware	Register bit is set high hardware.
Write 1 to clear	Software must write a 1 to the bit in order to clear it. Writing a 0 to these bits has no effect.
Write 1 only	Software may set the bit high by writing a 1 to it. However subsequent writes of 0 have no effect. RESET# must be asserted in order to clear the bit.
Write once	After RESET#, these registers may be written to once. After they are written, they become read only until the next RESET# assertion.

5.2 PCI-ISA Bridge Configuration Registers (C0Axx)

These registers are in PCI configuration space, function 0. See section 5.1.2 for a description of the register naming convention.

C0A00: PCI-ISA Bridge Vendor And Device ID
Configuration space; function 0; offset: 03-00h. Default: 7410 1022h. Read only.

31:16	15:0
DID	VID

VID. Vendor ID.
DID. PCI-ISA/LPC bridge device ID.

C0A04: PCI-ISA Bridge Status And Command Register
Configuration space; function 0; offset: 07-04h. Default: 0200 000Fh.

31:16	15:0
STATUS[15:0]	COMMAND[15:0]

COMMAND[2:0] IO, memory and master enable. Read only. Hardwired in the enabled state.
COMMAND[3] Special Cycle Enable, SPCYCEN. Read-write. 1=The IC responds to PCI shutdown special cycles by generating a pulse over either CPURST# or INIT# (based on the state of C0A47[CPURS]). 0=The IC ignores PCI shutdown special cycles.
COMMAND[15:4]. Read only. These bits are fixed at their default values.
STATUS[11:0]. Read only. These bits are fixed at their default values.
STATUS[12] Received Target Abort, RTGTABT. Read; set by hardware; write 1 to clear. 1=The PCI-ISA bridge received a target abort while master of the PCI bus.
STATUS[13] Received Master Abort, RMASABT. Read; set by hardware; write 1 to clear. 1=The PCI-ISA bridge received a master abort while master of the PCI bus.
STATUS[15:14]. Read only. These bits are fixed at their default values.

C0A08: PCI-ISA Bridge Revision And Class Code Register
Configuration space; function 0; offset: 0B-08h. Default: 0601 0001h. Read only.

31:8	7:0
CLASSCODE	REVISION

REVISION. PCI-ISA bridge silicon revision.
CLASSCODE. Provides the bridge class code as defined in the PCI specification.

C0A0C: PCI-ISA Bridge BIST-Header-Latency-Cache Register
Configuration space; function 0; offset: 0F-0Ch. Default: 0080 0000h. Read only.

31:24	23:16	15:8	7:0
BIST	HEADER	LATENCY	CACHE

CACHE, LATENCY, HEADER, BIST. These bits are fixed at their default values.

C0A2C: PCI-ISA Bridge Subsystem ID and Subsystem Vendor ID Register
Configuration space; function 0; offset: 2F-2Ch. Default: 0000_0000h. Read only.

31:16	15:0
SSID	SSVENDORID

SSVENDORID and SSID. Subsystem vendor ID and subsystem ID registers. This register is write accessible through C0A70.

C0A40: ISA Bus Control 1 Register

Configuration space; function 0; offset: 40h Default: 00h Read-write.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LPC_IOR	IORT	BLE	RWS	RWR

RWR. ROM write enable. 1=Write accesses to BIOS space specified by C0A43 are enabled. 0=BIOS write accesses are disabled. This bit functions whether ROM space is located on the ISA bus or LPC bus. Note: Writing this bit from 0 to 1 sets PM30[RWR_STS].

RWS. ROM wait states. 0=The ISA memory command signal (either MEMR# or MEMW#) is asserted for two BCLK cycles when accessing BIOS on the ISA bus. 1=The ISA memory command signal is asserted for one BCLK cycle when accessing BIOS on the ISA bus. If C3A48[ISABIOS]=0, then this bit has no affect.

BLE. BIOS lock enable. Read; write 1 only. 1=Setting C0A40[RWR] from 0 to 1 sets PM44[IBIOS_STS] and generate an SMI. 0=Setting C0A40[RWR] from 0 to 1 does not set PM44[IBIOS_STS] and does not generate an SMI. Once this BLE is set, it can only be cleared by PCIRST#.

IORT. IO recovery time. 0=There are a minimum of 5.5 BCLK cycles between the trailing edge of an ISA IO command signal (IOR# or IOW#) and the leading edge of the ISA IO command signal for the subsequent ISA bus IO cycle and there are at least 22 PCLKs between LPC IO cycles. 1=There are a minimum of 13.5 BCLK cycles between adjacent ISA bus IO cycles and there are at least 54 PCLKs between LPC IO cycles. This bit does not affect memory cycles.

LPC_IOR. LPC IO recovery. 1= IO recovery delay (specified by IORT) enforced for both LPC and legacy IO cycles. 0=IO recovery delay only enforced for legacy IO cycles (cycles to the DMA controller, legacy PIC, programmable interval timer, and real-time clock).

C0A41: ISA Bus Control 2 Register

Configuration space; function 0; offset: 41h Default: 02h

7	6	5	4	3	2	1	0
MBL	Reserved	P92FR	Reserved	Reserved	Reserved	NMIDIS	SHEN

SHEN. Shadow register access enable. Read-write. 1=Shadowed IO access to legacy write-only registers is enabled. 0=Normal access of legacy registers. The following table specifies all registers affected by this bit:

IO port	R/W	Normal mode	Shadow mode
DMA: 00h, 02h, 04h, 06h,	W	Base address for DMA channel	Current address for DMA channel
C0h, C4h, C8h, CCh	R	Current address for DMA channel	Base address for DMA channel
DMA: 01h, 03h, 05h, 07h,	W	Base byte count for DMA channel	Current byte count for DMA channel
C2h, C6h, CAh, CEh	R	Current byte count for DMA channel	Base byte count for DMA channel
DMA: 08h/D0h	W	Command Register DMA CH[3:0]/[7:4]	Status Register DMA CH[3:0]/[7:4]
	R	Status Register DMA CH[3:0]/[7:4]	1st read: Command reg DMA CH[3:0]/[7:4] 2nd read: Request reg DMA CH[3:0]/[7:4] 3rd read: Mode register DMA CH0/4 4th read: Mode register DMA CH1/5 5th read: Mode register DMA CH2/6 6th read: Mode register DMA CH3/7
DMA: 09h/D2h, 0Ah/D4h, 0Bh/D6h	W	See DMA controller	Reserved
DMA: 0Ch/D8h, 0Dh/DAh, 0Eh/DCh	W	See DMA controller	Same as normal mode
DMA: 0Fh/Deh	W	Write all masks [3:0]/[7:4]	Write all masks [3:0]/[7:4]
	R	Reserved	Read all masks [3:0]/[7:4]
PIT: 40h	R	Status byte counter 0	1st read: Status byte counter 0 2nd read: CRL for counter 0 3rd read: CRM for counter 0 4th read: CRL for counter 1 5th read: CRM for counter 1 6th read: CRL for counter 2 7th read: CRM for counter 2
PIT: 41h	R	Status byte counter 1	Status byte counter 1
PIT: 42h	R	Status byte counter 2	Status byte counter 2
PIC: 20h	R	Interrupt request register for PIC 1	1st read: ICW1 for controller 1 2nd read: ICW2 for controller 1 3rd read: ICW3 for controller 1 4th read: ICW4 for controller 1 5th read: OCW1 for controller 1 6th read: OCW2 for controller 1 7th read: OCW3 for controller 1 8th read: ICW1 for controller 2 9th read: ICW2 for controller 2 10th read: ICW3 for controller 2 11th read: ICW4 for controller 2 12th read: OCW1 for controller 2 13th read: OCW2 for controller 2 14th read: OCW3 for controller 2
PIC: 21h	R	In service register for PIC 1	In service register for PIC 1
PIC: A0h	R	Interrupt request register for PIC 2	Interrupt request register for PIC 2
PIC: A1h	R	In service register for PIC 2	In service register for PIC 2

NMIDIS. NMI disable. Read only. This provides read access to RTC70[NMIDIS].

P92FR. Port 92 fast reset. Read-write. 1=Writes that attempt to set PORT92[0]—the fast CPU reset bit—are enabled. 0=Writes to PORT92[0] are ignored.

MBL. Must be low. Read-write. This bit is required to be low at all times; otherwise undefined behavior will result.

C0A43: ROM Decode Control Register
Configuration space; function 0; offset: 43h Default: 00h Read-write.

This register specifies the address space mapped to the BIOS ROM on either the ISA bus or the LPC bus (based on the state of C3A48[ISABIOS]). The ROM_KBCS# pin is used to enable accesses to the system BIOS on the ISA bus. LPC bus accesses are decoded by the LPC BIOS device with the LPC address map shown below.

7:0
SEGEN

SEGEN. ROM segment enables. For each of these bits: 1=Enables the specified address range as a BIOS ROM access. 0=The specified address range is not decoded as a BIOS ROM access. These bits control the following address ranges; the last column shows the translated LPC bus addresses if C3A48[ISABIOS]=0; the next column shows the translated ISA bus address if C3A48[ISABIOS]=1:

SEGEN bit	Size	PCI Address Range[31:0]	Address translation for ISA bus[23:0]	Address translation for LPC bus
0	32K bytes	000C_0000 - 000C_7FFFh	FC_0000 - FC_7FFFh	FFFC_0000 - FFFC_7FFFh
1	32K bytes	000C_8000 - 000C_FFFFh	FC_8000 - FC_FFFFh	FFFC_8000 - FFFC_FFFFh
2	32K bytes	000D_0000 - 000D_7FFFh	FD_0000 - FD_7FFFh	FFFD_0000 - FFFD_7FFFh
3	32K bytes	000D_8000 - 000D_FFFFh	FD_8000 - FD_FFFFh	FFFD_8000 - FFFD_FFFFh
4	32K bytes	000E_0000 - 000E_7FFFh	FE_0000 - FE_7FFFh	FFFE_0000 - FFFE_7FFFh
5	32K bytes	000E_8000 - 000E_FFFFh	FE_8000 - FE_FFFFh	FFFE_8000 - FFFE_FFFFh
6	1 megabyte	FFB0_0000 - FFBF_FFFFh	B0_0000 - BF_FFFFh	FFB0_0000 - FFBF_FFFFh
7	4 megabytes	FFC0_0000 - FFFF_FFFFh	C0_0000 - FF_FFFFh	FFC0_0000 - FFFF_FFFFh

Note: The following ranges are fixed BIOS address ranges:

	Size	PCI Address Range[31:0]	Address translation for ISA bus[23:0]	Address translation for LPC bus
	64K bytes	000F_0000 - 000F_FFFFh	FF_0000 - FF_FFFFh	FFFF_0000 - FFFF_FFFFh
	64K bytes	FFFF_0000 - FFFF_FFFFh	FF_0000 - FF_FFFFh	FFFF_0000 - FFFF_FFFFh

Note: See C0A80 for further information about how access to BIOS spaces is controlled.

C0A46: Miscellaneous Control 1 Register
Configuration space; function 0; offset: 46h Default: 00h Read-write.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PMWE

PMWE. Posted memory write enable. 1=Enable the one-DWORD write buffer from PCI target memory writes to the ISA/LPC bus. 0=The IC waits until the ISA/LPC cycle is complete before passing ready back to the PCI bus.

C0A47: Miscellaneous Control 2 Register
Configuration space; function 0; offset: 47h Default: 00h

7	6	5	4	3	2	1	0
CPURS	PCIDTEN	Reserved	Reserved	Reserved	Reserved	Reserved	SWPCIR

SWPCIR. Software PCI reset. Write only. When this bit is written with a 1, a 1.5 to 2.0 millisecond reset pulse is generated over PCIRST# and CPURST#.
PCIDTEN. PCI delayed transaction enable. Read-write. 1=PCI accesses that target the ISA/LPC bus and internal legacy registers utilize delayed-transactions. 0=PCI accesses that target the ISA/LPC bus and internal legacy registers are terminated after the ISA/LPC bus cycle is complete. This bit does not affect posted memory writes (C0A46[PMWE]=1), for which always disconnect with data. Note: When PCIDTEN=0, the state of C0A4A[PGNT1ST] is ignored and the IC always waits for the PCI bus to be granted to the LPC DMA/master state machine before asserting the DACK# signal. It is expected that PCIDTEN is normally set high.
CPURS. CPU reset select. Read-write. 1=Processor resets are directed toward the INIT# pin. 0=Processor resets are directed toward the CPURST# pin. This bit is required to be high.

C0A48: Miscellaneous Control 3 Register
Configuration space; function 0; offset: 48h Default: 00h Read-write.

7	6	5	4:3	2	1	0
MBL	Reserved	Reserved	SUB	IUSBEN#	IDEEN#	Reserved

IDEEN#. EIDE controller enable. 1=Access to all EIDE configuration and IO space registers disabled.
IUSBEN#. Internal USB controller enable. 1=Access to all USB configuration and memory space registers disabled.
SUB. Subtractive decoding select. Specifies how subtractive-decoding is handled by the IC. 00b=Subtractive-decoding cycles claimed by the IC and routed to the ISA bus. 01b=Subtractive-decoding cycles claimed by the IC and routed to the LPC bus. 1xb=Subtractive-decoding cycles not claimed by the IC.
MBL. Must be low. Read-write. This bit is required to be low at all times; otherwise undefined behavior will result.

C0A49: Miscellaneous Control 4 Register
Configuration space; function 0; offset: 49h Default: 08h.

Bits[2:1] may be used to lock out accesses to 8-byte blocks of CMOS RAM.

7	6	5	4	3	2	1	0
Reserved	MBL	Reserved	Reserved	ISA12MA	CMLK_B8	CMLK_38	PRISCH

PRISCH. PCI access priority. Read-write. Specifies the priority order for the IC's masters that access the PCI bus as follows:

PRISCH	Priority from highest to lowest
0	(1) ISA/LPC bus; (2) USB controller; (3) IDE controller
1	(1) ISA/LPC bus; (2) IDE controller; (3) USB controller

CMLK_38. CMOS RAM offsets 38h through 3Fh lock. Read; write 1 only. 0=Accesses to the eight bytes of CMOS RAM (powered by the VDD_AL plane) addressed from 38h to 3Fh are read-write accessible. 1=Writes to these bytes are ignored and read always return FFh (regardless as to which of the IO ports from 70h to 73h are used for the access). After this bit is set high, it can only be cleared by PWRGD reset.
CMLK_B8. CMOS RAM offsets B8h through BFh lock. Read; write 1 only. 0=Accesses to the eight bytes of CMOS RAM (powered by the VDD_AL plane) addressed from B8h to BFh are read-write accessible. 1=Writes to these bytes are ignored and read always return FFh (regardless as to which of the IO ports from 70h to 73h are used for the access). After this bit is set high, it can only be cleared by PWRGD reset.
ISA12MA. ISA bus selected to be 12 milliamps. Read-write. 1=The ISA bus signals source and sink up to 12 milliamps. 0=The ISA bus signals source and sink up to 24 milliamps. Signals affected by this bit are BCLK, IOR#, IOW#, MEMR#, MEMW#, LA, SA, and SD.
MBL. Must be low. Read-write. This bit is required to be low at all times; otherwise undefined behavior will result.

C0A4A: IDE Interrupt Routing Register
Configuration space; function 0; offset: 4Ah Default: 84h Read-write.

7	6	5	4	3:2	1:0
PGNT1ST	Reserved	Reserved	Reserved	MBLD	MBLD

MBLD. Must be left in their default state. Read-write. These bits are required to be left in their default state; otherwise undefined behavior will result.
PGNT1ST. PCI grant before DMA acknowledge. 1=The IC waits until the PCI bus is granted before DMA acknowledge is asserted to the LPC bus DMA controller for DMA/master LPC cycles. 0=DMA acknowledge is asserted regardless of whether the PCI bus is granted to the IC. It is expected that this bit is normally low. Note: When C0A47[PCIDTEN]=0, the state of C0A4A[PGNT1ST] is ignored and the IC always waits for the PCI bus to be granted to the LPC DMA/master state machine before asserting the DACK# signal to DMA controller.

C0A4B: IOAPIC Configuration Register

Configuration space; function 0; offset: 4Bh Default: 00h Read-write.

7:5	4:3	2	1	0
Reserved	APICCKS[1:0]	SCI2IOA	SMI2IOA	APICEN

APICEN. IOAPIC enable. 0=Accesses to the IOAPIC memory space are routed to the ISA/LPC bus and the interrupt message bus is not used. 1=The IOAPIC is enabled, accesses to the IOAPIC memory space are not reflected on the ISA/LPC bus, and the interrupt message bus is used to transmit IOAPIC interrupts.

SMI2IOA. SMI to IOAPIC redirection register 23. 1=The SMI output of the power management logic is routed through redirection register 23 of the IOAPIC; the SMI# pin is never asserted. 0=IRQ23 of the IOAPIC is driven with the output of the GPIO17 input path (regardless as to the state of PMD1) and the SMI# pin is controlled by the IC.

SCI2IOA. SCI to IOAPIC redirection register 22. 1=The SCI output of the power management logic is routed through redirection register 22 of the IOAPIC; C3A42[SCISEL] disabled. 0=IRQ22 of the IOAPIC is driven with the output of the GPIO16 input path (regardless as to the state of PMD0); C3A42[SCISEL] functions normally.

APICCKS. APIC clock select. Selects the source and frequency of the PICCLK as follows:

APICCKS[1:0]	Frequency	Source
00b	PCLK divided by 4 (8.3 MHz. max)	The IC drives PICCLK.
01b	PCLK divided by 2 (16.7 MHz. max)	The IC drives PICCLK.
10b	PCLK (33.3 MHz. max)	The IC drives PICCLK.
11b	Unknown. Note: In this mode, the external clock source is required to be 33.3 MHz or less.	PICCLK is driven by an external component.

C0A51: LPC Bus Decode Register 0

Configuration space; function 0; offset: 51h Default: 00h Read-write.

7	6	5	4	3	2	1:0
ACPI	KBDC	FDC2	FDC1	ECP	Reserved	PRANGE

PRANGE and ECP. Parallel port range and ECP enable. Specifies which parallel port IO range to route to the LPC bus as follows:

PRANGE	ECP = 0	ECP = 1
00b	3BC - 3BFh	3BC - 3BFh and 7BC - 7BFh
01b	378 - 37Fh	378 - 37Fh and 778 - 77Fh
10b	278 - 27Fh*	278 - 27Fh and 678 - 67Fh*
11b	None	None

* Note: Port 279h is read-only for LPC. Writes are forwarded to the ISA bus.

FDC1. Floppy drive controller 1. 1=IO ports 3F0h - 3F5h and 3F7h is are routed to LPC. 0=These accesses are routed to the ISA bus.

FDC2. Floppy drive controller 2. 1=IO ports 370h – 375h and 377h is are routed to LPC. 0=These accesses are routed to the ISA bus.

KBDC. Keyboard controller. 1=When USB keyboard emulation is not enabled via HceControl[0] (offset 100h in USBxxx space), IO ports 60h and 64h are routed to LPC. 0=When USB keyboard emulation is not enabled, IO ports 60h and 64h are routed to ISA. If USB keyboard emulation is enabled, these cycles are routed to the USB block.

ACPI. ACPI controller. 1= IO ports 62h and 66h are routed to LPC. 0=These accesses are routed to the ISA bus.

C0A52: LPC Bus Decode Register 1

Configuration space; function 0; offset: 52h Default: 00h Read-write.

7	6:4	3	2:0
SBEN	SBRANGE	SAEN	SARANGE

SARANGE and SBRANGE. Serial port A and B range. Selects the serial port IO ranges routed to the LPC bus.

S[A,B]RANGE	Range	S[A,B]RANGE	Range
000b	3F8 - 3FFh (COM1)	100b	238 - 23Fh
001b	2F8 - 2FFh (COM2)	101b	2E8 - 2EFh (COM4)
010b	220 - 227h	110b	338 - 33Fh
011b	228 - 22Fh	111b	3E8 - 3EFh (COM3)

SAEN and SBEN. Serial ports A and B enable. 1=Serial port IO port accesses specified by the corresponding RANGE field in this register are routed to the LPC bus (SAEN enables SARANGE and SBEN enables SBRANGE). 0=These accesses are routed to the ISA bus.

C0A53: LPC Bus Decode Register 2

Configuration space; function 0; offset: 53h Default: 00h Read-write.

7	6	5:4	3	2	1:0
Reserved	MEN	MRANGE	AL	AEN	ARANGE

ARANGE. Audio range. Selects the audio device range routed to the LPC bus as follows:

ARANGE	Range
00b	220 - 233h
01b	240 - 253h
10b	260 - 273h
11b	280 - 293h

AEN. Audio enable. 1=Audio IO port accesses specified by the ARANGE field in this register are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

AL. Audio legacy enable. 1=Audio legacy IO ports, 388h - 389h, are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

MRANGE. MIDI range. Selects the MIDI device range routed to the LPC bus as follows:

MRANGE	Range
00b	300 - 301h
01b	310 - 311h
10b	320 - 321h
11b	330 - 331h

MEN. MIDI enable. 1=MIDI IO port accesses specified by the MRANGE field in this register are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

C0A54: LPC Bus Decode Register 3

Configuration space; function 0; offset: 54h. Default: 00h. Read-write.

7:6	5	4	3	2	1:0
Reserved	ASIO	SIO	RESERVED	MSEN	MSRANGE

MSRANGE. MSS range. Selects the MSS device range routed to the LPC bus as follows:

MSRANGE	Range
00b	530 - 537h
01b	604 - 60Bh
10b	E80 - E87h
11b	F40 - F47h

MSEN. MSS enable. 1=MSS IO port accesses specified by the MSRANGE field in this register are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

SIO. Super IO configuration. 1=Super IO configuration IO ports, 2Eh - 2Fh, are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

ASIO. Alternate super IO configuration. 1=Alternate super IO configuration IO ports, 4Eh - 4Fh, are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

C0A55: LPC Bus Decode Register 4
Configuration space; function 0; offset: 55h. Default: 00h. Read-write.

7:5	4	3:0
Reserved	GP1EN	GP1RANGE

GP1RANGE. Game port 1 range. Selects one byte of IO address space in the range 200h - 20Fh (where GP1RANGE specifies the four LSBs of the address) that is routed to the LPC bus.
GP1EN. Game port 1 enable. 1=Game port 1 accesses specified by the GP1RANGE field in this register are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

C0A56: LPC Bus Decode Register 5
Configuration space; function 0; offset: 56h. Default: 00h. Read-write.

7:5	4	3:0
Reserved	GP2EN	GP2RANGE

GP2RANGE. Game port 2 range. Selects one byte of IO address space in the range 200h - 20Fh (where GP2RANGE specifies the four LSBs of the address) that is routed to the LPC bus.
GP2EN. Game port 2 enable. 1=Game port 2 accesses specified by the GP2RANGE field in this register are routed to the LPC bus. 0=These accesses are routed to the ISA bus.

C0A58: LPC Bus Generic IO Decode Register
Configuration space; function 0; offset: 5B-58h. Default: 0000_DE01h. Read-write.

31:16	15:9	8:0
Reserved	IOBASE	Reserved

IOBASE. Generic IO base address. Specifies bits [15:9] of the base address for a 512-byte generic IO address range that is routed to the LPC bus. This function is disabled if IOBASE is set to 00h.

C0A5C: LPC Bus Generic Memory Decode Register
Configuration space; function 0; offset: 5F-5Ch. Default: 0000_0000h. Read-write.

31:20	19:0
MEMBASE	Reserved

MEMBASE. Generic memory base address. Specifies bits [31:20] of the base address for a 1-megabyte generic memory address range that is routed to the LPC bus. This function is disabled if MEMBASE is set to 000h.

C0A70: Device and Subsystem ID Read-Write Register
Configuration space; function 0; offset: 73-70h. Default: 0000_0000h. Read-write.

31:16	15:0
SSID	SSVENDORID

SSVENDORID and SSID. Subsystem vendor ID and Subsystem ID. The value placed in this register is visible in C0A2C, C1A2C, C3A2C, and C4A2C.

C0A80/C0A84/C0A88: BIOS Access Control Register
Configuration space; function 0; offset: 8B-80h. Default: 0000_0000h. Read-write. These registers include 24 4-bit registers called OAR (open at reset) locks. Each 4-bit register applies to a sector of the BIOS in the 5 megabyte BIOS range at the top of the 4-gigabyte address space as follows:

C0A84 and C0A80 include 16 four-bit lock registers, OARx where x ranges from 0h to Fh; each four-bit register controls a 64Kbyte address range at the top megabyte of memory as follows: [FFF(x)_FFFFh: FFF(x)_0000h].

C0A88 includes 8 four-bit lock registers, OARx where x ranges as [E, C, A, 8, 6, 4, 2, 0]; each four-bit register controls an 8Kbyte address range as follows: [FFBF_(x+1)FFFh: FFBF_(x)000h].

Accesses to BIOS space in the low megabyte (between 000C_0000h and 000F_FFFFh) are mapped to the top megabyte (between FFFC_0000h and FFFF_FFFFh) on the LPC bus; the OAR locks for these—whether the LPC bus or ISA bus is targeted—apply to these accesses based on the remapped address at the top megabyte. Note: There is an additional OAR lock specified in C0A8C. Note: OAR locks only apply to BIOS address space; if there is an access to an OAR lock address range that is not in BIOS address space as specified by C0A43, then the OAR lock register is ignored.

PCI special cycles determine when the system is in SMM mode, for the SMM-mode locks. The special cycles data phase determines the system state as follows:

0005_0002h: system is entering SMM mode;
0006_0002h: system is exiting SMM mode.

C0A88:	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
	OARE	OARC	OARA	OAR8	OAR6	OAR4	OAR2	OAR0
C0A84:	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
	OARF	OARE	OARD	OARC	OARB	OARA	OAR9	OAR8
C0A80:	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
	OAR7	OAR6	OAR5	OAR4	OAR3	OAR2	OAR1	OAR0

OARx[0], RDLOCK. BIOS sector x read lock. Read; write if enabled by SLLOCK and FLLOCK. 0=Read access to BIOS sector x enabled. 1=Read access to BIOS sector x disabled.
OARx[1], WRLOCK. BIOS sector x write lock. Read; write if enabled by SLLOCK and FLLOCK. 0=Write access to BIOS sector x enabled (if C0A40[RWR]=1). 1=Write access to BIOS sector x disabled.
OARx[2], SLLOCK. SMM access to RD/WRLOCK lock. Read; write 1 only. This bit may only be set high by software; it is cleared by PCIRST#. 0=Read-write access to RDLOCK and WRLOCK enabled (if FLLOCK=0). 1=Write access to RDLOCK and WRLOCK only enabled in SMM mode (if FLLOCK=0).
OARx[3], FLLOCK. Full access to RD/WRLOCK lock. Read; write 1 only. This bit may only be set high by software; it is cleared by PCIRST#. 0=Read-write access to RDLOCK and WRLOCK enabled. 1=Write access to RDLOCK and WRLOCK disabled (whether the system is in SMM mode or not).

C0A8C: OAR Control Register
Configuration space; function 0; offset: 8Ch. Default: 0000_0000h.

7	6	5	4	3:0
Reserved	Reserved	Reserved	LKLOCK	OAR_ROB

OAR_ROB. OAR locks for rest of BIOS space. Read-write. These four bits are defined identically to the OAR registers in C0A80/84/88. They apply to the BIOS ROM space across [FFEF_FFFFh:FFC0_0000h] (if the space is specified by C0A43 to be BIOS).
LKLOCK. SMM access to the ROM access registers lock. Read; write 1 only. This bit may only be set high by software; it is cleared by PCIRST#. 0=Write access to C0A80/C084/C0A88/C0A8C and C0A43 always enabled. 1=Write access to C0A80/C084/C0A88/C0A8C and C0A43 only enabled in SMM mode (see C0A80 for determination of when the system is in SMM mode).

5.3 Legacy Registers

5.3.1 Miscellaneous Legacy and Fixed IO Address Registers

These registers are in IO space at fixed addresses. See section 5.1.2 for a description of the register naming convention.

PORT61: AT Compatibility Register
Fixed IO space; offset: 61h. Default: 00h.

7	6	5	4	3	2	1	0
SERR	IOCHK	TMR2	RSHCLK	CLRIOCHK	CLRSERR	SPKREN	TMR2EN

TMR2EN. Programmable interval timer, timer number 2 enable. Read-write. 1=PIT timer 2 is enabled to count. 0=PIT timer 2 is halted.
SPKREN. Speaker enable. Read-write. 1=The output of PIT timer number 2 drives the SPKR pin. 0=SPKR is held low.
CLRSERR. Clear PORT61[SERR]. Read-write. 1=Bit[7] of this register, SERR, is asynchronously cleared. 0=PORT61[SERR] may be set high.
CLRIOCHK. Clear PORT61[IOCHK]. Read-write. 1=Bit[6] of this register, IOCHK, is asynchronously cleared. 0=PORT61[IOCHK] may be set high.
RSHCLK. Refresh clock. Read only. This bit toggles state at intervals specified by PIT timer 1 (normally, every 15 microseconds).
TMR2. Programmable interval timer, timer number 2 output. Read only. This bit provides the current state of the output signal from legacy PIT timer number 2.
IOCHK. IOCHK# latch. Read only. This bit is set high when the IOCHK# pin is asserted or if there is a sync-with-error message received on the LPC bus; it stays high until cleared by PORT61[CLRIOCHK]. The state of this bit is combined with RTC70[NMIDIS] and PORT61[SERR] to generate NMI interrupts.
SERR. SERR# latch. Read only. This bit is set high when SERR# is asserted and stays high until cleared by PORT61[CLRSERR]. The state of this bit is combined with RTC70[NMIDIS] and PORT61[IOCHK] to generate NMI interrupts.

PORT92: System Control Register
Fixed IO space; offset: 92h. Default: 00h.

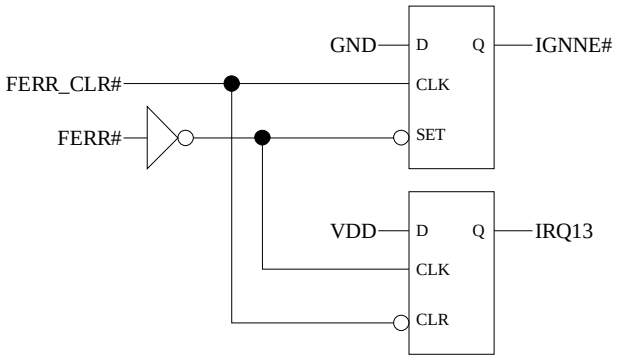
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	A20EN	RSTCPU

RSTCPU. Generate processor reset pulse. Read-write. When this bit is low and then written to a high, the IC generates a 1.0 to 1.5 microsecond pulse to either CPURST# or INIT#, based on the state of C0A47[CPURS]. This bit must be written to a low again before another processor reset can be generated. Note: Use of this bit is enabled by C0A41[P92FR].
A20EN. Processor address bit 20 enable. Write only; reads provide the current state of the A20M# pin rather than the state of the bit. The value written to this bit is ORed with the KA20G bit from the keyboard controller and then routed to the A20M# pin. In order for this bit to control A20M#, KA20G must be low.

PORTF0, PORTF1 and the FERR# and IGNNE# Logic

Fixed IO space; offset: F0h and F1h.

FERR# is used to control IGNNE# and generate IRQ13 to the PIC and IOAPIC. The diagram shows the logic. FERR_CLR# is asserted by (1) an IO write to F0h, (2) an IO write to F1h, (3) any processor reset command, and (4) PWRGD reset; when any of these are active, FERR_CLR# goes low.



PORT4D0: Level Sensitive IRQ Select Register
Fixed IO space; offset: 4D1-4D0h. Default: 0000h. Read-write.

15:8	7:0
LIRQ1	LIRQ0

LIRQ0 and LIRQ1. Level sensitive IRQs. Each of these 16 bits controls whether a corresponding IRQ line that enters the legacy PIC is edge sensitive (if the bit is low) or level sensitive (if it is high). Edge sensitive interrupts must enter the PIC such that the rising edge generates the interrupt and level sensitive interrupts must enter the PIC as active low; see section 4.3.4.1 for details about how the interrupts are mapped to the PIC. The bit numbers correspond directly to the IRQ numbers (e.g., bit[12] controls IRQ12). Bits[0 and 2] are reserved (IRQ0 is always edge sensitive and IRQ2 does not exist).

PORTCF9: Miscellaneous SMI Status Register
Fixed IO space; offset: CF9h. Default: 00h. Note: This register is enabled by C3A41[PCF9EN].

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	FULLRST	RSTCMD	SYSRST	Reserved

SYSRST. System reset. Read-write. This bit specifies whether a full system reset or a processor INIT# interrupt is generated when PORTCF9[RSTCMD] is written to a 1. 1=Full system reset with PCIRST# and CPURST# asserted for 1.5 to 2.0 milliseconds. 0=INIT# asserted for 16 PCI clocks.
RSTCMD. Reset command. Write only; always reads as a zero. 1=A reset is generated as specified by bits[3,1] of this register (bits[3,1] are observed in their state when RSTCMD is written to a 1; their previous value does not matter).
FULLRST. Full reset. Read-write. 1=Full resets require the IC to place the system in the SOFF state for 3 to 5 seconds; full resets occurs whenever (1) RSTCMD and SYSRST are both written high, (2) an AC power fail is detected (PWRGD goes low without the appropriate command), or (3) PM46[2NDTO_STS] is set while C3A48[NO_REBOOT]=0. 0=Full resets do not transition the system to SOFF; only the reset signals are asserted.

5.3.2 Legacy DMA Controller (DMAC) Registers

The legacy DMA controller (DMAC) in the IC supports the features required by the LPC I/F Specification Revision 1.0, which are a subset of the features in legacy DMA Controllers. Single, demand, verify, and increment modes are supported. Block, decrement, cascade modes are not supported. Also, memory-to-memory transfers and external EOPs (end of process) are not supported.

There are 7 supported DMA channels. Channels 0-3 support 8-bit transfers. Channels 5-7 support 16-bit transfers. There is no support for 32-bit DMA transfers. LPC master device requests are made using channel 4.

Although not all registers of legacy DMA controllers are supported, the IO address locations for the unsupported registers is consistent with legacy logic. The implemented DMAC registers are listed in the following table.

Name	Size	Number	Comments
Base Address Registers	16 bits	8	1 for each channel (0-7) (see note 1)
Base Word Count Registers	16 bits	8	1 for each channel (0-7) (see note 1)
Current Address Registers	16 bits	8	1 for each channel (0-7) (see note 1)
Current Word Count Registers	16 bits	8	1 for each channel (0-7) (see note 1)
Status Registers	8 bits	2	1 for Master and 1 for Slave DMAC
Command Registers	1 bit	2	1 for Master and 1 for Slave DMAC
Mode Registers	5 bits	8	1 for each channel (0-7) (see note 1)
Mask Registers	4 bits	2	1 for Master and 1 for Slave DMAC

Note 1: although channel 4 base and current registers exist for compatibility, they are not used.

Note that not all bits in the command and mode registers of legacy DMA controllers are implemented in the IC's DMA controller. The bit usage for these registers are as follows.

Command registers (master and slave DMAC)

Bit	Legacy DMAC function	DMAC function of the IC
7	DACK sense	Obsolete
6	DREQ sense	Obsolete
5	Late/Extended write	Obsolete
4	Fixed/Rotating priority	Obsolete (always fixed priority)
3	Normal/Compressed timing	Obsolete
2	Controller enable/disable	Controller enable/disable
1	Ch0 address hold enable/disable	Obsolete
0	Memory-to-memory enable/disable	Obsolete

Mode registers (master and slave DMAC)

Bit	Legacy DMAC function	DMAC function of the IC
7:6	00b Demand mode select 01b Single mode select 10b Block mode select 11b Cascade mode select	00b Demand mode select 01b Single mode select 10b Obsolete 11b Obsolete (see note)
5	Address increment/decrement select	Obsolete (always increment)
4	Auto initialization enable/disable	Auto initialization enable/disable
3:2	00b Verify transfer 01b Write transfer 10b Read transfer 11b Illegal	00b Verify transfer 01b Write transfer 10b Read transfer 11b Illegal
1:0	Channel select	Channel select

Note: DMA channel 4 is hard-wired into cascade mode; however cascade mode is obsolete for all other channels.

5.3.3 Legacy Programmable Interval Timer (PIT) Registers

These timers are halted from counting, if enabled to do so in C3A4C[PIT_DIS], when PRDY is asserted.

The following are ports used to access the legacy PIT:

Offset	Access	Port
40h	Write	Counter 0 write access port
	Read	Counter 0 read access port
41h	Write	Counter 1 access port
	Read	Counter 1 read access port
42h	Write	Counter 2 access port
	Read	Counter 2 read access port
43h	Write	Control byte
	Read	Not supported

PORT43: PIT Control Byte Register
Fixed IO space; offset: 43h. Default: 00h. Write only.

Bits	Description
7:6	**SC[1:0]: select counter.** Specifies the counter that the command applies to as follows: 00b Counter 0. 01b Counter 1. 10b Counter 2. 11b Read back command.
5:4	**RW[1:0]: read-write command.** Specifies the read-write command as follows: 00b Counter latch command. 01b Read/write least significant byte only. 10b Read/write most significant byte only. 11b Read/write least significant byte followed by most significant byte.
3:1	**M[2:0]: counter mode.** Specifies the mode in which the counter selected by SC[1:0] operates as follows: 000b Interrupt on terminal count. 001b Hardware retriggerable one-shot (not supported). 010b Rate generator. 011b Square wave mode. 100b Software triggered strobe. 101b Hardware triggered (retriggerable) strobe (not supported). 110b When this value is written, 010b is stored in the register, rate generator mode. 111b When this value is written, 011b is stored in the register, square wave mode.
0	**BCD: binary coded decimal.** 1=Counter specified by SC[1:0] operates in binary coded decimal. 0=Counter specified by SC[1:0] operates in 16-bit binary mode.

5.3.4 Legacy Programmable Interrupt Controller (PIC) Registers

The legacy programmable interrupt controller (PIC) includes a master, which is accessed through ports 20h and 21h and controls IRQ[7:0], and a slave, which is accessed through ports A0h and A1h and controls IRQ[15:8].

The following are all the PIC registers.

Offset	Access type	Register
20h (master),	Write only; D[4]=1b	Initialization command word 1 (ICW1)
A0h (slave)	Write only; D[4:3]=00b	Operation command word 2 (OCW2)
	Read-write; D[4:3]=01b	Operation command word 3 (OCW3)
21h (master),	Write only	Initialization command word 2 (ICW2)
A1h (slave)	Write only	Initialization command word 3 (ICW3)
	Write only	Initialization command word 4 (ICW4)
	Read-write	Operation command word 1 (OCW1)

D[4:3] above refers to bits[4:3] of the associated 8-bit data field. Normally, once ICW1 is sent, ICW2, ICW3, and ICW4 are sent in that order before any OCW registers are accessed.

ICW1: Initialization Command Word 1 Register
Fixed IO space; offset: 20h for master and A0h for slave; data bit[4] must be high. Write only.

Bits	Description
7:5	**A[7:5]: interrupt vector address.** These bits are not implemented.
4	This should always be high.
3	**LTIM: level triggered mode.** This bit is not implemented; PORT4D0 controls this function instead.
2	**ADI: call address interval.** This bit is not implemented.
1	**SNGL: single mode.** This bit must be programmed low to indicate cascade mode.
0	**IC4: ICW4 needed.** This bit must be programmed high.

ICW2: Initialization Command Word 2 Register
Fixed IO space; offset: 21h for master and A1h for slave. Write only.

ICW3M: Initialization Command Word 3 for Master Register
Fixed IO space; offset: 21h. Write only.

Bits	Description
7:0	**SLAVES[7:0].** These bits must always be programmed to 04h.

ICW3S: Initialization Command Word 3 for Slave Register
Fixed IO space; offset: A1h. Write only.

Bits	Description
7:3	Reserved (must be programmed to all zeros).
2:0	**ID[2:0].** These bits must always be programmed to 02h.

ICW4: Initialization Command Word 4 Register
Fixed IO space; offset: 21h for master and A1h for slave. Write only.

Bits	Description
7:5	Reserved (must be programmed all zeros)
4	**SFNM.** Special fully nested mode. This bit is normally programmed low.
3:2	**BUFF and MS.** These two are normally programmed to 00b for non-buffered mode.
1	**AEOI.** Auto EOI. This bit is ignored; the IC only operates in normal EOI mode (this bit low).
0	**UPM.** x86 mode. This bit is ignored; the IC only operates in x86 mode (this bit high).

OCW1: Operation Command Word 1 Register

Fixed IO space; offset: 21h for master and A1h for slave. Write only.

Bits	Description
7:0	**MASK[7:0].** Interrupt mask. 1=Interrupt is masked. Masking IRQ2 on the master interrupt controller masks all slave-controller interrupts.

OCW2: Operation Command Word 2 Register

Fixed IO space; offset: 20h for master and A0h for slave; data bits[4:3] must be 00b. Write only.

Bits	Description
7:5	**R (bit 7), SL (bit 6), and EOI (bit 5).** These are decoded as: R, SL, EOI — Function 000b — * Rotate in auto EOI mode clear. 001b — Non-specific EOI mode. 010b — No operation. 011b — Specific EOI command. 100b — * Rotate in auto EOI mode set 101b — Rotate on non-specific EOI command 110b — ** Set priority command 111b — ** Rotate on specific EOI command * Not supported. ** Uses IRLEVEL field.
4:3	Reserved (must be programmed all zeros).
2:0	**IRLEVEL.** Interrupt request level. Specifies the interrupt request level to be acted upon.

OCW3: Operation Command Word 3 Register

Fixed IO space; offset: 20h for master and A0h for slave; data bits[4:3] must be 01b. Write only.

Bits	Description
7	Must be programmed low.
6:5	**ESMM (bit 6) and SMM (bit 5).** Special mask mode. These are decoded as: [ESMM, SMM] = 0Xb No action. [ESMM, SMM] = 10b Reset special mask mode. [ESMM, SMM] = 11b Set special mask mode.
4:3	01b
2	**P: poll command.** 1=Poll enabled; next IO read of the interrupt controller treated like an interrupt acknowledge cycle.
1:0	**RR (bit 1) and RIS (bit 0).** Read register command. These are decoded as: [RR,RIS] = 0Xb No action. [RR,RIS] = 10b Read in-request (IR) register. [RR,RIS] = 11b Read IS register.

5.3.5 IOAPIC Registers

The IOAPIC register set for the 24 IOAPIC interrupts supported by the IC is indexed through two fixed-location, memory-mapped ports: FEC0_0000h, which provides the 8-bit index register, and FEC0_0010h, which provides the 32-bit data port. Writes to the 32-bit data port at FEC0_0010h require that all four bytes be enabled.

The index register selects one of the following:

Index	Description	Attribute	Default
00h	**APIC ID register.** The ID is in bits[27:24]. All other bits are reserved.	Read-write	0000 0000h
01h	**IOAPIC version register.**	Read only	0017 0011h
02h	**IOAPIC arbitration ID register.** The ID is in bits[27:24]. All other bits are reserved.	Read only	0000 0000h
10h-3Fh	**Redirection registers.** Each of the 24 redirection registers uses two of these indexes. Bits[63:32] are accessed through the odd indexes and bits[31:0] are accessed through the even indexes.	Read-write	0000 0000 0001 0000h
40h-FFh	Reserved.		

The redirection registers are defined as follows:

Bits	Description
63:56	**Destination.** In physical mode, bits[59:56] specify the APIC ID of the target processor. In logical mode bits[63:56] specify a set of processors.
55:17	Reserved.
16	**Interrupt mask.** 1=Interrupt is masked.
15	**Trigger mode.** 0=Edge sensitive. 1=Level sensitive.
14	**IRR: interrupt request receipt.** Read only. This bit is not defined for edge-triggered interrupts. For level-triggered interrupts, this bit is set by the hardware after an interrupt is detected. It is cleared by receipt of EOI with the vector specified in bits[7:0].
13	**Polarity.** 0=Active high. 1=Active low.
12	**Delivery status.** 0=Idle. 1=Interrupt message pending.
11	**Destination mode.** 0=Physical mode. 1=Logical mode.
10:8	**Delivery mode.** 000b=fixed. 001b=Lowest priority. 010b=SMI. 011b=Reserved. 100b=NMI. 101=Init. 110b=Reserved. 111b=ExtINT.
7:0	**Interrupt vector.**

5.3.6 Real-Time Clock Registers

RTC70: Real-Time Clock Legacy Indexed Address.
IO mapped (fixed); offset: 0070h. Default: 80h. Write only.

Note: RTC70[6:0] and RTC72 occupy the same physical register; after writes to RTC70, RTC72 reads back as {0b, RTC70[6:0]}; after writes to RTC72, reads of RTC72 provide all 8 bits written.

7	6:0
NMIDIS	RTCADDR

RTCADDR. Real time clock address. Specifies the address of the real-time clock CMOS RAM. The data port associated with this index is RTC71. Only the lower 128 bytes of the CMOS RAM are accessible through RTC70 and RTC71.
NMIDIS. NMI disable. 1=PORT61[IOCHK and SERR] are disabled from being able to generate NMI interrupts to the processor. Note: The state of this register is read accessible through C0A41[NMIDIS].

RTC71: Real-Time Clock Legacy Data Port.
IO mapped (fixed); offset: 0071h. Read-write.

7:0
RTCDATA

RTCDATA. Real time clock data. This is the data port for accesses to the real-time clock CMOS RAM that is indexed by RTC70.

RTC72 and RTC73: Real-Time Clock 256-Byte Address and Data Port.
IO mapped (fixed); offsets: 0072h and 0073h. Read-write.

These two 8-bit ports are similar to RTC70 and RTC71. However, RTC72, the address register, provides the full eight bits needed to access all 256 bytes of CMOS RAM. RTC73, the data port, provides access to the CMOS data indexed by RTC72. See RTC70 for details about reading RTC72.

Real-Time Clock Alarm And Century Registers.
RTC indexed address space (indexed by RTC70); offsets: 7Dh, 7Eh, and 7Fh. Attribute: read-write. The day alarm, month alarm, and centenary value are stored in CMOS RAM indexed address space.

CMOS RAM offset	Function	Range for binary mode	Range for BCD mode
7Dh	Date alarm	01-1Fh	01-31h
7Eh	Month alarm	01-0Ch	01-12h
7Fh	Century field	13-63h	19-99h

Bits[7:6] of the date alarm (offset 7Dh) are reserved; writes to them have no effect and they always read back as zero. To place the RTC into 24-hour alarm mode, an invalid code must be written to bits[5:0] of the date alarm byte (anything other than 01h to 31h for BCD mode or 01h to F1h for hex mode). Refer to the ACPI specification for specifics on the month alarm field (offset 7Eh) and century field (offset 7Fh) functionality.

5.4 Enhanced IDE Controller Configuration Registers (C1Axx)

These registers are in PCI configuration space, function 1. See section 5.1.2 for a description of the register naming convention.

C1A00: EIDE Controller Vendor And Device ID
Configuration space; function 1; offset: 03-00h. C1A00 default: 7411 1022h. Read only.

31:16	15:0
DID	VID

VID. Vendor ID.
DID. EIDE controller device ID.

C1A04: EIDE Controller Status And Command Register
Configuration space; function 1; offset: 07-04h. Default: 0200 0000h.

31:16	15:0
STATUS[15:0]	COMMAND[15:0]

COMMAND[0] IO Space, IOEN. Read-write. 1=Enables access to the IO space for the EIDE controller.
COMMAND[1] Memory Space. Read only. This bit is fixed in the low state.
COMMAND[2] Bus Master Enable, BMEN. Read-write. 1=Enables EIDE bus master capability.
COMMAND[15:3]. Read only. These bits are fixed at their default values.
STATUS[11:0]. Read only. These bits are fixed at their default values.
STATUS[12] Received Target Abort, RTGTABT. Read; set by hardware; write 1 to clear. 1=The IC received a target abort while the EIDE controller was master of the PCI bus.
STATUS[13] Received Master Abort, RMASABT. Read; set by hardware; write 1 to clear. 1=An EIDE master cycle was terminated with a master abort.
STATUS[15:14]. Read only. These bits are fixed at their default values.

C1A08: EIDE Revision ID, Programming Interface, Sub Class and Base Registers
Configuration space; function 1; offset: 0B-08h. Default: 0101 8A01h.

31:24	23:16	15:8	7:0
BASE CLASS	SUB CLASS	PROG I/F[7:0]	REVISION ID

REVISION ID. Read only. EIDE controller silicon revision.
PROG I/F[0] Primary native mode. Read-write. 0=Compatibility mode for primary port; C1A10 and C1A14 are ignored and not visible; address decode is based on legacy addresses 1F0-1F7h, 3F6h; C1A3C[7:0] read-only zeros; C1A3C[15:8] = 00h; IRQ14 an ISA bus interrupt that may be used by the IDE controller. 1=native mode; C1A10 and C1A14 are visible and used for address decode; C1A3C[7:0] read-write; C1A3C[15:8] = 01h; IRQ14 pin becomes NMPIRQ, used exclusively by the primary IDE port.
PROG I/F[1] Primary native/compatibility mode selectable. Read only. This is high to indicate that PROG I/F[0] is read-write.
PROG I/F[2] Secondary native mode. Read-write. 0=compatibility mode for secondary port; C1A18 and C1A1C are ignored and not visible; address decode is based on legacy addresses 170-177h, 376h; C1A3C[7:0] read-only zeros; C1A3C[15:8] = 00h; IRQ15 an ISA bus interrupt that may be used by the IDE controller. 1=native mode; C1A18 and C1A1C are visible and used for address decode; C1A3C[7:0] read-write; C1A3C[15:8] = 01h; IRQ15 pin becomes NMSIRQ, used exclusively by the secondary IDE port.
PROG I/F[3] Secondary native/compatibility mode selectable. Read only. This is high to indicate that PROG I/F[2] is read-write.
PROG I/F[6:4]. Read only. These bits are fixed in the low state.
PROG I/F[7] Master IDE Capability. Read only. This bit is fixed in the high state.
SUB CLASS[7:0]. Read only. These bits are fixed at 01h indicating an IDE controller.
BASE CLASS[7:0]. Read only. These bits are fixed at 01h indicating a mass storage device.

C1A0C: EIDE Controller BIST, Header and Latency Register
Configuration space; function 1; offset: 0F-0Ch. Default: 0000 0000h.

31:24	23:16	15:8	7:0
BIST	HEADER	LATENCY	CACHE

CACHE. Read only. These bits are fixed at their default values.
LATENCY. Read-write. This field controls no hardware.
HEADER. Read only. These bits are fixed at their default values.
BIST. Read only. These bits are fixed at their default values.

C1A10: EIDE Controller Primary Command Base Address
Configuration space; function 1; offset: 13-10h. Default: 0000 01F1h. Read-write. When C1A08[8] is low, the primary port is in compatibility mode and this register is ignored and not visible (reads as 0h).

31:3	2:0
BASE	Reserved.

BASE[31:3] Port Address. These bits specify an 8-byte IO address space that maps to the ATA-compliant command register set for the primary port (legacy IO space 1F0h through 1F7h).

C1A14: EIDE Controller Primary Control Base Address
Configuration space; function 1; offset: 17-14h. Default: 0000 03F5h. Read-write. When C1A08[8] is low, the primary port is in compatibility mode and this register is ignored and not visible (reads as 0h).

31:2	1:0
BASE	Reserved.

BASE[31:2] Port Address. These bits specify a 4-byte IO address space that maps to the ATA-compliant control register set for the primary port (legacy IO space 3F6h). Note: Only byte 2 of this space is used.

C1A18: EIDE Controller Secondary Command Base Address
Configuration space; function 1; offset: 1B-18h. Default: 0000 0171h. Read-write. When C1A08[10] is low, the secondary port is in compatibility mode and this register is ignored and not visible (reads as 0h).

31:3	2:0
BASE	Reserved.

BASE[31:3] Port Address. These bits specify an 8-byte IO address space that maps to the ATA-compliant command register set for the secondary port (legacy IO space 170h through 177h).

C1A1C: EIDE Controller Secondary Control Base Address
Configuration space; function 1; offset: 1F-1Ch. Default: 0000 0375h. Read-write. When C1A08[10] is low, the secondary port is in compatibility mode and this register is ignored and not visible (reads as 0h).

31:2	1:0
BASE	Reserved.

BASE[31:2] Port Address. These bits specify a 4-byte IO address space that maps to the ATA-compliant control register set for the secondary port (legacy IO space 376h). Note: Only byte 2 of this space is used.

C1A20: EIDE Controller Bus Master Control Registers Base Address
Configuration space; function 1; offset: 23-20h. Default: 0000 CC01h. Read-write.

31:4	3:0
BASE	‘b0001

BASE[31:4] Port Address. These bits specify the 16-byte IO address space that maps to an EIDE register set that is compliant with the SFF 8038I rev. 1.0 specification (Bus Master Programming Interface for IDE ATA Controllers), IBMx.

C1A2C: EIDE Controller Subsystem ID and Subsystem Vendor ID Register
Configuration space; function 1; offset: 2F-2Ch. Default: 0000_0000h. Read-only.

31:16	15:0
SSID	SSVENDORID

SSVENDORID and SSID. Subsystem vendor ID and subsystem ID registers. This register is write accessible through C0A70.

C1A3C: EIDE Controller Interrupt Line, Interrupt Pin, Min Grant, Max Latency Register
Configuration space; function 1; offset: 3F-3Ch. Default: 0000 0000h.

31:24	23:16	15:8	7:0
MAX LATENCY	MIN GNT	INTERRUPT PIN	INTERRUPT LINE

INTERRUPT LINE. This register is either read-write or read-only based on the state of C1A08[10,8]. When either C1A08[8] or C1A08[10] is high, then this is a read-write register. When they are both low, then it is a read-only register, reading 00h. This register controls no hardware.
INTERRUPT PIN. Read only. When either C1A08[8] or C1A08[10] is high, then field reads 01h. When they are both low, it reads 00h.
MIN GNT. Read only. These bits are fixed at their default values.
MAX LATENCY. Read only. These bits are fixed at their default values.

C1A40: EIDE Controller Configuration Register
Configuration space; function 1; offset: 43-40h. Default: 0000 0400h.

31:24	23:20	19:16	15:0
Reserved	RW	CABLE	IDE_CONFIG

IDE_CONFIG[0] Secondary Channel Enable, SECEN. Read-write. 1=The secondary port of the EIDE controller is enabled.
IDE_CONFIG[1] Primary Channel Enable, PRIEN. Read-write. 1=The primary port of the EIDE controller is enabled.
IDE_CONFIG[4:2] MBLD. Must be left in their default state. Read-write. These bits are required to be left in their default state; otherwise undefined behavior will result.
IDE_CONFIG[7:5] Reserved**.**
IDE_CONFIG[11:8] MBLD. Must be left in their default state. Read-write. These bits are required to be left in their default state; otherwise undefined behavior will result.
IDE CONFIG[12] Secondary Posted Write Buffer, SECPWB. Read-write. 1=Enable the EIDE secondary port PIO-mode posted-write buffer. Only 32-bit writes to the data port are allowed when this bit is set.
IDE CONFIG[13] Secondary Read Prefetch Buffer, SECRPB. Read-write. 1=Enable the EIDE secondary port read-prefetch buffer.
IDE CONFIG[14] Primary Posted Write Buffer, PRIPWB. Read-write. 1=Enable the EIDE primary port PIO-mode posted-write buffer. Only 32-bit writes to the data port are allowed when this bit is set.
IDE CONFIG[15] Primary Read Prefetch Buffer, PRIRPB. Read-write. 1=Enable the EIDE primary port read-prefetch buffer.
CABLE. Read-write. These bits are expected to be programmed by BIOS to specify the cable type of each of the IDE drives to the driver. 1=High speed 80-pin cable is present. The bits specify the drive as follows:

- Bit[16]: primary master.
- Bit[17]: primary slave.
- Bit[18]: secondary master.
- Bit[19]: secondary slave.

RW. Read-write. These bits are read-write accessible through software; they control no hardware.

C1A48: EIDE Controller Drive Timing Control
Configuration space; function 1; offset: 4B-48h. Default: A8A8 A8A8h. Read-write.

This register specifies timing for PIO data transfers (not 171h though 177h or 1F1h though 1F7h) and multi-word DMA transfers. The value in each 4-bit field, plus one, specifies a time period in 30 nanosecond PCI clocks. Note: The default state, A8h, results in a recovery time of 270ns and an active pulse width of 330ns for a 30ns PCI clock (total cycle time = 600ns) which corresponds to ATA PIO Mode 0.

Note: PIO modes are controlled via C1A48 and C1A4C. To set the timing associated with the various modes, C1A4C should be left at its default value and the appropriate byte of C1A48 should be programmed as follows: mode 0=A8h; mode 1=65h; mode 2=42h; mode 3=22h; mode 4=20h.

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
PD0PW	PD0RT	PD1PW	PD1RT	SD0PW	SD0RT	SD1PW	SD1RT

SD1RT[3:0] Secondary Drive 1 Minimum Recovery Time.
SD1PW[3:0] Secondary Drive 1 Active Pulse Width.
SD0RT[3:0] Secondary Drive 0 Minimum Recovery Time.
SD0PW[3:0] Secondary Drive 0 Active Pulse Width.
PD1RT[3:0] Primary Drive 1 Minimum Recovery Time.
PD1PW[3:0] Primary Drive 1 Active Pulse Width.
PD0RT[3:0] Primary Drive 0 Minimum Recovery Time.
PD0PW[3:0] Primary Drive 0 Active Pulse Width.

C1A4C: EIDE Controller Cycle Time and Address Setup Time Register
Configuration space; function 1; offset: 4F-4Ch. Default: FFFF 00FFh. Read-write.

For bits[7:0] the value in each 2-bit field, plus one, specifies the address setup time in 30 nanosecond PCI clocks; this applies to all PIO and multi-word DMA cycles. For bits[31:16] the value in each 4-bit field, plus one, specifies the time in 30 nanosecond PCI clocks; this applies address ports 171h though 177h, 1F1h though 1F7h, 376h, and 3F6h. For 170h and 1F0h, see C1A48.

31:28	27:24	23:20	19:16	15:8	7:6	5:4	3:2	1:0
PXPW	PXRT	SXPW	SXRT	Reserved	P0ADD	P1ADD	S0ADD	S1ADD

S1ADD[1:0] Secondary Drive 1 Address Setup Time.
S0ADD[1:0] Secondary Drive 0 Address Setup Time.
P1ADD[1:0] Primary Drive 1 Address Setup Time.
P0ADD[1:0] Primary Drive 0 Address Setup Time.
SXRT[3:0] Secondary Non-170 DIOR#/DIOW# Recovery Time.
SXPW[3:0] Secondary Non-170 DIOR#/DIOW# Active Pulse Width.
PXRT[3:0] Primary Non-1F0 DIOR#/DIOW# Recovery Time.
PXPW[3:0] Primary Non-1F0 DIOR#/DIOW# Active Pulse Width.

C1A50: EIDE Controller UDMA Extended Timing Control Register
Configuration space; function 1; offset: 53-50h. Default: 0303 0303h.

Each byte of this register controls UDMA mode for access to the specified drive. Bits[7:0] specify the secondary slave drive; bits[15:8] specify the secondary master drive; bits[23:16] specify the primary slave drive; and bits[31:24] specify the primary master drive.

31:24	23:16	15:8	7:0
P0UDMA	P1UDMA	S0UDMA	S1UDMA

[P0, P1, S0, S1]UDMA[2:0] [Primary, Secondary] Drive [1,0] Cycle Time, [P0, P1, S0, S1]CYCT. Read-write.

Bits[2:0]	UDMA mode	Cycle time
0	UDMA mode 2	60 nanoseconds
1	UDMA mode 1	90 nanoseconds
2	UDMA mode 0	120 nanoseconds
3	Slow UDMA mode 0	150 nanoseconds
4	UDMA mode 3	45 nanoseconds
5	UDMA mode 4	30 nanoseconds
6	UDMA mode 5	20 nanoseconds

[P0, P1, S0, S1]UDMA[5:3]. Read only. These bits are fixed at their default values.
[P0, P1, S0, S1]UDMA[6] [Primary, Secondary] Drive [1,0] Ultra DMA Mode Enable, [P0, P1, S0, S1]UDMAEN. Read-write. 1=Enable UDMA mode.
[P0, P1, S0, S1]UDMA[7] [Primary, Secondary] Drive [1,0] Ultra DMA Mode Enable Method, [P0, P1, S0, S1]ENMODE. Read-write. 1=Enable UDMA mode by setting bit 6 of this register. 0=Enable UDMA mode by detecting the "Set Feature" ATA command.

5.5 Enhanced IDE Controller IO Registers

These registers are in IO space. The base address register is C1A20. See section 5.1.2 for a description of the register naming convention.

These registers comply with SFF 8038i for control of DMA transfers between drives and system memory.

IBM0: Primary Bus Master IDE Command Register
IO mapped (base pointers: C1A20); offset: 00h. Default: 00h.

7:0
PCMD

PCMD[0] Start/Stop Bus Master, STSP. Write 1 only. Reads always return zero.
PCMD[2:1]. Reserved.
PCMD[3] Read or Write Control, RW. Read-write. 1=Read cycles specified (read from the drive; write to system memory). 0=Write cycles specified.
PCMD[7:4]. Reserved.

IBM2: Primary Bus Master IDE Status Register
IO space (base pointers: C1A20); offset: 02h. Default: 00h.

7:0
PSTAT

PSTAT[0] Bus Master IDE Active, ACTV. Read only.
PSTAT[1] Error, ERR. Read; set by hardware; write 1 to clear.
PSTAT[2] Interrupt, IRQ. Read; set by hardware; write 1 to clear. This bit is set by the rising edge of the IDE interrupt line.
PSTAT[4:3]. Reserved.
PSTAT[5] Drive 0 DMA Capable, DMA0C. Read-write.
PSTAT[6] Drive 1 DMA Capable, DMA1C. Read-write.
PSTAT[7] Simplex Only. Read only.

IBM4: Primary Bus Master IDE PRD Table Address Register
IO space (base pointers: C1A20); offset: 07-04h. Default: 0000 0000h.

31:2	1:0
PPRDADD	Reserved

PPRDADD[1:0]. Read only. These bits are fixed in the low state
PPRDADD[31:2] Primary physical region descriptor table base address, PRDADD. Read-write.

IBM8: Secondary Bus Master IDE Command Register
IO space (base pointers: C1A20); offset: 08h. Default: 00h.

7:0
SCMD

SCMD[0] Start/Stop Bus Master, STSP. Write 1 only. Reads always return zero.
SCMD[2:1]. Reserved.
SCMD[3] Read or Write Control, RW. Read-write. 1=Read cycles specified (read from the drive; write to system memory).
SCMD[7:4]. Reserved.

IBMA: Secondary Bus Master IDE Status Register
IO space (base pointers: C1A20); offset: 0Ah. Default: 00h.

7:0
SSTAT

SSTAT[0] Bus Master IDE Active, ACTV. Read only.
SSTAT[1] Error, ERR. Read; set by hardware; write 1 to clear.
PSTAT[2] Interrupt, IRQ. Read; set by hardware; write 1 to clear. This bit is set by the rising edge of the IDE interrupt line.
SSTAT[4:3]. Reserved.
SSTAT[5] Drive 0 DMA Capable, DMA0C. Read-write.
SSTAT[6] Drive 1 DMA Capable, DMA1C. Read-write.
SSTAT[7] Simplex Only. Read only.

IBMC: Secondary Bus Master IDE PRD Table Address Register
IO space (base pointers: C1A20); offset: 0Ch. Default: 0000 0000h.

31:2	1:0
PPRDADD	Reserved

SPRDADD[1:0]. Read only. These bits are fixed in the low state
SPRDADD[31:2] Secondary physical region descriptor table base address, SRDADD. Read-write.

5.6 USB Host Controller Configuration Registers (C4Axx)

These registers are in PCI configuration space, function 4. See section 5.1.2 for a description of the register naming convention.

C4A00: USB Controller Vendor And Device ID
Configuration space; function 4; offset: 03-00h. Default: 7414 1022h. Read only.

31:16	15:0
DID	VID

VID. Vendor ID.
DID. USB controller device ID.

C4A04: USB Controller Status And Command Register
Configuration space; function 4; offset: 07-04h. Default: 0280 0000h.

31:16	15:0
STATUS[15:0]	COMMAND[15:0]

COMMAND[0] IO Space Enable, IOEN. Read-write. 1=Enables access to the IO space for the keyboard/mouse controller ports use in legacy emulation.
COMMAND[1] Memory Space Enable. Read-write. 1=Enables access to the memory space for the host controller registers.
COMMAND[2] Bus Master Enable. Read-write. 1=Enables USB bus master capability.
COMMAND[4] Memory Write and Invalidate Enable. Read-write. 1=Enables bus master to issue memory write and invalidate cycles.
COMMAND[8] SERR# Detection Enable. Read-write. This bit has no effect.
COMMAND[15:9,7:5,3]. Read only. These bits are fixed at their default values.
STATUS[11:0]. Read only. These bits are fixed at their default values.
STATUS[12] Received Target Abort. Read; set by hardware; write 1 to clear. 1=The IC received a target abort while the USB controller was master of the PCI bus.
STATUS[13] Received Master Abort. Read; set by hardware; write 1 to clear. 1=A USB master cycle was terminated with a master abort.
STATUS[15:14]. Read only. These bits are fixed at their default values.

C4A08: USB Revision ID, Programming Interface, Sub Class and Base Registers
Configuration space; function 4; offset: 0B-08h. Default: 0C03 1007h. Read only.

31:8	7:0
CLASSCODE	REVISION ID

REVISION ID. USB controller silicon revision.
CLASSCODE. USB controller class code.

C4A0C: USB Controller BIST, Header, Latency, and Cacheline Size Register
Configuration space; function 4; offset: 0F-0Ch. Default: 0000 0800h.

31:24	23:16	15:8	7:0
BIST	HEADER	LATENCY	CACHELINE SIZE

CACHELINE SIZE. Read-write. 08h=32 Bytes; 00h=0 Bytes. No other values are allowed.
LATENCY, HEADER, BIST. Read only. These are fixed at their default values.

C4A10: USB Controller Base Address Register
Configuration space; function 4; offset: 13-10h. Default: 0000 0000h. Read-write.

31:12	11:0
BASE	Reserved

BASE[31:12] Base Address. These bits specify a 4-KByte non-prefetchable memory space for the USB controller registers.

C4A2C: USB Controller Subsystem ID and Subsystem Vendor ID Register
Configuration space; function 4; offset: 2F-2Ch. Default: 0000_0000h. Read only.

31:16	15:0
SSID	SSVENDORID

SSVENDORID and SSID. Subsystem vendor ID and subsystem ID registers. This register is write accessible through C0A70.

C4A3C: USB Controller Interrupt Line, Interrupt Pin, Min Grant, Max Latency Register
Configuration space; function 4; offset: 3F-3Ch. Default: 5000 0400h.

31:24	23:16	15:8	7:0
MAX LATENCY	MIN GNT	INTERRUPT PIN	INTERRUPT LINE

INTERRUPT LINE. Read-write. This field controls no hardware.
INTERRUPT PIN. Read only. The value 04h indicates that USB interrupts are routed through PIRQD#.
MIN GNT. Read only. These bits are fixed at their default values.
MAX LATENCY. Read only. These bits are fixed at their default values.

C4A44: USB Controller Interrupt Line, Interrupt Pin, Min Grant, Max Latency Register
Configuration space; function 4; offset: 45-44h. Default: 0000h. Read-write.

15:9	8	7:1	0
Reserved	PIPDIS	Reserved	DB16

DB16: Data Buffer Region 16. 1=The size of the region for the data buffer is 16 bytes. 0=The region is 32 bytes.
PIPDIS: SIE Pipelining Disable. 1=Transfer descriptors are disabled from being pipelined with USB bus activity.

5.7 USB Host Controller Memory-Mapped Registers

5.7.1 Summary

For a complete description of these registers, see the OCHI 1.0a specification.

Offset	Register	Offset	Register
00-03h	*HcRevision*	34-37h	*HcFmInterval*
04-07h	*HcControl*	38-3Bh	*HcFrameRemaining*
08-0Bh	*HcCommandStatus*	3C-3Fh	*HcFmNumber*
0C-0Fh	*HcInterruptStatus*	40-43h	*HcPeriodicStart*
10-13h	*HcInterruptEnable*	44-47h	*HcLSThreshold*
14-17h	*HcInterruptDisable*	48-4Bh	*HcRhDescriptorA*
18-1Bh	*HcHCCA*	4C-4Fh	*HcRhDescriptorB*
1C-1Fh	*HcPeriodCurrentED*	50-53h	*HcRhStatus*
20-23h	*HcControlHeadED*	54-57h	*HcRhPortStatus[1]*
24-27h	*HcControlCurrentED*	58-5Bh	*HcRhPortStatus[2]*
28-2Bh	*HcBulkHeadED*	5C-5Fh	*HcRhPortStatus[3]*
2C-2Fh	*HcBulkCurrentED*	60-63h	*HcRhPortStatus[4]*
30-33h	*HcDoneHead*	100h	*HceControl*
		104h	*HceInput*
		108h	*HceOutput*
		10Ch	*HceStatus*

5.7.2 Implementation-Specific Items

- *HcRevision[7:0]* is 10h to indicate that it conforms to OHCI 1.0.
- *HcRevision[8]* is 1 to indicate that legacy keyboard & mouse emulation support is present.
- *HcFmInterval_FSLargestDataPacket* resets to 0.
- *HcRhDescriptorA_NumberDownstreamPorts* is hardwired to 4.
- *HcRhDescriptorA_NoPowerSwitching* resets to 1.
- *HcRhDescriptorA_PowerSwitchingMode* and *HcRhDescriptorA_OverCurrentProtectionMode* must not be set and reset to 0.
- *HcRhDescriptorA_PowerOnToPowerGoodTime* resets to 1 (representing 2 ms), and can only hold the values 0 to 3 (0 to 6 ms).
- *HcRhDescriptorA_NoOverCurrentProtection* resets to 0.
- *HcRhDescriptorB_DeviceRemovable* resets to 0 and should be set by BIOS if non-removable devices are attached.
- *HcRhDescriptorB_PortPowerControlMask* resets to 0 and should not be set.
- Because power switching is not implemented, the set and clear power bits in *HcRhStatus* and *HcRhPortStatus[1-4]* are not supported.
- *HceControl* and *HceStatus* reset to 00h.
- *HceInput* and *HceOutput* are not reset.
- *HcDoneHd[31:4]* should not be modified.
- *HcFmInterval_FSLargestDataPacket* is limited to 14 bits. Bit 15 is read-only 0.
- *HcFmNumber* should not be modified.

5.8 Power Management Configuration Registers (C3Axx)

These registers are in PCI configuration space, function 3. See section 5.1.2 for a description of the register naming convention.

C3A00: System Management Vendor And Device ID
Configuration space; function 3; offset: 03-00h. Default: 7413 1022h. Read only.

31:16	15:0
DID	VID

VID. Vendor ID.
DID. System management device ID.

C3A04: System Management Status And Command Register
Configuration space; function 3; offset: 07-04h. Default: 0280 0000h. Read only.

31:16	15:0
STATUS[15:0]	COMMAND[15:0]

COMMAND[15:0]. These bits are fixed at their default values.
STATUS[15:0]. These bits are fixed at their default values.

C3A08: System Management Revision And Class Code Register
Configuration space; function 3; offset: 0B-08h. Default: 0000 0001h. Read only.

31:8	7:0
CLASSCODE	REVISION

REVISION. System management silicon revision.
CLASSCODE. This register is write accessible through C3A60.

C3A0C: System Management BIST-Header-Latency-Cache Register
Configuration space; function 3; offset: 0F-0Ch. Default: 0000 1600h.

31:24	23:16	15:8	7:0
BIST	HEADER	LATENCY	CACHE

CACHE. Read only. These bits are fixed at their default values.
LATENCY. Read-write. This field controls no hardware.
HEADER. Read only. These bits are fixed at their default values.
BIST. Read only. These bits are fixed at their default values.

C3A2C: System Management Subsystem ID and Subsystem Vendor ID Register
Configuration space; function 3; offset: 2F-2Ch. Default: 0000_0000h. Read only.

31:16	15:0
SSID	SSVENDORID

SSVENDORID and SSID. Subsystem vendor ID and subsystem ID registers. This register is write accessible through C0A70.

C3A40: General Configuration 1 Register
Configuration space; function 3; offset: 40h. Default: 00h. Read-write.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TH2SD

TH2SD. Throttling 2 second delay. 1=There is a 2.0 to 2.5 seconds delay after THERM# is asserted before thermal throttling is initiated as specified by C3A50. 0=Thermal throttling is initiated immediately after THERM# is asserted.

C3A41: General Configuration 2 Register

Configuration space; function 3; offset: 41h. Default: 40h.

7	6	5	4	3	2	1	0
PMIOEN	TMRRST	PCF9EN	PBIN	TMR32	NO_REBOOT	STPGNT	W4SG

W4SG. Wait for stop-grant before deasserting STPCLK#. Read-write. 1=After STPCLK# is asserted for any reason, it is not deasserted until the corresponding stop-grant cycle is received.

STPGNT. PCI stop-grant cycle specification. Read-write. 0=Stop-grant cycles are detected by the IC as PCI special cycles in which the address phase AD[4]=1. 1=Stop-grant cycles are detected by the IC as PCI special cycles in which the data phase AD[31:0]=0012_0002h.

NO_REBOOT. Do not reboot the system when a double TCO timer time out occurs. Read-write. 0=Reboot system with as specified by PORTCF9[FULLRST] when PM46[2NDTO_STS] is set. 1=Do not reboot the system.

TMR32. ACPI timer size selection. Read-write. 0=The ACPI timer, PM08, is 24 bits. 1=The ACPI timer is 32 bits.

PBIN. Power button in. Read only. This bit reflects the current state of the PWRBTN# pin (before the debounce circuit). 0=PWRBTN# is asserted.

PCF9EN. Port CF9 enable. Read-write. 1=Enable access to PORTCF9.

TMRRST. ACPI timer reset. Read-write. 1=The ACPI timer, PM08, is held in the asynchronously cleared state. 0=The timer is enabled to count.

PMIOEN. System management IO space enable. Read-write. 1=PMxx, The IO space specified by C3A58, is enabled.

C3A42: SCI Interrupt Configuration

Configuration space; function 3; offset: 42h. Default: 00h. Read-write.

7	6	5	4	3:0
Reserved	Reserved	TRAPSCI	GPIOSCI	SCISEL

SCISEL. SCI interrupt selection. This field specifies the IRQ number routed to the interrupt controllers used for ACPI-defined SCI interrupts. A value of 0h disables SCI interrupts. Values of 2h, 8h, and Dh are reserved. When C0A4B[SCI2IOA] is high, the value in this register is ignored and SCI does not enter the PIC. All other values are valid. See section 4.3.4.1 for details about SCI interrupt routing.

GPIOSCI. General purpose IO SCI enable. 1=Enable SCI/SMI (based on the state of PM04[SCI_EN]) interrupts when status bits in PMD4 are set while enabled by PMD8. This bit has no affect on whether SMI interrupts are generated via PM2A[GPIOSMI_EN].

TRAPSCI. Trap SCI enable. 1=Enable SCI/SMI (based on the state of PM04[SCI_EN]) interrupts when status bits in PMA8 are set while enabled by PMAC. This bit has no affect on whether SMI interrupts are generated via PM2A[TRPSMI_EN].

C3A43: Power State Register

Configuration space; function 3; offset: 43h.

7	6	5:3	2:0
VDDA_STS	G3TOS5	PWRFL_STS	PPSTATE

PPSTATE. Previous power state. Read only. This field holds the most previous power state from which the system entered the FON state. This field resides on the VDD_AUX power plane. This field is encoded as follows:

PPSTATE	Power state	PPSTATE	Power state
0h	Reserved	4h	MOFF mechanical off
1h	POS power on suspend	5h	STR suspend to RAM
2h	C2	6h	STD suspend to disk
3h	C3	7h	SOFF soft off

PWRFL_STS. Power failure status. Read; updated by hardware; write 1 to LSB to reset to 4h. If power fails (system enters MOFF or PWRGD goes from 1 to 0 while PWRON# is asserted), then this register captures and retains the state the system was in when the failure occurred. This field resides on the VDD_AL plane. This field defaults to 4h when VDD_AL becomes valid. Writing a one to C3A43[3] sets this field to 4h; writing a zero to C3A43[3] or writing any value to any other bits in this field has no effect. This field is encoded as follows:

PWRFL_STS	Power state
0h	FON full on
1h	POS power on suspend
2h	C2
3h	C3

PWRFL_STS	Power state
4h	No AC power failure
5h	STR suspend to RAM
6h	STD suspend to disk
7h	SOFF soft off

G3TOS5. Mechanical off (G3) to soft off (S5). Read-write. 0=When power is a applied to the VDD_AUX plane, the system automatically transitions to the FON state. 1=When power is a applied to the VDD_AUX plane, the system enters the SOFF state. This bit resides on the VDD_AL power plane. When VDD_AL becomes valid, this bit defaults to 0. When there is a PCIRST# generated by a write to PORTCF9[RSTCMD, SYSRST] == 11b, then this is cleared.

VDDA_STS. VDD_AL reset status. Read; set by hardware; write 1 to clear. 1=VDD_AL became invalid. This bit resides on the VDD_AL power plane.

C3A44: PNP IRQ Select Register

Configuration space; function 3; offset: 45-44h. Default: 0000h. Read-write.

Bits[11:0] assign PNPIRQ[2:0] pins to IRQs that are routed to interrupt controllers. See section 4.3.4.1 for more details.

15	14:12	11:8	7:4	3:0
TCO_INT_EN	TCO_INT_SEL	IRQ2SEL	IRQ1SEL	IRQ0SEL

IRQ0SEL. PNPIRQ0 interrupt select. This selects the IRQ number for PNPIRQ0. IRQ0, IRQ2, IRQ8, and IRQ13 are reserved. If PMD2 does not select the PNPIRQ0 function then this field has no effect.

IRQ1SEL. PNPIRQ1 interrupt select. This selects the IRQ number for PNPIRQ1. IRQ0, IRQ2, IRQ8, and IRQ13 are reserved. If PMD3 does not select the PNPIRQ1 function then this field has no effect.

IRQ2SEL. PNPIRQ2 interrupt select. This selects the IRQ number for PNPIRQ2. IRQ0, IRQ2, IRQ8, and IRQ13 are reserved. If PMF4 does not select the PNPIRQ2 function then this field has no effect.

TCO_INT_SEL. TCO interrupt select. Specifies the IRQ line asserted by either PM46[INTRDR_STS] (if PM4A[INTRDR_SEL] selects IRQ) or PM44[TCO_INT_STS]. Note: If PM22[TCOSCI_EN] is set, then this field is has no effect. Note: if one of IRQ[11:9] is selected, then the PIC is required to be programmed as level sensitive for this interrupt. This field is encoded as follows:

TCO_INT_SEL	Interrupt
0	IRQ9
1	IRQ10
2	IRQ11
3	Reserved

TCO_INT_SEL	Interrupt
4	APIC IRQ20
5	APIC IRQ21
6	APIC IRQ22
7	APIC IRQ23

TCO_INT_EN. TCO interrupt enable. 1=Enable TCO IRQ selected by C3A44[TCO_INT_SEL] (if PM22[TCOSCI_EN] = 0).

C3A46: PNP DMA and Chip Select Register

Configuration space; function 3; offset: 47-46h. Default: 0000h. Read-write.

15	14	13	12	11	10:9		8
Reserved	Reserved	Reserved	CS1UBM	CS0UBM	IRQ12_SEL		Reserved
7	6:4			3	2	1	0
Reserved	Reserved			CS1MEM	CS1IO	CS0MEM	CS0IO

CS0IO. PNPCS0# IO space selection. 1=PNPCS0# is asserted during accesses to the IO addresses specified by programmable IO range monitor 3 (C3A46[CS0UBM], C3AC8, and C3ACC) and PCI accesses to this range are claimed by the IC and routed to the ISA bus. If the PNPCS0# function is not selected by PMF6, then this bit has no effect.

CS0MEM. PNPCS0# memory space selection. 1=PNPCS0# is asserted during accesses to the memory addresses specified by programmable memory range monitor 1 (C3AD0 and C3AD8) and PCI accesses to this range are claimed by the IC and routed to the ISA bus. If the PNPCS0# function is not selected by PMF6, then this bit has no effect.
CS1IO. PNPCS1# IO space selection. 1=PNPCS1# is asserted during accesses to the IO addresses specified by programmable IO range monitor 4 (C3A46[CS1UBM], C3AC8, and C3ACC) and PCI accesses to this range are claimed by the IC and routed to the ISA bus. If the PNPCS1# function is not selected by PMF7, then this bit has no effect.
CS1MEM. PNPCS1# memory space selection. 1=PNPCS1# is asserted during accesses to the memory addresses specified by programmable memory range monitor 2 (C3AD4 and C3AD8 and PCI) and PCI accesses to this range are claimed by the IC and routed to the ISA bus. If the PNPCS1# function is not selected by PMF7, then this bit has no effect.
IRQ12_SEL. Pin definition select for IRQ12. This field is encoded as follows:

IRQ12_SEL	Function for IRQ12 pin
00b	IRQ12
01b	No function (pin disabled such that interrupt request 12 to the PIC may be controlled by the mouse interrupt, EKIRQ12, or serial IRQ12)
10b	SMBALERT# input to the system management logic
11b	USBOC1#, USB over current 1, to the USB controller

See section 4.3.4.1 for details about routing interrupts to the PIC.
CS0UBM. PNPCS0# upper bit mask. 1=Bits[10:8] of the IO address are masked from the PNPCS0# decode for IO cycles. 0=Masking for PNPCS0# is only available for the eight LSBs, as specified by C3ACC[MASKIO3].
CS1UBM. PNPCS1# upper bit mask. 1=Bits[10:8] of the IO address are masked from the PNPCS1# decode for IO cycles. 0=Masking for PNPCS1# is only available for the eight LSBs, as specified by C3ACC[MASKIO4].

C3A48: Pins Latched On The Trailing Edge Of Reset Register
Configuration space; function 3; offset: 49-48h. Default: 00??_?000_00?0_?00?b, where ?'s indicate bits that are latched on the trailing edge of reset.

The default for some of these bits is specified by pull up or pull down resistors on pins during the trailing edge of the specified reset (PWRGD). To latch a low from these pins, a 10K to 100K ohm resistor to ground is placed on the signal. To latch a high from these pins, a 10K to 100K ohm resistor to the pin's power plane is placed on the signal.

The resistors enabled by ENIDE, ENPCI, and ENISA are nominally 5K ohms. The default state of these bits are specified by the state of the SPKR pin during reset. A pull-up resistor on SPKR causes these bits to default to high and a pull-down resistor causes these bits to default to low.

15	14	13	12	11	10	9	8
Reserved	Reserved	ENIDE	ENPCI	ENISA	Reserved	Reserved	Reserved
7	6	5	4	3:2		1	0
Reserved	Reserved	MBH	Reserved	MBL		Reserved	ISABIOS

ISABIOS. Direct BIOS accesses to the ISA bus versus the LPC bus. Read only. This reflects the state of the ISABIOS pin. 1=ROM accesses as specified by C0A43 are routed to the ISA bus. 0=ROM accesses as specified by C0A43 are routed to the LPC bus.
MBL. Must be low. Read-write. These bits are required to be low at all times; otherwise undefined behavior will result. The default state of bit[3] is latched off the ROM_KBCS# pin during PWRGD reset (so a pull-down resistor is required).
MBH. Must be high. Read-write. This bit is required to be high at all times; otherwise undefined behavior will result. The default state of bit[3] is latched off the IOCHRDY pin during PWRGD reset (so a pull-up resistor is required).
ENISA. Enable ISA pull-up/down resistors. Read-write. 1=The internal pull-up and pull-down resistors for the ISA bus signals are enabled. This includes pull-ups on IOCHRDY, IOCHK#, IRQ[15,14,11:9,7:3], and SD[7:0]. 0=Disable internal ISA bus resisters. The default state of this bit is latched off the SPKR pin during PWRGD reset.

ENPCI. Enable PCI pull-up resistors. Read-write. 1=The internal pull-ups for PCI bus signals are enabled. This includes pull-ups on DEVSEL#, FRAME#, IRDY#, PIRQ[A,B,C,D]#, SERR#, STOP#, TRDY#. 0=Disable internal PCI bus resisters. The default state of this bit is latched off the SPKR pin during PWRGD reset.
ENIDE. Enable IDE pull-down resistors. Read-write. 1=The internal pull-down resistors for the IDE bus signals are enabled. This includes pull-downs on DDRQP, DDRQS. 0=Disable internal IDE bus resisters. The default state of this bit is latched off the SPKR pin during PWRGD reset.

C3A4A: Serial IRQ Control Register
Configuration space; function 3; offset: 4Ah. Default: 10h. Read-write.

7	6	5:2	1:0
Reserved	CONTMD	FRAMES	STARTCLKS

STARTCLKS. Number of clocks in start pulse. This specifies the number of clocks in the start pulse over SERIRQ is during the start frame of a serial IRQ cycle (including the slave cycle if in quiet mode). 00b = 4 clocks; 01b = 6 clocks; 10b = 8 clocks; 11b = reserved.
FRAMES. Number if IRQ frames for a serial IRQ cycle. This specifies the number of 3-clock IRQ frames that the IC generates during a serial IRQ cycle before issuing the stop frame. The number of frames is 17 plus the value of this field. Thus, the number of frames varies from 17 (for a value of 0h) and to 32 (for a value of Fh).
CONTMD. Continuous mode selected versus quiet mode. 1=The serial IRQ logic is in continuous mode. In continuous mode, the start frame is initiated by the IC immediately following each stop frame. 0=The serial IRQ logic is in quiet mode. In quiet mode, start frames are initiated by external slave devices.

C3A4C: PRDY Timer Control Register
Configuration space; function 3; offset: 4Ch. Default: 00h. Read-write.

Each of these bits control the ability of the PRDY input signal to disable internal counters. When PRDY is active the counters that correspond to the bits in this register that are high stop counting. If the PRDY function of the PRDY pin is not selected by PMCD, then this register has no effect.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ACPI_DIS	SIT_DIS	RW	RTC_DIS	PIT_DIS

PIT_DIS. Programmable interval timer disable. 1=The three timers of the internal legacy PIT stop counting when PRDY is active.
RTC_DIS. Real time clock disable. 1=The real-time clock's counters that are clocked off of the 32 kHz clock stop counting while PRDY is active.
RW. Read-write. This bit is read-write accessible through software; is controls no hardware.
SIT_DIS. System inactivity timer disable. 1=The system inactivity timer specified by PM98 stops counting from counting while PRDY is active.
ACPI_DIS. ACPI power management timer disable. 1=The ACPI timer specified by PM08 stops counting while PRDY is active.

C3A4E: Square Wave Generation Register
Configuration space; function 3; offset: 4Eh. Default: 00h. Read-write.

7	6	5	4	3:0
Reserved	Reserved	Reserved	Reserved	SQWAVE

SQWAVE. Square wave frequency control. When PMD0 selects square wave output function, then this field to specifies the frequency of square wave output on the INTIRQ8# pin. The square wave output is generated by dividing down the 32 kHz clock. This field is encoded as follows:

SQWAVE	Frequency	SQWAVE	Frequency	SQWAVE	Frequency	SQWAVE	Frequency
0h	Output low	4h	4096 Hz.	8h	256 Hz.	Ch	16 Hz.
1h	256 Hz.	5h	2048 Hz.	9h	128 Hz.	Dh	8 Hz.
2h	128 Hz.	6h	1024 Hz.	Ah	64 Hz.	Eh	4 Hz.
3h	8192 Hz.	7h	512 Hz.	Bh	32 Hz.	Fh	2 Hz.

C3A50: Power State Pin Control Register
Configuration space; function 3; offset: 53-50h. Default: 1800_0000h. Read-write.

The bits[23:0] of this register specify the output pins controlled during C2, C3, and POS transitions. Each byte provides the enables for each low-power states. C2 is specified by bits[7:0], C3 is specified by bits [15:8], and POS is specified by bits[23:16]. See section 4.6.1.5 for timing details.

Note: The reserved bits in this register are read-write accessible, however they control no hardware.

31	30	29	28	27:25			24
APIC_POSEN	Reserved	TTHLOCK	TTH_EN	TTH_RATIO			PITRSM#
23	22	21	20	19	18	17	16
CRST_POSEN	SUSP_POSEN	CSLP_POSEN	PSTP_POSEN	CSTP_POSEN	POSEN	DCST_POSEN	ZZ_POSEN
15	14	13	12	11	10	9	8
CRST_C3EN	SUSP_C3EN	CSLP_C3EN	PSTP_C3EN	CSTP_C3EN	C3EN	DCST_C3EN	ZZ_C3EN
7	6	5	4	3	2	1	0
CRST_C2EN	SUSP_C2EN	CSLP_C2EN	PSTP_C2EN	CSTP_C2EN	C2EN	DCST_C2EN	ZZ_C2EN

ZZ_[POS,C3,C2]EN. Enable CACHE_ZZ assertion to the L2 cache during power management. 1=Enable control of the CACHE_ZZ pin during the specified C2, C3, and POS states. 0=CACHE_ZZ is not asserted. This bit has no effect if the PMC8 does not select the CACHE_ZZ function.
DCST_[POS,C3,C2]EN. Enable DCSTOP# assertion to the DRAM controller during power management. 1=Enable control of the DCSTOP# pin during the specified C2, C3, and POS states. 0=DCSTOP# is not asserted.
[POS,C3,C2]EN. Enable STPCLK# during power management. 1=Enable control of the STPCLK# pin during the specified C2, C3, and POS states. 0=STPCLK# is not asserted during C2, C3, and POS. This bit required to be set for any of the other bits in this register's byte to function (i.e., if STPCLK# is not asserted for a given power state, then no other power management control signals are asserted for that power state).
CSTP_[POS,C3,C2]EN. Enable CPUSTOP# assertion to the external PLL during power management. 1=Enable control of the CPUSTOP# pin during the specified C2, C3, and POS states. 0=CPUSTOP# is not asserted. This bit has no effect if the PMC6 does not select the CPUSTOP# function.
PSTP_[POS,C3,C2]EN. Enable PCISTOP# assertion to the external PLL during power management. 1=Enable control of the PCISTOP# pin during the specified C2, C3, and POS states. 0=PCISTOP# is not asserted. This bit has no effect if the PMC7 does not select the PCISTOP# function.
CSLP_[POS,C3,C2]EN. Enable CPUSLEEP# assertion to the processor during power management. 1=Enable control of the CPUSLEEP# pin during the specified C2, C3, and POS states. 0=CPUSLEEP# is not asserted. This bit has no effect if the PMC5 does not select the CPUSLEEP# function.
SUSP_[POS,C3,C2]EN. Enable SUSPEND# assertion during power management. 1=Enable control of the SUSPEND# pin during the specified C2, C3, and POS states. 0=SUSPEND# is always high. This bit has no effect if the PMC4 does not select the SUSPEND# function.
CRST_[POS,C3,C2]EN. Enable assertion of CPURST# during transition to FON. 1=Enables assertion of the CPURST# pin during the transition to FON from the specified C2, C3, and POS states. 0=CPURST# is not asserted during the specified transition. This bit should not be set unless the corresponding SUSP_[POS,C3,C2]EN bit is set (i.e., processor resets are only allowed if SUSPEND# gets asserted).
PITRSM#. Enable the PIT to generate interrupts during POS. 1=Legacy PIT does not generate IRQ0 while in POS, starting from the time that the command to enter POS is sent to PM04. This is necessary to prevent timer-tick interrupts from resuming the system while in POS. 0=PIT generates IRQ0 while in POS.

TTH_RATIO. Thermal throttling duty cycle. These specify the duty cycle of the STPCLK# signal to the processor when the system is in thermal throttling mode (initiated by the THERM# pin when enabled by TTH_EN). The field is encoded as follows:

RATIO bits	Description
000b	Reserved.
001b	87.5% STPCLK# active.
010b	75.0% STPCLK# active.
011b	62.5% STPCLK# active.

RATIO bits	Description
100b	50.0% STPCLK# active.
101b	37.5% STPCLK# active.
110b	25.0% STPCLK# active.
111b	12.5% STPCLK# active.

TTH_EN. Thermal throttling enable. 1=When THERM# is asserted, thermal throttling (duty cycle specified by TTH_RATIO) is enabled. Thermal throttling has priority over normal throttling (see PM10); however, it is disabled if the system is in C2, C3, POS, STR, STD, or SOFF. 0=Thermal throttling disabled.

TTHLOCK. Thermal throttling lock. Write 1 only. 1=Writes to TTH_EN and TTH_RATIO are disabled. Once set, this bit cannot be cleared by software. It is cleared by PCIRST#. Note: TTH_EN and TTH_RATIO are allowed to change during the write command that sets TTHLOCK high.

APIC_POSEN. APIC interrupt message bus PICCLK enable during POS state. 1=PICCLK continues operation during the POS state. 0=PICCLK is driven low after the stop-grant cycle while going into the POS suspend state.

C3A54: PCI IRQ Edge-Or-Level Select Register

Configuration space; function 3; offset: 54h. Default: 00h. Read-write.

7:4	3	2	1	0
Reserved	EDGEPID	EDGEPIC	EDGEPIB	EDGEPIA

EDGEPI[D,C,B,A]. Edge triggered interrupt selects for PCI interrupts. Each of these controls the corresponding PCI interrupt pin, PIRQ[D,C,B,A]#, polarity in the interrupt routing logic (see section 4.3.4.1 for details). 0=The PIRQ[D,C,B,A]# signals are assumed to be active low and level triggered. 1=The signals are assumed to be active low and edge triggered such that the falling edge of the external signals results in rising edges to the PIC. Note: When these bits are high, the corresponding serial IRQ PCI interrupts are disabled.

C3A56: PCI IRQ Routing Register

Configuration space; function 3; offset: 57-56h. Default: 0000h. Read-write.

15:12	11:8	7:4	3:0
PIRQD# Select	PIRQC# Select	PIRQB# Select	PIRQA# Select

PIRQ[D,C,B,A]# Selects. These map the PCI IRQ pins to the internal ISA-bus-compatible interrupt controller (see section 4.3.4.1 for details). The fields are encoded as follows:

PIRQ[D,C,B,A]# Selects	Selected IRQ
0h	None
1h	IRQ1
2h	Reserved
3h	IRQ3
4h	IRQ4
5h	IRQ5
6h	IRQ6
7h	IRQ7

PIRQ[D,C,B,A]# Selects	Selected IRQ
8h	Reserved
9h	IRQ9
Ah	IRQ10
Bh	IRQ11
Ch	IRQ12
Dh	Reserved
Eh	IRQ14
Fh	IRQ15

C3A58: System Management IO Space Pointer

Configuration space; function 3; offset: 5B-58h. Default: 0000_DD01h.

31:16	15:8	7:0
Reserved	PMBASE	PMBLSB

PMBASE. Read-write. Specifies PCI address bits[15:8] of the 256-byte block of IO-mapped registers used for system management (address space PMxx). Access to this address space is enabled by C3A41[PMIOEN].

PMBLSB. Read only. These bits are fixed in their default state.

C3A60: System Management Class Code Write Register
Configuration space; function 3; offset: 63-60h. Default: 0000_0000h. Read-write.

31:8	7:0
CCWRITE	Reserved

CCWRITE. The value placed in this register is visible in C3A08[CLASSCODE].

C3AA0: Serial Port Trap Address Register
Configuration space; function 3; offset: A3-A0h. Default: 02F8_03F8h. Read-write.

C3AA0 along with C3AA4 specify the address for COMA and COMB trap events. These events may be used to generate an SMIs or SCIs or reload the system inactivity timer. The COMA and COMB trap events occur when the following equations are true:
COMA trap event: `AD[15:0] | MASKCA == ADDRCA | MASKCA;`
COMB trap event: `AD[15:0] | MASKCB == ADDRCB | MASKCB;`
Where AD is the address phase of a PCI bus IO cycle. It is not necessary for the cycle to be targeted at the IC. The mask bits cover of bits[7:0] .

31:16	15:0
ADDRCB	ADDRCA

ADDRCA and ADDRCB. Address for the COMA and COMB trap events.

C3AA4: Serial Port Trap Mask Register
Configuration space; function 3; offset: A5-A4h. Default: 0F0Fh. Read-write.

15:8	7:0
MASKCB	MASKCA

MASKCA and MASKCB. Address mask for the COMA and COMB trap events. See C3AA0 for details.

C3AA8: Audio Port 1 and 2 Trap Address Register
Configuration space; function 3; offset: AB-A8h. Default: 0330_0220h. Read-write.

C3AA8, C3AAC, and C3AB0 combine to specify the audio trap event. This event may be used to generate an SMIs or SCIs or reload the system inactivity timer. The audio trap event occurs when the following equation is true:
Audio trap event:

```
      (AD[15:0] | MASKAUD1 == ADDRAUD1 | MASKAUD1) & (PCI IO space access)
    | (AD[15:0] | MASKAUD2 == ADDRAUD2 | MASKAUD2) & (PCI IO space access)
    | (AD[15:0] | MASKAUD3 == ADDRAUD3 | MASKAUD3) & (PCI IO space access)
    | (AD[15:0] | MASKAUD4 == ADDRAUD4 | MASKAUD4) & (PCI IO space access);
```

Where AD is the address phase of a PCI bus IO cycle. It is not necessary for the cycle to be targeted at the IC. The mask bits cover bits[7:0] .

31:16	15:0
ADDRAUD2	ADDRAUD1

ADDRAUD1 and ADDRAUD2. Address for the audio trap events 1 and 2.

C3AAC: Audio Port 3 and 4 Trap Address Register
Configuration space; function 3; offset: AF-ACh. Default: 0388_0530h. Read-write.

31:16	15:0
ADDRAUD4	ADDRAUD3

ADDRAUD3 and ADDRAUD4. Address for the audio trap events 3 and 4. See C3AA8 for details.

C3AB0: Audio Port Trap Mask Register
Configuration space; function 3; offset: B3-B0h. Default: 0707_010Fh. Read-write.

31:24	23:16	15:8	7:0
MASKAUD4	MASKAUD3	MASKAUD2	MASKAUD1

MASKAUD[4:1]. Address masks for the audio trap event. See C3AA8 for details.

C3AB4: PCMCIA Trap 1 and 2 IO Address Register
Configuration space; function 3; offset: B7-B4h. Default: 0000_0000h. Read-write.

C3AB4, C3AB8, C3ABC, and C3AC0 combine to specify the address for the PCMCIA1 and PCMCIA2 trap events. These events may be used to generate an SMIs or SCIs or reload the system inactivity timer. The PCMCIA1 and PCMCIA2 trap events occur when the following is true:
PCMCIA1:

```
  ((AD[15:0] | MASKPIO1 == ADDRPIO1 | MASKPIO1) & (PCI IO space access) )
| ((AD[31:10]| MASKPME1 == ADDRPME1 | MASKPME1) & (PCI memory space access) );
```

PCMCIA2:

```
  ((AD[15:0] | MASKPIO2 == ADDRPIO2 | MASKPIO2) & (PCI IO space access) )
| ((AD[31:10]| MASKPME2 == ADDRPME2 | MASKPME2) & (PCI memory space access) );
```

Where AD is the address phase of a PCI bus cycle. It is not necessary for the cycle to be targeted at the IC. The IO space mask bits cover bits[7:0]. The memory space mask bits cover bits[17:10].

31:16	15:0
ADDRPIO2	ADDRPIO1

ADDRPIO1 and ADDRPIO2. IO address for the PCMCIA1 and PCMCIA2 trap events.

C3AB8: PCMCIA Trap 1 Memory Address Registers
Configuration space; function 3; offset: BB-B8h. Default: 0000_0000h. Read-write.

31:10	9:0
ADDRPME1	Reserved

ADDRPME1. Memory address for the PCMCIA1 trap event. See C3AB4 for details.

C3ABC: PCMCIA Trap 2 Memory Address Registers
Configuration space; function 3; offset: BF-BCh. Default: 0000_0000h. Read-write.

31:10	9:0
ADDRPME2	Reserved

ADDRPME2. Memory address for the PCMCIA2 trap event. See C3AB4 for details.

C3AC0: PCMCIA Trap Mask Registers
Configuration space; function 3; offset: C3-C0h. Default: 0000_0000h. Read-write.

31:24	23:16	15:8	7:0
MASKPME2	MASKPME1	MASKPIO2	MASKPIO1

MASKPME[1,2] and MASKPIO[1,2]. Address mask for the PCMCIA trap events. See C3AB4 for details.

C3AC4: Programmable IO Range Monitor 1 and 2 Trap Address Register
Configuration space; function 3; offset: C7-C4h. Default: 0000_0000h. Read-write.

C3AC4, C3AC8, and C3ACC combine to define the programmable IO range monitor trap events (PIORM[4:1]). These events may be used to generate an SMIs or SCIs or reload the system inactivity timer. The trap events occurs following equations are true:

```
PIORM1:  (AD[15:0] | MASKIO1 == ADDRIO1 | MASKIO1) & (PCI IO space access);
PIORM2:  (AD[15:0] | MASKIO2 == ADDRIO2 | MASKIO2) & (PCI IO space access);
PIORM3:  (AD[15:0] | MASKIO3 == ADDRIO3 | MASKIO3) & (PCI IO space access);
PIORM4:  (AD[15:0] | MASKIO4 == ADDRIO4 | MASKIO4) & (PCI IO space access);
```

Where AD is the address phase of a PCI bus IO cycle. It is not necessary for the cycle to be targeted at the IC. The mask bits cover bits[7:0]. See C3A46[CS1UMB,CS0UMB] for a description of how the mask bits for programmable IO range monitors 3 and 4 can be extended to bits[10:8].

31:16	15:0
ADDRIO2	ADDRIO1

ADDRIO1 and ADDRIO2. Address for the PIORM[1,2] trap events.

C3AC8: Programmable IO Range Monitor 3 and 4 Trap Address Register
Configuration space; function 3; offset: CB-C8h. Default: 0000_0000h. Read-write.

31:16	15:0
ADDRIO4	ADDRIO3

ADDRIO3 and ADDRIO4. Address for the PIORM[3,4] trap events. See C3AC4 for details.

C3ACC: Programmable IO Range Monitor Trap Mask Register
Configuration space; function 3; offset: CF-CCh. Default: 0000_0000h. Read-write.

31:24	23:16	15:8	7:0
MASKIO4	MASKIO3	MASKIO2	MASKIO1

MASKIO[4:1]. Address masks for the PIORM[4:1] trap events. See C3AC4 for details.

C3AD0: Programmable Memory Range Monitor 1 Trap Address Register
Configuration space; function 3; offset: D3-D0h. Default: 0000_0000h. Read-write.

C3AD0, C3AD4, and C3AD8 combine to define the address for the programmable memory range monitor 1 and 2 trap events (PMEMRM[1,2]). These events may be used to generate an SMIs or SCIs or reload the system inactivity timer. These trap events occur when the following equations are true:

```
PMEMRM1: (AD[31:8] | MASKMEM1) == (ADDRMEM1 | MASKMEM1);
PMEMRM2: (AD[31:8] | MASKMEM2) == (ADDRMEM2 | MASKMEM2);
```

Where AD is the address phase of a PCI bus memory cycle. It is not necessary for the cycle to be targeted at the IC. The mask bits cover bits[23:8].

31:8	7:0
ADDRMEM1	Reserved

ADDRMEM1. Memory address for the PMEMRM1 trap event.

C3AD4: Programmable Memory Range Monitor 2 Trap Address Register
Configuration space; function 3; offset: D7-D4h. Default: 0000_0000h. Read-write.

31:8	7:0
ADDRMEM2	Reserved

ADDRMEM2. Memory address for the PMEMRM2 trap event. See C3AD0 for details.

C3AD8: Programmable Memory Range Monitor Trap Mask Registers
Configuration space; function 3; offset: DB-D8h. Default: 0000_0000h. Read-write.

31:16	15:0
MASKMEM2	MASKMEM1

MASKMEM[1,2]. Address mask for the PMEMRM[1,2] trap events. See C3AD0 for details.

5.9 System Management IO Mapped Registers (PMxx)

These registers are in IO space. The base address register for these registers is C3A58. See section 5.1.2 for a description of the register naming convention.

PM00: Power Management 1 Status Register
IO mapped (base pointer: C3A58); offset: 01-00h. Default: 0000h. Read; set by hardware; write 1 to clear.

Most of these bits have the ability to generate an SCI/SMI interrupt, if they are enabled to do so in PM02.

15	14:12	11	10	9	8
WAK_STS	Reserved	PBOR_STS	RTC_STS	SLPBTN_STS	PWRBTN_STS

7:6	5	4	3:1	0
Reserved	GBL_STS	BM_STS	Reserved	TMR_STS

TMR_STS. ACPI timer status. 1=The MSB of the ACPI timer (either bit 23 or 31 based on C3A41[3]), PM08, toggled (from 0 to 1 or 1 to 0).
BM_STS. Bus master status. 1=One of the PCI REQ# signals (brought in on IRQ[11:9, 7:3]) or BMREQ# or any internal PCI master requests signals was asserted.
GBL_STS. Global status. 1=PM2C[BIOS_RLS] was set high.
PWRBTN_STS. Power button status. 1=PWRBTN# has been asserted. The debounce circuitry causes a 12-to-16 millisecond delay from the time the input signal stabilizes until this bit changes. If PM26[PBOR_DIS] is low and PWRBTN# is held low for more than four seconds, then this bit is cleared and PBOR_STS is set. This bit resides on the VDD_AUX power plane. Note: The debounce circuit functions in the high-to-low and low-to-high directions.
SLPBTN_STS. Sleep button status. 1=SLPBTN# has been asserted. The debounce circuitry causes a 12-to-16 millisecond delay from the time the input signal stabilizes until this bit changes. If the GPIO debounce circuitry specified by PMC3 is enabled, then the debounce period is twice as long before setting the status bit. If the SLPBTN# function is not selected by PMC3, then this bit cannot be set. If PM26[SBOR_DIS] is low and SLPBTN# is held low for more than four seconds, then this bit is cleared and PBOR_STS is set. This bit resides on the VDD_AUX power plane. Note: The debounce circuit functions in the high-to-low and low-to-high directions.
RTC_STS. Real time clock status. 1=The real-time clock generated an interrupt. This bit resides on the VDD_AUX power plane.
PBOR_STS. Power button override status. 1=A power button override event occurred. A power button override event occurs if (1) PM26[PBOR_DIS] is low and PWRBTN# is held in the active state for more than four seconds or (2) if PM26[SBOR_DIS] is low, the SLPBTN# function is enabled by PMC3, and SLPBTN# is held in the active state for more than four seconds. This bit resides on the VDD_AUX power plane.
WAK_STS. Wakeup status. 1=The system was in a sleep state (S1 to S5) and an enabled resume event occurred. Upon setting this bit, the system resumes.

PM02: Power Management 1 Enable Register
IO mapped (base pointer: C3A58); offset: 03-02h. Default: 0000h. Read-write.

These bits work in conjunction with the corresponding bits in PM00 to generate SCI or SMI interrupts.

15:11	10	9	8
Reserved	RTC_EN	SLPBTN_EN	PWRBTN_EN

7:6	5	4:1	0
Reserved	GBL_EN	Reserved	TMR_EN

TMR_EN. ACPI timer SCI enable. 1=Enable an SCI interrupt when PM00[TMR_STS] is set high. Note: This results in an SCI interrupt, regardless as to the state of PM04[SCI_EN].
GBL_EN. Global SCI enable. 1=Enable an SCI interrupt when PM00[GBL_STS] is set high. Note: This results in an SCI interrupt, regardless as to the state of PM04[SCI_EN].
PWRBTN_EN. Power button SCI/SMI enable. 1=Enable either an SCI or an SMI interrupt (based on the state of PM04[SCI_EN]) when PM00[PWRBTN_STS] is set high.
SLPBTN_EN. Sleep button SCI/SMI enable. 1=Enable either an SCI or an SMI interrupt (based on the state of PM04[SCI_EN]) when PM00[SLPBTN_STS] is set high.
RTC_EN. Real time clock alarm SCI/SMI enable. 1=Enable either an SCI or an SMI interrupt (based on the state of PM04[SCI_EN]) when PM00[RTC_STS] is set high.

PM04: Power Management 1 Control Register
IO mapped (base pointer: C3A58); offset: 05-04h. Default: 0000h.

15:14	13	12:10	9:3	2	1	0
Reserved	SLP_EN	SLP_TYP	Reserved	GBL_RLS	BM_RLD	SCI_EN

SCI_EN. SCI-SMI select. Read-write. Selects the type of interrupt generated by power management events.
0 SMI interrupt.
1 SCI interrupt.
Certain power management events may be programmed individually to generate SMI interrupts independent of the state of this bit. Also, TMR_STS and GBL_STS always generate SCI interrupts regardless as to the state of this bit. See section 4.6.1.1 for details.
BM_RLD. Bus master reload. Read-write. 1=Enables PM00[BM_STS] to resume from C3.
GBL_RLS. Global release. Read; write 1 to set; cleared by hardware. When this bit is set high, the hardware sets PM28[BIOS_STS] high. GBL_RLS is cleared by the hardware when PM28[BIOS_STS] is cleared by software.
SLP_TYP. Sleep type. Read-write. Specifies the type of sleep state the system enters when SLP_EN is set high.
0 FON, S0. Full on.
1 POS, S1. Power on suspend.
2-4 Reserved.
5 STR, S3. Suspend to RAM.
6 STD, S4. Suspend to disk.
7 SOFF, S5. Soft off.
SLP_EN. Sleep enable. Write 1 only; reads back as 0. Writing a 1 to this bit causes the system to sequence into the sleep state specified by SLP_TYP.

PM08: ACPI Power Management Timer
IO mapped (base pointer: C3A58); offset: 0B-08h. Default: 0000 0000h. Read only.

This is either a 24- or a 32-bit counter, based on the state of C3A41[3]. It is a free-running, incrementing counter clocked off of a 3.579545 MHz clock. It does not count when in the system is in MOFF, SOFF, STD, or STR state. When the MSB toggles (either bit[23] or bit[31]) then PM00[TMR_STS] is set. This timer is asynchronously cleared when C3A41[TMRRST] is high.

31:24	23:0
ETM_VAL	TMR_VAL

TMR_VAL. Timer value. This provides the current count of the ACPI power management timer.
ETM_VAL. Extended timer value. If C3A41[3] is high, then these are the 8 MSBs of the ACPI power management timer. If C3A41[3] is low, then this field always reads back as all zeros.

PM10: Processor Clock Control Register
IO mapped (base pointer: C3A58); offset: 13-10h. Default: 0000 0000h. Read-write.

31:5	4	3:1	0
Reserved	NTH_EN	NTH_RATIO	Reserved

NTH_RATIO. Normal throttling duty cycle. These specify the duty cycle of the STPCLK# signal to the processor when the system is in normal throttling mode, enabled by NTH_EN. The field is encoded as follows:

RATIO bits	Description	RATIO bits	Description
000b	Reserved.	100b	50.0% STPCLK# active.
001b	87.5% STPCLK# active.	101b	37.5% STPCLK# active.
010b	75.0% STPCLK# active.	110b	25.0% STPCLK# active.
011b	62.5% STPCLK# active.	111b	12.5% STPCLK# active.

NTH_EN. Normal throttling enable. 1=Normal throttling (duty cycle specified by NTH_RATIO) is enabled. Normal throttling is lower priority than thermal throttling (as specified by C3A50); when thermal throttling is enabled, the throttling duty cycle is specified by C3A50. Throttling is disabled when in the C2, C3, POS, STR, STD, or SOFF states. 0=Normal throttling is not enabled.

PM14: Processor Level 2 Register
IO mapped (base pointer: C3A58); offset: 14h. Default: 00h. Read only.

7:0
P_LVL2

P_LVL2. Reads from this register initiate the transition of the processor to the C2 state, as specified by C3A50. This register is byte readable only. Reads from this register always return 00h.

PM15: Processor Level 3 Register
IO mapped (base pointer: C3A58); offset: 15h. Default: 00h. Read only.

7:0
P_LVL3

P_LVL3. Reads from this register initiate the transition of the processor to the C3 state, as specified by C3A50. This register is byte readable only. Reads from this register always return 00h.

PM16: Resume Event Enable Register
IO mapped (base pointer: C3A58); offset: 17-16h. Default: 0000h. Read-write.

For these bits, 1=Enable the specified event to resume the system out C2, C3, or POS.

15	14	13	12	11	10	9	8
Reserved	RI_RSM	Reserved	Reserved	Reserved	SIT_RSM	RTC_RSM	IRQ_RSM
7	6	5	4	3	2	1	0
USB_RSM	SLPB_RSM	SMBA_RSM	HSLV_RSM	SNP_RSM	EXT_RSM	PME_RSM	PB_RSM

PB_RSM. Resume on PM00[PWRBTN_STS]=1.
PME_RSM. Resume on PM20[PME_STS]=1.
EXT_RSM. Resume on PM20[EXTSMI_STS]=1.
SNP_RSM. Resume PME0[SNP_STS]=1.
HSLV_RSM. Resume on PME0[HSLV_STS]=1.
SMBA_RSM. Resume on PME0[SMBA_STS]=1.
SLPB_RSM. Resume on PM00[SLPBTN_STS]=1.
USB_RSM. Resume on PM20[USB_RSM_STS]=1.
IRQ_RSM. Resume on assertion of an unmasked IRQ (when INTR to the processor is set). Note: IRQ0, the timer tick interrupt, may be masked from generating these resume events via C3A50[PITRSM#].
RTC_RSM. Resume on PM00[RTC_STS]=1.
SIT_RSM. Resume on PM20[SIT_STS]=1.
RI_RSM. Resume on PM20[RI_STS]=1.

PM18: Flag Write Register
IO mapped (base pointer: C3A58); offset: 19-18h. Default: 0000h. Read-write.

15:0
FWRDATA

FWRDATA. Flag write data. Writes to this register are routed to the ISA bus with the FLAGWR pin asserted. The SA and SD ISA bus pins are guaranteed to be valid at least 30 nanoseconds before and 20 nanoseconds after FLAGWR is asserted. Reads provide the last data written to this register (internally latched). PM18 and PM1A should not be read in a single cycle; the two registers are required to be read separately. To use the FLAGWR pin, PMCA is required to be configured as the FLAGWR function.

PM1A: Flag Read Register
IO mapped (base pointer: C3A58); offset: 1B-1Ah. Default: 0000h. Read only.

15:0
FRDDATA

FRDDATA. Flag read data. Reads from this register are routed to the ISA bus with the FLAGRD# pin asserted. FLAGRD# is asserted with the same timing as IOR# for these cycles. PM18 and PM1A should not be read in a single cycle; the two registers are required to be read separately. To use the FLAGRD# pin, PMCB is required to be configured as the FLAGRD# function.

PM1E (PM2F): Software SMI Trigger Register
IO mapped (base pointer: C3A58); offset: 1Eh. Default: 00h. Read-write. This address accesses the same physical register located at PM2F (i.e., both accesses to PM1E and PM2F identically access the same register and both may be used to set PM28[SWI_STS]).

PM20: ACPI GP Status Register
IO mapped (base pointer: C3A58); offset: 21-20h. Default: 0000h. Read; set by hardware; write 1 to clear.

Access to some of these bits is replicated in PM24 and PM28. For these bits, there is only one physical register. These bits have the ability to generate an SCI/SMI interrupt, if they are enabled to do so in PM22.

15	14	13	12	11	10	9	8
USB_RSM_STS	RI_STS	Reserved	Reserved	Reserved	THERM_STS	EXTSMI_STS	PME_STS
7	6	5	4	3	2	1	0
TCOSCI_STS	Reserved	SIT_STS	Reserved	Reserved	Reserved	Reserved	Reserved

SIT_STS. System inactivity timer time out status. 1=The system inactivity timer, PM98, timed out. Access to this register is replicated in PM28.
TCOSCI_STS. TCO SCI interrupt status. 1=There was a 0 to 1 transition on PM46[INTRDR_STS] or PM44[TCO_INT_STS].
PME_STS. PME# pin status. 1=The PME# pin was asserted. This bit resides on the VDD_AUX power plane. Access to this register is replicated in PM28.
EXTSMI_STS. External SMI pin status. 1=The EXTSMI# pin was asserted (the active state is dependent upon the GPIO12 input polarity). This bit resides on the VDD_AUX power plane. Access to this register is replicated in PM28.
THERM_STS. THERM# pin status. 1=The THERM# pin was asserted. Access to this register is replicated in PM28.
RI_STS. RI# pin status. 1=The RI# pin is asserted (the active state is dependent upon the GPIO14 input polarity). This bit resides on the VDD_AUX power plane. Access to this register is replicated in PM28.
USB_RSM_STS. USB-defined resume event status. 1=The USB-defined resume event has occurred. This bit resides on the VDD_AUX power plane. Access to this register is replicated in PM24.

PM22: ACPI GP Enable Register
IO mapped (base pointer: C3A58); offset: 23-22h. Default: 0000h. Read-write.

These bits work in conjunction with the corresponding bits in PM20 to generate SCI or SMI interrupts. For each of the bits in this register: 1=Enable a corresponding status bit in PM20 to generate an SMI or SCI interrupt (based on the state of PM04[SCI_EN]); 0=Do not enable the SMI or SCI interrupt.

15	14	13	12	11	10	9	8
USB_RSM_EN	RI_EN	Reserved	Reserved	Reserved	THERM_EN	EXTSMI_EN	PME_EN
7	6	5	4	3	2	1	0
TCOSCI_EN	Reserved	SIT_EN	Reserved	Reserved	Reserved	Reserved	Reserved

SIT_EN. System inactivity timer time out ACPI interrupt enable.
TCOSCI_EN. TCO SCI enable. Note: When this is high, C3A44[TCO_INT_SEL] is ignored.
PME_EN. PME# pin ACPI interrupt enable.
EXTSMI_EN. External SMI pin ACPI interrupt enable.
THERM_EN. THERM# pin ACPI interrupt enable.
RI_EN. RI# pin ACPI interrupt enable.
USB_RSM_EN. USB resume event ACPI interrupt enable. Access to this bit is replicated in PM25; there is only one physical register accessed through both PM22 and PM25.

PM24: LPT-USB Event Status Register
IO mapped (base pointer: C3A58); offset: 24h. Default: 00h. Read; set by hardware; write 1 to clear.

7	6	5	4	3	2	1	0
LPT3_STS	LPT2_STS	LPT1_STS	USB_RSM_STS	USB_BLK_STS	USB_INT_STS	USB_ISO_STS	USB_CTL_STS

USB_CTL_STS. USB control transfer status. 1=A USB control transfer has been completed.
USB_ISO_STS. USB isochronous transfer status. 1=A USB isochronous transfer has been completed.
USB_INT_STS. USB interrupt transfer status. 1=A USB interrupt transfer has completed.
USB_BLK_STS. USB bulk transfer status. 1=A USB bulk transfer has been completed.
USB_RSM_STS. USB-defined resume event status. Access to this bit is replicated in PM20; see that register. This bit resides on the VDD_AUX power plane.
LPT1_STS. IO access to 378-37Fh status. 1=An access to IO space between 378h and 37Fh has occurred.
LPT2_STS. IO access to 278-27Fh status. 1=An access to IO space between 278h and 27Fh has occurred.
LPT3_STS. IO access to 3BC-3BFh status. 1=An access to IO space between 3BCh and 3BFh has occurred.

PM25: LPT-USB Event Interrupt Enable Register
IO mapped (base pointer: C3A58); offset: 25h. Default: 0000h. Read-write.

For each of the bits in this register: 1=Enable a corresponding status bit in PM24 to generate an SMI or SCI interrupt (based on the state of PM04[SCI_EN]); 0=Do not enable the SMI or SCI interrupt.

7	6	5	4	3	2	1	0
LPT3_EN	LPT2_EN	LPT1_EN	USB_RSM_EN	USB_BLK_EN	USB_INT_EN	USB_ISO_EN	USB_CTL_EN

USB_CTL_EN. USB control transfer interrupt enable.
USB_ISO_EN. USB isochronous transfer interrupt enable.
USB_INT_EN. USB interrupt transfer interrupt enable.
USB_BLK_EN. USB bulk transfer interrupt enable.
USB_RSM_EN. USB-defined resume event interrupt enable. Access to this bit is replicated in PM22.
LPT1_STS. IO access to 378-37Fh interrupt enable.
LPT2_STS. IO access to 278-27Fh interrupt enable.
LPT3_STS. IO access to 3BC-3BFh interrupt enable.

PM26: Sleep State Resume Enable Register
IO mapped (base pointer: C3A58); offset: 27-26h. Default: 2200h. Read-write.

The CTL bits in this register enable resume events from STR, STD, and SOFF. This register resides on the VDD_AUX power plane.

15	14	13	12	11	10	9	8
Reserved	RI_CTL	SBOR_DIS	SLPBTN_CTL	PBOR_DIS	PME_CTL	PB_CTL	RTC_PS_CTL
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	HSLV_CTL	SNP_CTL	USBRSM_CTL	EXTSMI_CTL

EXTSMI_CTL. EXTSMI# resume. 1=Enables the assertion of PM20[EXTSMI_STS] to resume the system from STR, STD, and SOFF.
USBRSM_CTL. USB resume. 1=Enables the assertion of PM20[USB_RSM_STS] to resume the system from STR, STD, and SOFF.
SNP_CTL. SMBus snoop address match resume. 1=Enables the assertion of PME0[SNP_STS] to resume the system from STR, STD, and SOFF.
HSLV_CTL. SMBus host-as-slave address match resume. 1=Enables the assertion of PME0[HSLV_STS] to resume the system from STR, STD, and SOFF.
RTC_PS_CTL. Real time clock resume. 1=Enables the assertion of PM00[RTC_STS] to resume the system from STR, STD, and SOFF.
PB_CTL. Power button resume. 1=Enables the assertion of PM00[PWRBTN_STS] to resume the system from STR, STD, and SOFF.
PME_CTL. PME# resume. 1=Enables the assertion of PM20[PME_STS] to resume the system from STR, STD, and SOFF.

PBOR_DIS. Power button override disable. 1=The power button override event is disabled; PM00[PBOR_STS] stays low and the system does not automatically transition to SOFF. 0=The power button override event is enabled.
SLPBTN_CTL. SLPBTN# resume. 1=Enables the assertion of PM00[SLPBTN_STS] to resume the system from STR, STD, and SOFF.
SBOR_DIS. SLPBTN# override disable. 1=The sleep button override event is disabled; PM00[PBOR_STS] stays low and the system does not automatically transition to SOFF. 0=The sleep button override event is enabled.
RI_CTL. RI# resume. 1=Enables the assertion of PM20[RI_STS] to resume the system from STR, STD, and SOFF.

PM28: Global Status Register
IO mapped (base pointer: C3A58); offset: 29-28h. Default: 0000h.

Each of the EVT bits in this register specify enabled status bits in other registers. These are not sticky bits; they reflect the combinatorial equation of: _EVT = (status1 AND enable1) OR (status2 AND enable2)…

15	14	13	12	11	10	9	8
MISC_EVT	RI_STS	Reserved	Reserved	SMBUS_EVT	THERM_STS	EXTSMI_STS	PME_STS
7	6	5	4	3	2	1	0
SWI_STS	BIOS_STS	SIT_STS	LPTUSB_EVT	GPIO_EVT	PM1_EVT	TCO_EVT	TRP_EVT

TRP_EVT. Hardware trap status. Read only. 1=The enabled hardware trap status bits specified by PMA8 are active.
TCO_EVT. TCO SMI interrupt event. Read only. 1=Any of PM44[NMI2SMI_STS, SW_TCO_SMI, TOUT_STS, IBIOS_STS] are set.
PM1_EVT. Power management 1 status. Read only. 1=Any of the enabled power management events specified by PM00 (enabled by PM02) are active.
GPIO_EVT. GPIO interrupt status. Read only. 1=Any of the enabled GPIO pin status bits specified by PMD4 are active.
LPTUSB_EVT. LPT access or USB transfer or resume event status. Read only. 1=Any of the bits in PM24 that are enabled in PM25 are active.
SIT_STS. System inactivity timer time out status. Access to this bit is replicated in PM20; see that register.
BIOS_STS. BIOS status. Read; set by hardware; write 1 to clear. 1=PM04[GBL_RLS] was set high. BIOS_STS is cleared when a 1 is written to it; writing a 1 to BIOS_STS also causes the hardware to clear PM04[GBL_RLS]. This bit may enabled to generate SMI interrupts only (if enabled in PM2A[BIOSSMI_EN]); it cannot be enabled to generate SCI interrupts.
SWI_STS. Software SMI status. Read; set by hardware; write 1 to clear. 1=A write of any value was sent to PM2F or PM1E. This bit may be enabled to generate SMI interrupts only (if enabled in PM2A[SWISMI_EN]); it cannot be enabled to generate SCI interrupts.
PME_STS. PME# pin status. Access to this bit is replicated in PM20; see that register. This bit resides on the VDD_AUX power plane.
EXTSMI_STS. External SMI pin status. Access to this bit is replicated in PM20; see that register. This bit resides on the VDD_AUX power plane.
THERM_STS. THERM# pin status. Access to this bit is replicated in PM20; see that register.
SMBUS_EVT. System management bus status. Read only. 1=An SMBus event occurred including the completion of the current SMBus host access, host-as-slave accesses, slave detect accesses, and assertion of SMBALERT# (PME0 status bits enabled in PME2).
RI_STS. RI# pin status. Access to this bit is replicated in PM20; see that register. This bit resides on the VDD_AUX power plane.
MISC_EVT. Miscellaneous SMI event. Read only. 1=Any of the status bits in PM30 that are enabled in PM32 are active.

PM2A Global SMI Enable Register
IO mapped (base pointer: C3A58); offset: 2B-2Ah. Default: 0000h. Read-write.

Each of the bits in this register enable SMI# interrupts for the specified status register. For each of these bits: 1=Enable the specified event to generate an SMI interrupt, regardless as to the state of PM04[SCI_EN].

15	14	13	12	11	10	9	8
Reserved	RISMI_EN	SLPBTN_EN	PWRBTN_EN	SMBUS_EN	THMSMI_EN	EXTSMI_EN	PMESMI_EN
7	6	5	4	3	2	1	0
SWISMI_EN	BIOSSMI_EN	SITSMI_EN	USBSMI_EN	GPIOSMI_EN	PM1SMI_EN	TCO_EN	TRPSMI_EN

TRPSMI_EN. Hardware trap SMI enable. An SMI is generated if PM28[TRP_EVT] is asserted.
TCO_EN. TCO SMI interrupt enable. An SMI is generated if PM28[TCO_EVT] is asserted. Note: If PM48[NMI2SMI_EN] is set, then PM44[NMI2SMI_STS] generates SMI interrupts regardless of the state of this bit. Even if the TCO_EN bit is 0, NMIs are still routed to generate SMI interrupts.
PM1SMI_EN. Power management 1 SMI enable. An SMI is generated if PM28[PM1_EVT] is asserted.
GPIOSMI_EN. GPIO interrupt SMI enable. An SMI is generated if PM28[GPIO_EVT] is asserted.
USBSMI_EN. USB transfer or resume event enable. An SMI is generated if any of PM24[4:0] is asserted while being enabled by the corresponding bits in PM25[4:0].
SITSMI_EN. System inactivity timer time out SMI enable. An SMI is generated if PM20[SIT_STS] is asserted.
BIOSSMI_EN. BIOS SMI enable. An SMI is generated if PM28[BIOS_STS] is asserted.
SWISMI_EN. Software SMI enable. An SMI is generated if PM28[SWI_STS] is asserted.
PMESMI_EN. PME# pin SMI enable. An SMI is generated if PM20[PME_STS] is asserted.
EXTSMI_EN. External SMI pin SMI enable. An SMI is generated if PM20[EXTSMI_STS] is asserted.
THMSMI_EN. THERM# pin SMI enable. An SMI is generated if PM20[THERM_STS] is asserted.
SBUS_EN. SMBus event enable. An SMI is generated if PM28[SMBUS_EVT] goes high.
PWRBTN_EN. PWRBTN# pin SMI enable. An SMI is generated if PM00[PWRBTN_STS] is asserted.
SLPBTN_EN. SLPBTN# pin SMI enable. An SMI is generated if PM00[SLPBTN_STS] is asserted.
RISMI_EN. RI# pin SMI enable. An SMI is generated when PM20[RI_STS] is asserted.

PM2C: Global SMI Control Register
IO mapped (base pointer: C3A58); offset: 2D-2Ch. Default: 0000h.

15:6	5	4	3	2	1	0
Reserved	SMIACT	SMILK	EOS	Reserved	BIOS_RLS	SMI_EN

SMI_EN. SMI enable control. Read-write. 1=Enable SMI generation. 0=SMI disabled (however, if SMIACT is set and SMI_EN is cleared, then SMI# remains asserted until SMIACT is cleared).
BIOS_RLS. BIOS SCI/SMI lock release. Read; write 1 only; cleared by hardware. 1=The SCI/SMI lock has been released. When this bit is set high, PM00[GBL_STS] is set high by the hardware. BIOS_RLS is cleared by the hardware when PM00[GBL_STS] is cleared by software. Note that if PM02[GBL_EN] is set, then setting this bit generates an SCI interrupt.
EOS. End of SMI. Write 1 only. Writing a 1 to this bit forces the SMI# pin to be deasserted for 4 PCI clocks. This bit always reads as a 0.
SMILK. SMI lock control. Read-write. 1=The SMI# pin is locked into the active state after it is asserted. The latch is controlled by SMIACT. 0=The SMI# pin is not internally latched.
SMIACT. SMI active. Read; set by hardware; write 1 to clear. This bit is set high by the hardware on the asserting edge of SMI#. If SMILK is high, then SMIACT holds the SMI# pin in the active state. If SMILK is low, then SMIACT has no effect on the SMI# pin.

PM2F: Software SMI Trigger Register
IO mapped (base pointer: C3A58); offset: 2Fh. Default: 00h. Read-write.

7:0
SMI_CMD

SMI_CMD. SMI command. Writes to this register set PM28[SWI_STS]. Reads of this register provide the data last written to it. Note: This register is identically accessible from offset 1Eh as well (PM1E).

PM30: Miscellaneous SMI Status Register
IO mapped (base pointer: C3A58); offset: 31-30h. Default: 0000h. Read; set by hardware; write 1 to clear.

Each of these status bits may be enabled to generate SMI interrupts via PM32.

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	64MS_STS	1MIN_STS	SIRQSMI_STS	RWR_STS	SLPCMD_STS

SLPCMD_STS. Sleep command status. 1=A write occurred to PM04 with bit[13], SLP_EN, set high.
RWR_STS. BIOS ROM write enable status. 1=C0A40[RWR] was written from a 0 to a 1.
SIRQSMI_STS. Serial IRQ SMI status. 1=SMI interrupt was initiated from the serial IRQ logic from the SERIRQ pin.
1MIN_STS. One minute status bit. 1=One minute expired. After entering the FON state, this bit is set every 60 +/- 4 seconds.
64MS_STS. 64 millisecond timer status. 1=64 milliseconds expired. After PM32[64MS_EN] is set high, the 64 millisecond timer sets this bit every 64 +/- 4 milliseconds. The timer does not stop after this bit is set.

PM32: Miscellaneous SMI Enable Register
IO mapped (base pointer: C3A58); offset: 33-32h. Default: 0000h.

For each of the bits in this register: 1=enable a corresponding status bit in PM30 to generate an SMI interrupt. 0=Do not enable the SMI interrupt.

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	64MS_EN	1MIN_EN	SIRQSMI_EN	RWR_EN	SLPCMD_EN

SLPCMD_EN. Enable SMI on sleep command. Read-write. Note: When this bit is high and the sleep command is sent to PM04, the system power state is disabled from changing. It is expected that the SMI interrupt service routine clears PM30[SLPCMD_STS], clears this bit, and then re-issues the command in order to change the power state.
RWR_EN. BIOS ROM write enable SMI enable. Read, write to 1 only. Once this bit is set, it may only be cleared by PCIRST#.
SIRQSMI_EN. Serial IRQ SMI enable. Read-write.
1MIN_EN. One minute SMI enable. Read-write.
64MS_EN. 64 millisecond SMI enable. Read-write. 1=Enable PM32[64MS_STS] to generate SMI interrupts and enable the 64 millisecond timer. 0=The 64 millisecond timer is cleared.

PM38: IO Cycle Tracker Register
IO mapped (base pointer: C3A58); offset: 3B-38h. Default: 0000_0000h. Read only.

31:20	19:16	15:0
Reserved	TKRCMD	TKRADDR

TDRADDR. Tracker address. Contains the lower 16 bits of the PCI bus address phase for the last transaction before SMI was asserted. This may be used to determine the IO access that triggered an SMI.
TDRCMD. Tracker command. Contains the PCI bus command for the last transaction before SMI was asserted.

PM40: TCO Timer Reload and Current Value Register
IO mapped (base pointer: C3A58); offset: 40h. Default: 04h. Read; write command.

The TCO timer is a 6-bit down counter that is clocked approximately every 0.6 seconds providing times of up to 38 seconds. If it counts past zero, PM44[TOUT_STS] is set, the timer rolls over to the value in PM41, and the timer continues counting.

7:6	5:0
Reserved	TCORLD

TCORLD. TCO timer. Reads from this register return the current count of the TCO timer. Writes of any value cause the TCO timer to be reloaded with the value in PM41.

PM41: TCO Timer Initial Value Register
IO mapped (base pointer: C3A58); offset: 41h. Default: 04h. Read-write.

7:6	5:0
Reserved	TCOTIME

TCOTIME. TCO timer reload value. Specifies the value loaded into the TCO timer; see PM40.

PM42: TCO SMI Data In Register
IO mapped (base pointer: C3A58); offset: 42h. Default: 00h. Read-write.

7:0
TCOSMI

TCOSMI. TCO SMI data. Writes of any value to this register set PM44[SW_TCO_SMI] and generate an SMI. Reads provide the last value written.

PM43: TCO SMI Data Out Register
IO mapped (base pointer: C3A58); offset: 43h. Default: 00h. Read-write.

7:0
TCOOUT

TCOOUT. TCO output data to OS. Writes of any value to this register set PM44[TCO_INT_STS] and generate an IRQ as specified by C3A44[TCO_INT_SEL] and PM22[TCOSCI_EN]. Reads provide the last value written.

PM44: TCO Status 1 Register
IO mapped (base pointer: C3A58); offset: 45-44h. Default: 0000h. Read; set by hardware; write 1 to clear.

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IBIOS_STS
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	TOUT_STS	TCO_INT_STS	SW_TCO_SMI	NMI2SMI_STS

NMI2SMI_STS. NMI to SMI status. 1=An NMI was detected while PM48[NMI2SMI_EN] was high. This bit is not affected by setting PM48[NMI_NOW]. Assertion of this bit results in an SMI interrupt.
SW_TCO_SMI. Software-generated SMI status. 1=A write to PM42 was detected. This bit may be enabled by PM2A[TCO_EN] to generate SMI interrupts.
TCO_INT_STS. TCO interrupt status. 1=A write to PM43 was detected. Assertion of this bit results in an IRQ as specified by C3A44[TCO_INT_SEL] and PM22[TCOSCI_EN].
TOUT_STS. TCO timer timeout status. 1=The TCO timer, PM40, counted past zero. This bit may be enabled by PM2A[TCO_EN] to generate SMI interrupts.
IBIOS_STS. BIOS illegal access status. 1=An illegal access to BIOS address space has occurred. This occurs when: (1) there is a read to a read-locked address or a write to a write-locked address as specified by C0A40[RWR], C0A80, C0A84, C0A88, and C0A8C[3:0] or (2) C0A40[BLE]=1 and C0A40[RWR] is written from a 0 to a 1. This bit may enabled by PM2A[TCO_EN] to generate SMI interrupts.

PM46: TCO Status 2 Register
IO mapped (base pointer: C3A58); offset: 46h. Default: 00h. Read; set by hardware; write 1 to clear.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	BOOT_STS	2NDTO_STS	INTRDR_STS

INTRDR_STS. Intruder detect status. 1=The INTRUDER# pin was detected asserted for more than 60 microseconds (debounce time). This register resides on the VDD_AL power plane. It functions in all power states unless VDD_AL is not valid. When VDD_AL is powered, this bit defaults low.
2NDTO_STS. Second TCO time out status. 1=The TCO timer, PM40, timed out a second time before PM44[TOUT_STS] was cleared. If enabled by C3A41[NO_REBOOT], assertion of this bit reboots the system. This bit resides on the VDD_AUX power plane.
BOOT_STS. Boot status. 1=The TCO timer has timed out twice without any BIOS ROM accesses. This is detected when PM46[2NDTO_STS] changes from 0 to 1 after any PCIRST# before any BIOS ROM accesses have occurred. This bit resides on the VDD_AUX power plane.

PM48: TCO Control 1 Register

IO mapped (base pointer: C3A58); offset: 49-48h. Default: 0000h. Read-write.

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	TCOHALT	MBL	NMI2SMI_EN	NMI_NOW
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

NMI_NOW. Generate NMI. 1=Assert NMI. It is expected that the NMI interrupt handler clears this bit.

NMI2SMI_EN. NMI interrupts generate SMI interrupts. 1=Whenever an NMI is detected, PM44[NMI2SMI_STS] is set and the NMI pin is not asserted; this bit does not affect NMI_NOW (setting NMI_NOW generates an NMI interrupt regardless of the state of NMI2SMI_EN). Note: If this bit is set and RTC70[NMIDIS] is set, then neither NMI nor SMI# is asserted when NMI events occur.

MBL. Must be low. Read-write. This bit is required to be low at all times; otherwise undefined behavior will result.

TCOHALT. TCO timer halt. 1=Freeze TCO timer in its current state; PM44[TOUT_STS] and PM46[2NDTO_STS] may not be set.

PM4A: TCO Control 2 Register

IO mapped (base pointer: C3A58); offset: 4Ah. Default: 00h. Read-write.

7	6	5	4	3	2:1	0
Reserved	Reserved	Reserved	Reserved	Reserved	INTRDR_SEL	Reserved

INTRDR_SEL. Select action taken if PM46[INTRDR_STS] is set. 00b=Reserved; 01b=IRQ (as specified by C3A44[TCO_INT_SEL]); 10b=SMI; 11b=Reserved.

PM98: System Inactivity Timer Register

IO mapped (base pointer: C3A58); offset: 9B-98h. Default: 0000_0000h.

31:18	17:16	15:8	7:0
Reserved	CLKSRC	CURCOUNT	RELOAD

RELOAD. System inactivity timer reload value. Read-write. Writes to this field cause the system inactivity timer to be reloaded with the value written. System inactivity timer reload events enabled by PMB0 and PMB4 reload this value into the timer.

CURCOUNT. Read only. System inactivity timer current count value.

CLKSRC. System inactivity timer clock source. Read-write. Specifies the clock to the system inactivity timer per the following table.

CLKSRC	Clock period	Maximum time (clock period times 255)
00b	64 milliseconds	16.32 seconds
01b	1 second	255 seconds = 4.25 minutes
10b	16 seconds	68 minutes = 1.13 hours
11b	256 seconds	1088 minutes = 18.13 hours

PM[B0:A8]: Trap Registers

The following table provides the hardware events associated with the status, interrupt enable, and system inactivity timer reload events associated with these registers:

Bit	Hardware reload trigger	Address specification	Notes
0	Access to the master primary IDE drive.	IO space 1F0-1F7h, 3F6h	1
1	Access to the slave primary IDE drive.	IO space 1F0-1F7h, 3F6h	1
2	Access to the master secondary IDE drive.	IO space 170-177h, 376h	2
3	Access to the slave secondary IDE drive.	IO space 170-177h, 376h	2
4	Access to the primary or secondary floppy disk controllers.	IO space 3F0-3F5h, 3F7h, 370-375h, 377h fixed	
5	Access to the parallel ports.	IO space 378-37Fh, 278-27Fh, 3BC-3BFh	
6	Access to serial port COMA.	C3AA0, C3AA4	
7	Access to serial port COMB.		
8	Access to the audio hardware.	C3AA8, C3AAC, C3AB0	
9	Access to the video adapter.	IO space 3B0-3DFh; memory space 0A0000-0BFFFFh	
10	Access to the legacy keyboard and mouse ports.	IO space 60h, 64h	
11	Access to PCMCIA slot 1.	C3AB4, C3AB8, C3ABC, C3AC0	
12	Access to PCMCIA slot 2.		
13	USB controller activity.	Any USB controller DMA activity.	
14	Access to programmable IO range monitor 1.	C3AC4, C3AC8, C3ACC	
15	Access to programmable IO range monitor 2.		
16	Access to programmable IO range monitor 3.		
17	Access to programmable IO range monitor 4.		
18	Access to programmable memory range monitor 1.	C3AD0, C3AD4, C3AD8	
19	Access to programmable memory range monitor 2.		

Note 1: The IDE register at IO address PORT1F6[4], specifies whether the access is to the master or slave primary drive; this decoding is as follows: 0=master and 1=slave. Also, when the primary port is in native mode, then the address is specified by C1A10 and C1A14 (not the fixed addresses shown).
Note 2: The IDE register at IO address PORT176[4], specifies whether the access is to the master or slave secondary drive; this decoding is as follows: 0=master and 1=slave. Also, when the secondary port is in native mode, then the address is specified by C1A18 and C1A1C (not the fixed addresses shown).

PMA8: Hardware Trap Status Register
IO mapped (base pointer: C3A58); offset: AB-A8h. Default: 0000_0000h. Read; set by hardware; write 1 to clear.

Each of these status bits is controlled by hardware trap events described above in PM[B0:A8]. If the trap occurs, then the status bit is set. If a status bit and corresponding enable bit in PMAC are both high, ACPI interrupts occur.

31:20	19:0
Reserved	Status bits

Bit[0] DPM_TRP_STS. IDE primary master port access trap status.
Bit[1] DPS_TRP_STS. IDE primary slave port access trap status.
Bit[2] DSM_TRP_STS. IDE secondary master port access trap status.
Bit[3] DSS_TRP_STS. IDE secondary slave port access trap status.
Bit[4] FDD_TRP_STS. Floppy disk drive access trap status.
Bit[5] LPT_TRP_STS. Parallel port (LPT) access trap status.
Bit[6] CMA_TRP_STS. Serial port A (COM A) access trap status.
Bit[7] CMB_TRP_STS. Serial port B (COM B) access trap status.
Bit[8] AUD_TRP_STS. Audio functions access trap status.
Bit[9] VID_TRP_STS. Video functions access trap status.
Bit[10] KBM_TRP_STS. Keyboard and mouse access trap status.

Bit[11] PCMCIA1_TRP_STS. PCMCIA1 access trap status.
Bit[12] PCMCIA2_TRP_STS. PCMCIA2 access trap status.
Bit[13] USB_TRP_STS. USB access or activity trap status. This bit is set high by the hardware wen a USB control, isochronous, interrupt, or bulk transfer has been attempted (at the end of the transfer across the USB bus).
Bit[14] PRM1_TRP_STS. Programmable IO range monitor 1 access trap status.
Bit[15] PRM2_TRP_STS. Programmable IO range monitor 2 access trap status.
Bit[16] PRM3_TRP_STS. Programmable IO range monitor 3 access trap status.
Bit[17] PRM4_TRP_STS. Programmable IO range monitor 4 access trap status.
Bit[18] PMM1_TRP_STS. Programmable memory range monitor 1 access trap status.
Bit[19] PMM2_TRP_STS. Programmable memory range monitor 2 access trap status.

PMAC: Hardware Trap Enable Register
IO mapped (base pointer: C3A58); offset: AF-ACh. Default: 0000_0000h. Read-write.

For each of these bits: 1=enable the corresponding bit in the hardware trap status register, PMA8, to generate SMI or SCI interrupts (based on the state of PM04[SCI_EN]). Also, when an enabled status bit is set, PM28[TRP_EVT] is asserted.

31:20	19:0
Reserved	Enable bits

Bit[0] DPM_TRP_EN. IDE primary master port access trap enable.
Bit[1] DPS_TRP_EN. IDE primary slave port access trap enable.
Bit[2] DSM_TRP_EN. IDE secondary master port access trap enable.
Bit[3] DSS_TRP_EN. IDE secondary slave port access trap enable.
Bit[4] FDD_TRP_EN. Floppy disk drive access trap enable.
Bit[5] LPT_TRP_EN. Parallel port (LPT) access trap enable.
Bit[6] CMA_TRP_EN. Serial port A (COM A) access trap enable.
Bit[7] CMB_TRP_EN. Serial port B (COM B) access trap enable.
Bit[8] AUD_TRP_EN. Audio functions access trap enable.
Bit[9] VID_TRP_EN. Video functions access trap enable.
Bit[10] KBM_TRP_EN. Keyboard and mouse access trap enable.
Bit[11] PCMCIA1_TRP_EN. PCMCIA1 access trap enable.
Bit[12] PCMCIA2_TRP_EN. PCMCIA2 access trap enable.
Bit[13] USB_TRP_EN. USB access or activity trap enable.
Bit[14] PRM1_TRP_EN. Programmable range monitor 1 access trap enable.
Bit[15] PRM2_TRP_EN. Programmable range monitor 2 access trap enable.
Bit[16] PRM3_TRP_EN. Programmable range monitor 3 access trap enable.
Bit[17] PRM4_TRP_EN. Programmable range monitor 4 access trap enable.
Bit[18] PMM1_TRP_EN. Programmable memory range monitor 1 access trap enable.
Bit[19] PMM2_TRP_EN. Programmable memory range monitor 2 access trap enable.

PMB0: Hardware Trap Reload Enable For System Inactivity Timer Register
IO mapped (base pointer: C3A58); offset: B3-B0h. Default: 0000_0000h. Read-write.

For bits[19:0]: 1=enables the corresponding hardware trap in PMA8 to reload the system inactivity timer.

31:22	21:0
Reserved	Reload enable bits

Bit[0] DPM_TRP_RLEN. IDE primary master port access trap causes reload of system inactivity timer.
Bit[1] DPS_TRP_RLEN. IDE primary slave port access trap causes reload of system inactivity timer.
Bit[2] DSM_TRP_RLEN. IDE secondary master port access trap causes reload of system inactivity timer.
Bit[3] DSS_TRP_RLEN. IDE secondary slave port access trap causes reload of system inactivity timer.
Bit[4] FDD_TRP_RLEN. Floppy disk drive access trap causes reload of system inactivity timer.
Bit[5] LPT_TRP_RLEN. Parallel port (LPT) access trap causes reload of system inactivity timer.
Bit[6] CMA_TRP_RLEN. Serial port A (COM A) access trap causes reload of system inactivity timer.

Bit[7] CMB_TRP_RLEN. Serial port B (COM B) access trap causes reload of system inactivity timer.
Bit[8] AUD_TRP_RLEN. Audio functions access trap causes reload of system inactivity timer.
Bit[9] VID_TRP_RLEN. Video functions access trap causes reload of system inactivity timer.
Bit[10] KBM_TRP_RLEN. Keyboard and mouse access trap causes reload of system inactivity timer.
Bit[11] PCMCIA1_TRP_RLEN. PCMCIA1 access trap causes reload of system inactivity timer.
Bit[12] PCMCIA2_TRP_RLEN. PCMCIA2 access trap causes reload of system inactivity timer.
Bit[13] USB_TRP_RLEN. USB access or activity trap causes reload of system inactivity timer.
Bit[14] PRM1_TRP_RLEN. Programmable range monitor 1 access trap causes reload of system inactivity timer.
Bit[15] PRM2_TRP_RLEN. Programmable range monitor 2 access trap causes reload of system inactivity timer.
Bit[16] PRM3_TRP_RLEN. Programmable range monitor 3 access trap causes reload of system inactivity timer.
Bit[17] PRM4_TRP_RLEN. Programmable range monitor 4 access trap causes reload of system inactivity timer.
Bit[18] PMM1_TRP_RLEN. Programmable memory range monitor 1 access trap causes reload of system inactivity timer.
Bit[19] PMM2_TRP_RLEN. Programmable memory range monitor 2 access trap causes reload of system inactivity timer.
Bit[20] EXTSMI_RLEN. 1=Assertion of PM20[EXSMI_STS] causes a reload of the system inactivity timer. Note: As long as the status bit is set, the system inactivity timer is held in its reload value and does not decrement.
Bit[21] BMREQ_RLEN. 1=Assertion of a PCI bus master request causes a reload of the system inactivity timer.

PMB4: IRQ Reload Enable For System Inactivity Timer Register
IO mapped (base pointer: C3A58); offset: B7-B4h. Default: 0000_0000h. Read-write.

31:16	15:0
Reserved	IRQRL

IRQRL. IRQs reload the system inactivity timer. Each of these bits corresponds its bit number to an IRQ number to the legacy PIC (e.g., bit[12] corresponds to IRQ12). The exception to this is bit[2], which corresponds to the INTR pin, output of the legacy PIC. 1=Enable the corresponding interrupt signal to cause the system inactivity timer to reload when it transitions. 0=Do not affect the system inactivity timer.

PM[D3:C0]: General-Purpose IO Pins GPIO[19:0] Select Registers
PM[FF:F4]: General-Purpose IO Pins GPIO[31:20] Select Registers
IO mapped (base pointer: C3A58); offset: D3-C0h and F5-F4h (one single-byte register for each GPIO pin).
Default: see the MODE field definition.

See section 4.6.5 for details about GPIO hardware.

Usage note: to set a GPIO pin as a software-controlled output, its corresponding GPIO register should be written with the value 04h for a low and the value 05h for a high.

7	6	5	4	3:2	1	0
Reserved	LTCH_STS	RTIN	DEBOUNCE	MODE[1:0]	X1	X0

X[1:0]. Read-write. Extra select bits. These bits have meaning for GPIO pin inputs and outputs and to control the input paths to some alternative functions on these pins. This field is encoded as follows based on if the pin is programmed as an input or output.

IO (MODE)	Bit	Name	Function
Input	X0	ACTIVEHI	0=The pin is active low and the signal is inverted as it is brought into the input path. 1=The pin is active high and therefore not inverted as it is brought through the input path.
Input	X1	LATCH	0=The latched version of the signal is not selected. 1=The latch output is selected.
Output	X[1:0]=0h		Output is forced low.
Output	X[1:0]=1h		Output is forced high.
Output	X[1:0]=2h		GPIO output clock 0 (specified by PMDC[15:0]).
Output	X[1:0]=3h		GPIO output clock 1 (specified by PMDC[31:16]).

MODE[1:0]. Pin mode select. Read-write. These specify the GPIO pin modes as follows:

MODE[1:0]	GPIO pin mode
00b	General purpose input
01b	General purpose output
1xb	Pin specified to perform alternate function (non-GPIO mode). For GPIO[13, 16], MODE[0] selects between two alternate functions. For GPIO[31:24, 17, 9, 2], no alternate function exists, so this mode is not valid.

DEBOUNCE. Debounce the input signal. Read-write. 1=The input signal is required to be held active without glitches for 12 to 16 milliseconds before being allowed to set the GPIO latch or being capable of being passed along to the circuitry being controlled by the output of the input path.
RTIN. Real time in. Read only. This provides the current, not-inverted state of the pad for the pin that corresponds to the register.
LTCH_STS. GPIO latch status. Read; set by hardware; write 1 to clear. This provides the current state of the latch associated with the input path for the pin that corresponds to the register. This may be cleared by writing a 1 to this location or through PMD4.

The table below shows the default states for the GPIO registers and the pin definitions base on the state of MODE[1:0]. The “Default” column shows the defaults for all the bits in the register. The “Mode” field shows the value required in order to enable the function specified in the “Signal Name” column (“x” specifies that the bit does not matter). The “Input Path” field shows how the alternate function signal is mapped into internal logic; “GPIO” specifies that the signal passes through the GPIO input path (and may therefore use the polarity, latch, and debounce controls from the GPIO circuit); “Direct” specifies that the signal comes directly from the pad; “NA” specifies that it is an output signal.

GPIO name	Control register	Signal Name	Default	MODE	Alternate Functions	Input Path	Notes
GPIO[0]	PMC0	SMBUSC	08h (SMBUSC)	1xb	SMBUSC	Direct	2
GPIO[1]	PMC1	SMBUSD	08h (SMBUSD)	1xb	SMBUSD	Direct	2
GPIO[2]	PMC2	GPIO2	00h (GPIO input)				1
GPIO[3]	PMC3	SLPBTN#	0Ch (SLPBTN#)	1xb	SLPBTN#	GPIO	1, 2
GPIO[4]	PMC4	SUSPEND#	08h (SUSPEND#)	1xb	SUSPEND#	NA	
GPIO[5]	PMC5	CPUSLEEP#	05h (GPIO output, high)	1xb	CPUSLEEP#	NA	
GPIO[6]	PMC6	CPUSTOP#	05h (GPIO output, high)	1xb	CPUSTOP#	NA	
GPIO[7]	PMC7	PCISTOP#	05h (GPIO output, high)	1xb	PCISTOP#	NA	
GPIO[8]	PMC8	CACHE_ZZ	04h (GPIO output, low)	1xb	CACHE_ZZ	NA	
GPIO[9]	PMC9	GPIO9	05h (GPIO output, high)				
GPIO[10]	PMCA	FLAGWR	04h (GPIO output, low)	1xb	FLAGWR	NA	
GPIO[11]	PMCB	FLAGRD#	05h (GPIO output, high)	1xb	FLAGRD#	NA	
GPIO[12]	PMCC	EXTSMI#	0Ch (EXTSMI#)	1xb	EXTSMI#	GPIO	2
GPIO[13]	PMCD	PRDY	0Ch (No function)	10b	PRDY	Direct	
				11b	No function (input)	NA	
GPIO[14]	PMCE	RI#	08h (RI#)	1xb	RI#	GPIO	2
GPIO[15]	PMCF	C32KHZ	04h (GPIO output, low)	1xb	C32KHZ	NA	
GPIO[16]	PMD0	INTIRQ8#	05h (GPIO output, high)	10b	INTIRQ8#	NA	
				11b	SQWAVE	NA	
GPIO[17]	PMD1	GPIO17	00h (GPIO input)				
GPIO[18]	PMD2	GPIO18	00h (GPIO input)	1xb	PNPIRQ0	GPIO	
GPIO[19]	PMD3	GPIO19	00h (GPIO input)	1xb	PNPIRQ1	GPIO	
GPIO[20]	PMF4	GPIO20	00h (GPIO input)	1xb	PNPIRQ2	GPIO	
GPIO[21]	PMF5	GPIO21	08h (BMREQ#)	1xb	BMREQ#	Direct	3
GPIO[22]	PMF6	GPIO22	05h (GPIO output, high)	1xb	PNPCS0#	NA	
GPIO[23]	PMF7	GPIO23	05h (GPIO output, high)	1xb	PNPCS1#	NA	
GPIO[24]	PMF8	GPIO24	05h (GPIO output, high)				
GPIO[25]	PMF9	GPIO25	04h (GPIO output, low)				
GPIO[26]	PMFA	GPIO26	04h (GPIO output, low)				
GPIO[27]	PMFB	GPIO27	04h (GPIO output, low)				
GPIO[28]	PMFC	GPIO28	00h (GPIO input)				
GPIO[29]	PMFD	GPIO29	00h (GPIO input)				
GPIO[30]	PMFE	GPIO30	00h (GPIO input)				
GPIO[31]	PMFF	GPIO31	00h (GPIO input)				

Note 1: The output of the input path for GPIO[17, 16, 3, 2] is also routed to the IOAPIC to drive the interrupt request inputs to some of the redirection register entries (see section 4.3.4.2.2). These signals, to the IOAPIC, are never disabled, even if the alternate function is selected.

Note 2: PMC0, PMC1, PMC3, PMCC, and PMCE all reside on the VDD_AUX power plane.

Note 3: If PMF5 does not select the BMREQ# function, then IRQ[11:9, 7:3] are selected to be the REQ[7:0]# function.

PMD4: GPIO Pin Interrupt Status Register

IO mapped (base pointer: C3A58); offset: D7-D4h. Default: 0000_0000h. Read; set by hardware; write 1 to clear.

Each of these status bits is driven by the output of the input circuit associated with the GPIO pins. Bit[0] corresponds to GPIO 0; bit[1] corresponds to GPIO1, and so forth. The latch associated with each GPIO input circuit is cleared when the corresponding bit in this register is written with a 1; writing a 0 has no effect.

31:0
GPIO IRQ status bits

PMD8: GPIO Pin Interrupt Enable Register
IO mapped (base pointer: C3A58); offset: DB-D8h. Default: 0000_0000h. Read-write.

For each of these bits: 1=Enable either an SCI or SMI interrupt based on the state of PM04[SCI_EN] if the corresponding status bit in PMD4 is set. Note: If C3A42[GPIOSCI] is low, these SCI/SMI interrupts are disabled. However, if PM2A[GPIOSMI_EN] is high, an SMI is generated regardless of the state of C3A42[GPIOSCI].

31:0
GPIO IRQ enable bits

PMDC: GPIO Output Clock 0 and 1 Register
IO mapped (base pointer: C3A58); offset: DF-DCh. Default: FFFF_FFFFh. Read-write.

This register specifies the high time and the low time for the GPIO output clocks. These clocks may be selected as the output for any of the GPIO pins. These output clocks consist of a 7-bit down counter that is alternately loaded with the high time and the low time. The clock for the counters is selected by CLK[1,0]BASE.

31:30	29:23	22:16	15:14	13:7	6:0
CLK1BASE	CLK1HI	CLK1LO	CLK0BASE	CLK0HI	CLK0LO

CLK[1:0]LO. GPIO output clock 0 and 1 low time. Specifies the low time for the GPIO output clocks in increments of the clock period specified by CLK[1,0]BASE (e.g., if the base is 16 milliseconds, then 0 specifies 16 milliseconds, 1 specifies 32 milliseconds, etc.). CLK0LO specifies the low time for GPIO output clock 0 and CLK1LO specifies the low time for GPIO output clock 1.
CLK[1:0]HI. GPIO output clock 0 and 1 high time. Specifies the high time for the GPIO output clocks in increments of the clock period specified by CLK[1,0]BASE (e.g., if the base is 16 milliseconds, then 0 specifies 16 milliseconds, 1 specifies 32 milliseconds, etc.). CLK0HI specifies the high time for GPIO output clock 0 and CLK1HI specifies the high time for GPIO output clock 1.
CLK[1:0]BASE. GPIO output clock timer base. Specifies the clock for the counter that generates the GPIO output clock. 00b specifies a clock period of 250 microseconds; 01b specifies a clock period of 2 milliseconds; 10b specifies a clock period of 16 milliseconds; and 11b specifies a clock period of 128 milliseconds. CLK0BASE specifies the clock for GPIO output clock 0 and CLK1BASE specifies the clock for GPIO output clock 1.

PME0: SMBus Global Status Register
IO mapped (base pointer: C3A58); offset: E1-E0h. Default: 0000h.

Some of these bits have the ability to generate an SCI/SMI interrupt, if they are enabled to do so in PME2.

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	SMB_BSY	SMBA_STS	HSLV_STS	SNP_STS
7	6	5	4	3	2	1	0
Reserved	Reserved	TO_STS	HCYC_STS	HST_BSY	PRERR_STS	COL_STS	ABRT_STS

ABRT_STS. Host transfer abort status. Read; set by hardware; write 1 to clear. 1=A host transfer was aborted by the PME2[ABORT] command.
COL_STS. Host collision status. Read; set by hardware; write 1 to clear. 1=A host transfer was attempted while the SMBus was busy.
PRERR_STS. Protocol error status. Read; set by hardware; write 1 to clear. 1=A slave device did not generate an acknowledge at the appropriate time during a host SMBus cycle.
HST_BSY. Host controller busy. Read only. 1=The SMBus host controller is currently busy with a cycle.
HCYC_STS. Host cycle complete status. Read; set by hardware; write 1 to clear. 1=A host cycle completed successfully.
TO_STS. Time out error status. Read; set by hardware; write 1 to clear. 1=A slave device forced a time out by holding the SMBUSC pin low for more than 30 milliseconds.
SNP_STS. Snoop address match status. Read; set by hardware; write 1 to clear. 1=An SMBus master (including the host controller) generated an SMBus cycle with a 7-bit address that matched the one specified by PMEF. This bit is not set until the end of the acknowledge bit after the last byte is transferred over the SMBus cycle; if a time out

occurs after the address match occurs and before the last acknowledge, then this bit is not set. This bit resides on the VDD_AUX power plane.
HSLV_STS. Host-as-slave address match status. Read; set by hardware; write 1 to clear. 1=An SMBus master (including the host controller) generated an SMBus write cycle with a 7-bit address that matched the one specified by PMEE. This bit is not set until the end of the acknowledge bit after the last byte is transferred over the SMBus cycle; if a time out occurs after the address match occurs and before last acknowledge, then this bit is not set. This bit resides on the VDD_AUX power plane.
SMBA_STS. SMBALERT# interrupt status. Read; set by hardware; write 1 to clear. 1=SMBALERT# was asserted. This bit may not be set unless the SMBALERT# function is selected by C3A46[10:9].
SMB_BSY. SMBus busy. Read only. 1=The SMBus is currently busy with a cycle generated by either the host or another SMBus master.

PME2: SMBus Global Control Register
IO mapped (base pointer: C3A58); offset: E3-E2h. Default: 00h.

The _EN bits of this register work in conjunction with the _STS bits in PME0 to generate SCI or SMI interrupts (based on the state of PM04[SCI_EN]).

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	SMBA_EN	HSLV_EN	SNP_EN
7	6	5	4	3	2:0		
Reserved	Reserved	ABORT	HCYC_EN	HOSTST	CYCTYPE		

CYCTYPE. Host-generated SMBus cycle type. Read-write. This field specifies the type of SMBus cycle that is generated when it is initiated by the HOSTST command. It is encoded as follows (for each of the registers, the slave address is specified by PME4[7:1] and "receive" or "read" versus "send" or "write" is specified by PME4[0]):

CYCTYPE	SMBus Cycle Type	Registers
000b	Quick command	Data bit in PME4[0]
001b	Receive or send byte	Data in PME6[7:0]. If the address in PME4 is 0001_1001b and data received is 111_0xxxb, then another byte is received in PME6[15:8]; see the SMBALERT description in the system management section of this document.
010b	Read or write byte	Command in PME8; data in PME6[7:0]
011b	Read or write word	Command in PME8; data in PME6[15:0]
100b	Process call	Command in PME8; write data is placed in PME6[15:0]; then this data is replaced with the read data in the second half of the command
101b	Read or write block	Command in PME8; count data in PME6[5:0]; block data in the PME9 FIFO
11xb	Reserved	

HOSTST. Host start command. Write 1 only. 1=The SMBus host logic initiates the SMBus cycle specified by CYCTYPE. Writes to this field are ignored while PME0[HST_BSY] is active.
HCYC_EN. Enable host SMBus controller SMI or SCI interrupt. Read-write. 1=The SMBus host controller status bits, PME0[TO_STS, HCYC_STS, PRERR_STS, COL_STS, ABRT_STS], are enabled to generate SMI or SCI interrupts. 0=No interrupts are generated when these bits are set.
ABORT. Abort current host transfer command. Write 1 only. 1=The SMBus logic generates a stop event on the SMBus pins as soon as possible. After the stop event completes, PME0[ABRT_STS] is set high.
SNP_EN. Snoop address match interrupt enable. Read-write. 1=Enables an SMI or SCI interrupt when PME0[SNP_STS] is set. 0=No interrupts are generated when this bit is set. This bit resides on the VDD_AUX power plane.
HSLV_EN. Host-as-slave address match interrupt enable. Read-write. 1=Enables an SMI or SCI interrupt when PME0[HSLV_STS] is set. 0=No interrupts are generated when this bit is set. This bit resides on the VDD_AUX power plane.
SMBA_EN. SMBALERT# interrupt enable. Read-write. 1=Enables an SMI or SCI interrupt when PME0[SMBA_STS] is set. 0=No interrupts are generated when this bit is set. This bit has no effect unless the SMBALERT# function is selected by C3A46[10:9].

PME4: SMBus Host Address Register
IO mapped (base pointer: C3A58); offset: E5-E4h. Default: 0000h. Read-write.

15:8	7:1	0
HST10BA	HSTADDR	READCYC

READCYC. Host read (high) write (low) cycle. 1=Specifies that the cycle generated by a write to PM02[HOSTST] is a read or receive command. 0=Cycle is a write or send command.
HSTADDR. Host cycle address. This specifies the 7-bit address to the SMBus generated by the host (as a master) during SMBus cycles that are initiated by PME02[HOSTST].
HST10BA. Host 10-bit address LSBs. This field stores the second byte of the address, used in 10-bit SMBus host-as-master transfers. If HSTADDR == 1111_0xxb, then the cycle is specified to use 10-bit addressing. If HSTADDR is any other value, then HST10BA is not utilized.

PME6: SMBus Host Data Register
IO mapped (base pointer: C3A58); offset: E7-E6h. Default: 0000h. Read-write.

15:0
HSTDATA

HSTDATA. Host cycle data. This register is written to by software to specify the data to be passed to the SMBus during write and send cycles. It is read by software to specify the data passed to host controller by the SMBus during read and receive cycles. Bit[0] specifies the data written or read during the quick command cycle. Bits[7:0] specify the data for byte read and write cycles, send byte cycles, and receive byte cycles. Bits[15:0] are used for word read and write cycles and process calls. Bits[5:0] are used to specify the count for block read and write cycles.

PME8: SMBus Host Command Field Register
IO mapped (base pointer: C3A58); offset: E8h. Default: 00h. Read-write.

7:0
HSTCMD

HSTCMD. Host cycle command. This specifies the command field passed to the SMBus by the host controller during read byte, write byte, read word, write word, process call, block read, and block write cycles. Host cycles are initiated by PME2[HOSTST].

PME9: SMBus Host Block Data FIFO Access Port
IO mapped (base pointer: C3A58); offset: E9h. Default: 00h.

7:0
HSTFIFO

HSTFIFO. Host block read-write FIFO. For block write commands, software writes 1 to 32 bytes into this port before sending them to the SMBus via the PME2[HOSTST] command. For block read commands, software read 1 to 32 bytes from this port after the block read cycle is complete. If, during a block read or write, an error occurs, then the FIFO is flushed by the hardware. Read and write accesses to this port while the host is busy (PME0[HST_BSY]) are ignored.

PMEA: SMBus Host-As-Slave Data Register
IO mapped (base pointer: C3A58); offset: EB-EAh. Default: 0000h. Read only.

This register resides on the VDD_AUX power plane.

15:0
HSLVDATA

HSLVDATA. Host-as-slave data. When the SMBus logic determines that the current SMBus cycle is directed to the host's slave logic (because the address matches PMEE), then the data targeted to the IC during the cycle is latched in this register. Also, if the address matches the snoop address in PMEF, then the cycle is assumed to be a write word and the data is stored in this register.

PMEC: SMBus Host-As-Slave Device Address Register
IO mapped (base pointer: C3A58); offset: ED-ECh. Default: 0000h. Read only.

This register resides on the VDD_AUX power plane.

15:8	7:1	0
HSLV10DA	HSLVDA	SNPLSB

SNPLSB. Snoop command LSB. If the SMBus cycle address matches PMEF, then the cycle is assumed to be a write word. The LSB of the command field for the cycle is placed in this bit (and the other 7 bits are placed in HSLVDA).
HSLVDA. Host-as-slave device address. When the SMBus logic determines that the current SMBus cycle is directed to the host's slave logic (because the address matches PMEE), then the device address transmitted to the IC during the command phase of the cycle is latched in this register. Also, if the SMBus address matches the snoop address in PMEF, then the cycle is assumed to be a write word and bits[7:1] of the command field for the cycle are placed in this field.
HSLV10DA. Host-as-slave 10-bit device address LSBs. This field stores the second byte of the device address used in 10-bit SMBus transfers to the host as a slave. If HSLVDA == 1111_0xxb, then the cycle is specified to transmit a 10-bit device address to the host-as-slave logic and the second byte of that device address is stored in this field. If HSLVDA is any other value, then HSLV10BA is not utilized.

PMEE: SMBus Host-As-Slave Host Address Register
IO mapped (base pointer: C3A58); offset: EEh. Default: 10h. Read-write.

This register resides on the VDD_AUX power plane.

7:1	0
HSLVADDR	Reserved

HSLVADDR. Host-as-slave address. The SMBus logic compares the address generated by masters over the SMBus to this field to determine if there is a match (also, for a match to occur, the read-write bit is required to specify a write command). If a match occurs, then the cycle is assumed to be a write word command to the host, with the slave's device address transmitted during the normal command phase. The device address is captured in PMEC and the data is capture in PMEA for the cycle. After the cycle is complete, PME0[HSLV_STS] is set.

PMEF: SMBus Snoop Address Register
IO mapped (base pointer: C3A58); offset: EFh. Default: 10h. Read-write.

This register resides on the VDD_AUX power plane.

7:1	0
SNPADDR	Reserved

SNPADDR. Snoop address. The SMBus logic compares the address generated by masters over the SMBus to this field to determine if there is a match (regardless as to whether it is a read or a write). If there is a match, then PME0[SNP_STS] is set after the cycle completes. If the address specified here matches PMEE, then PME0[SNP_STS] is not set.

PM[F5:F4]: General-Purpose IO Pins GPIO[21:20] Select Registers
See PMC0 for definitions.

6 Electrical Data

6.1 Absolute Ratings

The IC is not designed to operate beyond the parameters shown in the following table.

Note: The absolute ratings in the following table and associated conditions must be adhered to in order to avoid damage to the IC. Systems using the IC must be designed to ensure that the power supply and system logic board guarantee that these parameters are not violated. VIOLATION OF THE ABSOLUTE RATINGS WILL VOID THE PRODUCT WARRANTY.

Absolute ratings.

Parameter	Minimum	Maximum	Comments
VDD3	-0.5 V	3.6 V	
VDD_AUX	-0.5 V	3.6 V	
VDD_REF	-0.5 V	5.25 V	
VDD_RTC	-0.5 V	3.6 V	
VDD_USB	-0.5 V	3.6 V	
V_{PIN}	-0.5 V	5.25 V	
T_{CASE} (under bias)		85 degrees C	
$T_{STORAGE}$	-65 degrees C	150 degrees C	

Note: This table contains preliminary information, which is subject to change.

6.2 Operating Ranges

The IC is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in the following table.

Parameter	Minimum	Typical	Maximum	Comments
VDD3	3.135 V	3.3 V	3.465 V	
VDD_AUX	3.135 V	3.3 V	3.465 V	
VDD_REF	4.75 V	5.0 V	5.25 V	
VDD_RTC	3.135 V	3.3 V	3.465 V	
VDD_USB	3.135 V	3.3 V	3.465 V	
T_{case}			85 degrees C	

Note: This table contains preliminary information, which is subject to change.

6.3 DC Characteristics

DC characteristics for PCI signals are available in the PCI specification. DC characteristics for the IDE signals are available from the ATA specification. DC characteristics for the USB signals are available from the USB specification. The following table provides the DC characteristics for the remaining signals in the IC.

Symbol	Parameter Description	Min	Max	Comments
V_{IL}	Input low voltage	-0.5 V	0.8 V	
V_{IH}	Input high voltage	2.0 V	5.5 V	
V_{OL}	Output low voltage		0.45 V	
V_{OH}	Output high voltage	2.4 V		
I_{LI}	Input leakage current	-10 uA	10 uA	$0 < V_{IN} <$ VDD
C_{IN}	Input capacitance		10 pf	

Note: This table contains preliminary information, which is subject to change.

6.4 Power Dissipation

The following table provides current consumption of the IC while it is operational.

Supply	Max
VDD3	200 mA
VDD_REF	1.0 mA
VDD_USB	50 mA

Note: This table contains preliminary information, which is subject to change.

6.5 Switching Characteristics

Switching characteristics for PCI signals are available in the PCI specification. Switching characteristics for the IDE signals are available from the ATA specification. Switching characteristics for the USB signals are available from the USB specification.

7 Pin Designations

Top side view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	SA1	SA2	SD7	IOCHK#	GPIO 22	AD3	AD2	CBE_L0	AD12	AD14	SERR #	TRDY #	CBE_L2	AD21	AD22	AD25	AD29	AD31	PGNT #	PCLK	A
B	GPIO17	SA0	SD5	SD6	GPIO26	AD1	AD6	AD8	AD10	AD13	AD15	STOP #	IDSEL	AD18	AD20	AD23	AD27	AD30	PREQ #	USB OC0#	B
C	LA23	GPIO19	SD4	IRQ9	STRAP L0	AD0	AD4	AD9	CBE_L1	DEV SEL#	FRAME #	AD17	AD19	AD24	AD28	PIRQA#	PIRQD#	PIRQB#	USB CLK	VDD_USB	C
D	LA22	GPIO18	SD3	VDD3	TEST#	AD5	AD7	AD11	PAR	IRDY#	VDD3	AD16	CBE_L3	AD26	STRAP L3	PIRQC#	VDD3	USBP3	USBN3	USBP2	D
E	LA21	IRQ10	SD2	EKIRQ 12													USBN2	USBP1	USBN1	USBP0	E
F	LA20	IRQ11	SD0	SD1													USBN0	VSS_USB	VDD_RTC	RTCX_IN	F
G	LA19	IRQ12	GPIO25	IOCH RDY													RTCX_OUT	INTRUDER#	SMBUSC	SMBUSD	G
H	LA18	IRQ15	SA16	GPIO21													SLP BTN#	PWR BTN#	EXT SMI#	PME#	H
J	LA17	IRQ14	IOW#	GPIO20					VSS	VSS	VSS	VSS					PWR ON#	PWR GD	VDD_AUX	STRAP H1	J
K	MEMR#	KA20G	CPU SLEEP#	IOR#					VSS	VSS	VSS	VSS					STRAP H0	RPWR ON	PCI RST#	RI#	K
L	MEMW#	KBRC#	GPIO9	VDD3					VSS	VSS	VSS	VSS					VDD3	STRAP L1	DC STOP#	STRAP H2	L
M	LAD0	STRAP L2	SA14	SA15					VSS	VSS	VSS	VSS					SMI#	A20M #	SUS PEND#	FLAG RD#	M
N	LAD1	GPIO2	PRDY	VDD_REF													STP CLK#	WSC#	CPU RST#	ROM_KBCS#	N
P	LAD2	GPIO29	EKIRQ1	SA13													SER IRQ	PCI STOP#	CPU STOP#	CACHE_ZZ	P
R	LAD3	GPIO28	GPIO23	SA12													INTR	NMI	PICD1#	PICD0#	R
T	LFRAME #	GPIO31	SA10	SA11													PIC CLK#	IGNNE#	FERR #	INIT#	T
U	LDRQ0#	GPIO30	SA9	VDD3	IRQ7	SA7	SA6	SA5	SA4	SA3	VDD3	DDATAS7	DDATAS5	DDATAS12	DDATAS13	DDATAS14	VDD3	DADDRP0	THERM #	OSC	U
V	LDRQ1#	BCLK	SA8	IRQ6	IRQ5	IRQ4	IRQ3	FLAG WR	GPIO27	INT IRQ8#	SPKR	DDATAS6	DDATAS4	DDATAS3	DDATAS2	DDATAS1	DDATAS15	DADDRP2	DCS1S#	C32 KHZ	V
W	GPIO24	DDATAP8	DDATAS8	DDATAP6	DDATAP10	DDATAS10	DDATAP4	DDATAP12	DDATAP13	DDATAP14	DDATAP15	DDRQS	DIOWS#	DIORS#	DRDYS	DDACKS#	DADDRS1	DADDRS0	DCS1P#	DCS3S#	W
Y	ISA BIOS	DDATAP7	DDATAP9	DDATAS9	DDATAP5	DDATAP11	DDATAS11	DDATAP3	DDATAP2	DDATAP1	DDATAP0	DDRQP	DIOWP#	DIORP#	DRDYP	DDACKP#	DADDRP1	DDATAS0	DADDRS2	DCS3P#	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Alphabetical listing of signals and corresponding BGA designators.

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
A20M#	M18	DCS1S#	V19	FERR#	T19	LA21	E1
AD0	C6	DCS3P#	Y20	FLAGRD#	M20	LA22	D1
AD1	B6	DCS3S#	W20	FLAGWR	V8	LA23	C1
AD2	A7	DCSTOP#	L19	FRAME#	C11	LAD[0]	M1
AD3	A6	DDACKP#	Y16	GPIO2	N2	LAD[1]	N1
AD4	C7	DDACKS#	W16	GPIO9	L3	LAD[2]	P1
AD5	D6	DDATAP0	Y11	GPIO17	B1	LAD[3]	R1
AD6	B7	DDATAP1	Y10	GPIO18	D2	LDRQ0#	U1
AD7	D7	DDATAP2	Y9	GPIO19	C2	LDRQ1#	V1
AD8	B8	DDATAP3	Y8	GPIO20	J4	LFRAME#	T1
AD9	C8	DDATAP4	W7	GPIO21	H4	MEMR#	K1
AD10	B9	DDATAP5	Y5	GPIO22	A5	MEMW#	L1
AD11	D8	DDATAP6	W4	GPIO23	R3	NMI	R18
AD12	A9	DDATAP7	Y2	GPIO24	W1	OSC	U20
AD13	B10	DDATAP8	W2	GPIO25	G3	PAR	D9
AD14	A10	DDATAP9	Y3	GPIO26	B5	PCIRST#	K19
AD15	B11	DDATAP10	W5	GPIO27	V9	PCISTOP#	P18
AD16	D12	DDATAP11	Y6	GPIO28	R2	PCLK	A20
AD17	C12	DDATAP12	W8	GPIO29	P2	PGNT#	A19
AD18	B14	DDATAP13	W9	GPIO30	U2	PIC_D0#	R20
AD19	C13	DDATAP14	W10	GPIO31	T2	PIC_D1#	R19
AD20	B15	DDATAP15	W11	IDSEL	B13	PICCLK	T17
AD21	A14	DDATAS0	Y18	IGNNE#	T18	PIRQA#	C16
AD22	A15	DDATAS1	V16	INIT	T20	PIRQB#	C18
AD23	B16	DDATAS2	V15	INTIRQ8#	V10	PIRQC#	D16
AD24	C14	DDATAS3	V14	INTR	R17	PIRQD#	C17
AD25	A16	DDATAS4	V13	INTRUDER#	G18	PME#	H20
AD26	D14	DDATAS5	U13	IOCHK#	A4	PRDY	N3
AD27	B17	DDATAS6	V12	IOCHRDY	G4	PREQ#	B19
AD28	C15	DDATAS7	U12	IOR#	K4	PWRBTN#	H18
AD29	A17	DDATAS8	W3	IOW#	J3	PWRGD	J18
AD30	B18	DDATAS9	Y4	IRDY#	D10	PWRON#	J17
AD31	A18	DDATAS10	W6	IRQ3	V7	RI#	K20
BCLK	V2	DDATAS11	Y7	IRQ4	V6	ROM_KBCS#	N20
C32KHZ	V20	DDATAS12	U14	IRQ5	V5	RPWRON	K18
CACHE_ZZ	P20	DDATAS13	U15	IRQ6	V4	RTCX_IN	F20
CBE_L0	A8	DDATAS14	U16	IRQ7	U5	RTCX_OUT	G17
CBE_L1	C9	DDATAS15	V17	IRQ9	C4	SA0	B2
CBE_L2	A13	DDRQP	Y12	IRQ10	E2	SA1	A1
CBE_L3	D13	DDRQS	W12	IRQ11	F2	SA2	A2
CPURST	N19	DEVSEL#	C10	IRQ12	G2	SA3	U10
CPUSLEEP#	K3	DIORP#	Y14	IRQ14	J2	SA4	U9
CPUSTOP#	P19	DIORS#	W14	IRQ15	H2	SA5	U8
DADDRP0	U18	DIOWP#	Y13	ISABIOS	Y1	SA6	U7
DADDRP1	Y17	DIOWS#	W13	KA20G	K2	SA7	U6
DADDRP2	V18	DRDYP	Y15	KBRC#	L2	SA8	V3
DADDRS0	W18	DRDYS	W15	LA17	J1	SA9	U3
DADDRS1	W17	EKIRQ1	P3	LA18	H1	SA10	T3
DADDRS2	Y19	EKIRQ12	E4	LA19	G1	SA11	T4
DCS1P#	W19	EXTSMI#	H19	LA20	F1	SA12	R4

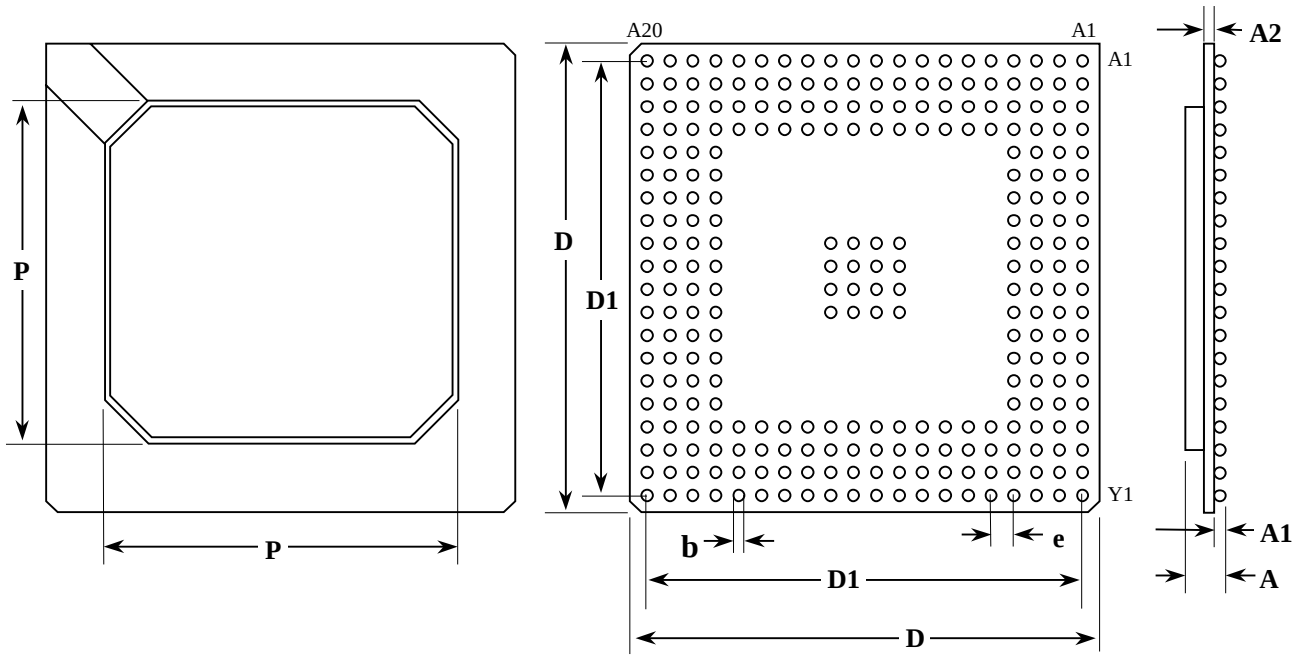
Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
SA13	P4	SLPBTN#	H17	SUSPEND#	M19	VDD_REF	N4
SA14	M3	SMBUSC	G19	TEST#	D5	VDD_RTC	F19
SA15	M4	SMBUSD	G20	THERM#	U19	VDD_AUX	J19
SA16	H3	SMI#	M17	TRDY#	A12	VDD_USB	C20
SD0	F3	SPKR	V11	USBCLK	C19	VDD3_0	D4
SD1	F4	STOP#	B12	USBN0	F17	VDD3_1	U4
SD2	E3	STPCLK#	N17	USBN1	E19	VDD3_2	D17
SD3	D3	STRAPH0	K17	USBN2	E17	VDD3_3	U17
SD4	C3	STRAPH1	J20	USBN3	D19	VDD3_4	D11
SD5	B3	STRAPH2	L20	USBOC0#	B20	VDD3_5	L4
SD6	B4	STRAPL0	C5	USBP0	E20	VDD3_6	U11
SD7	A3	STRAPL1	L18	USBP1	E18	VDD3_7	L17
SERIRQ	P17	STRAPL2	M2	USBP2	D20	VSS_USB	F18
SERR#	A11	STRAPL3	D15	USBP3	D18	WCS#	N18

8 Package Specification

The IC comes in a 272-ball Plastic Ball Grid Array (PBGA).

All dimensions are in millimeters.

Symbol	Min	Typical	Max	Description
A	2.20	2.33	2.46	Overall thickness
A1	0.50	0.60	0.70	Ball height
A2	0.51	0.56	0.61	Body thickness
D		27.00 BSC.		Body size
D1		24.13 BSC.		Ball footprint
b	0.60	0.75	0.90	Ball diameter
e		1.27 BSC.		Ball pitch
P		24.00		Encapsulation area



9 Test

The IC includes five NAND trees for continuity testing. It is also possible to place all the IO pins into the high-impedance state. These modes are entered by asserting the following pins:

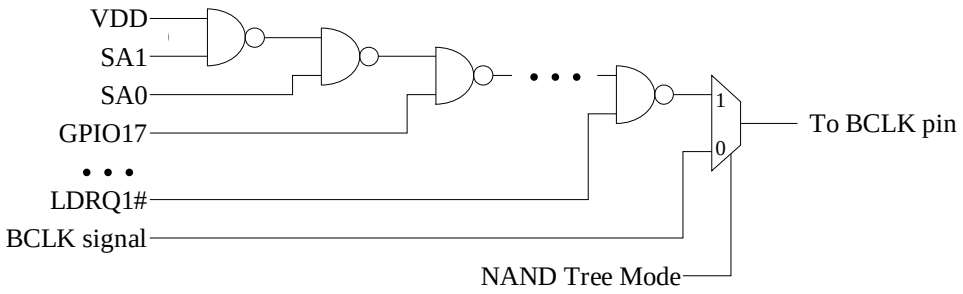
Mode	Equation to enable mode
High Impedance	~TEST# & PWRGD & ~PGNT# & ~SERR#
NAND Tree	~TEST# & PWRGD & ~PGNT# & SERR#

9.1 High Impedance Mode

When in high impedance mode, all the signals on the IC are placed into the high impedance state.

9.2 NAND Tree Mode

There are five NAND trees in the IC. The following diagram shows how these are connected, using example signals from NAND tree 1.



When in NAND tree mode, the five NAND tree output signals are enabled and the remaining signals are in high-impedance mode. The following pins are not part of the NAND tree: RTCX_IN, RTCX_OUT, PWRGD, PCLK, TEST#, PGNT#, and SERR#.

The following tables provide the signal order and output signal for each NAND tree.

NAND tree 1: output signal BCLK.

1	SA1	11	SD2	21	LA19	31	CPUSLEEP#	41	LAD1	51	SA12
2	SA0	12	IRQ10	22	GPIO21	32	KA20G	42	GPIO2	52	LFRAME#
3	GPIO17	13	LA21	23	SA16	33	MEMR#	43	PRDY	53	GPIO31
4	SD4	14	SD1	24	IRQ15	34	MEMW#	44	LAD2	54	SA10
5	GPIO19	15	SD0	25	LA18	35	KBRC#	45	GPIO29	55	SA11
6	LA23	16	IRQ11	26	GPIO20	36	GPIO9	46	EKIRQ1	56	LDRQ0#
7	SD3	17	LA20	27	IOW#	37	LAD0	47	SA13	57	GPIO30
8	GPIO18	18	IOCHRDY	28	IRQ14	38	STRAPL2	48	LAD3	58	SA9
9	LA22	19	GPIO25	29	LA17	39	SA14	49	GPIO28	59	LDRQ1#
10	EKIRQ12	20	IRQ12	30	IOR#	40	SA15	50	GPIO23		

NAND tree 2: output signal DADDRS2.

1	GPIO24	13	DDATAP10	25	DDATAP12	37	SPKR	49	DDATAS12	61	DDATAS0
2	ISABIOS	14	DDATAP5	26	DDATAP3	38	DDRQP	50	DRDYP	62	DADDRS0
3	DDATAP8	15	SA7	27	SA4	39	DDRQS	51	DRDYS		
4	DDATAP7	16	IRQ4	28	GPIO27	40	DDATAS6	52	DDATAS2		
5	SA8	17	DDATAS10	29	DDATAP13	41	DDATAS7	53	DDATAS13		
6	DDATAS8	18	DDATAP11	30	DDATAP2	42	DIOWP#	54	DDACKP#		
7	DDATAP9	19	SA6	31	SA3	43	DIOWS#	55	DDACKS#		
8	IRQ6	20	IRQ3	32	INTIRQ8#	44	DDATAS4	56	DDATAS1		
9	DDATAP6	21	DDATAP4	33	DDATAP14	45	DDATAS5	57	DDATAS14		
10	DDATAS9	22	DDATAS11	34	DDATAP1	46	DIORP#	58	DADDRP1		
11	IRQ7	23	SA5	35	DDATAP0	47	DIORS#	59	DADDRS1		
12	IRQ5	24	FLAGWR	36	DDATAP15	48	DDATAS3	60	DDATAS15		

NAND tree 3: output signal PREQ#.

1	DCS3P#	11	IGNNE#	21	CACHE_ZZ	31	USBOC0#
2	DCS1P#	12	FERR#	22	STPCLK#		
3	DCS3S#	13	INIT#	23	WSC#		
4	DADDRP2	14	INTR	24	CPURST#		
5	DCS1S#	15	NMI	25	ROM_KBCS#		
6	C32KHZ	16	PICD1#	26	SMI#		
7	DADDRP0	17	PICD0#	27	A20M		
8	THERM#	18	SERIRQ	28	SUSPEND#		
9	OSC	19	PCISTOP#	29	FLAGRD#		
10	PICCLK#	20	CPUSTOP#	30	USBCLK		

NAND tree 4: output signal SA2.

1	PIRQB#	11	STRAPL3	21	IDSEL	31	DEVSEL#	41	AD2	51	STRAPL0
2	AD30	12	AD28	22	CBE_L2	32	IRDY#	42	AD6	52	IOCHK#
3	AD31	13	AD20	23	AD16	33	AD12	43	AD4	53	SD6
4	PIRQD#	14	AD22	24	AD17	34	AD10	44	AD7	54	IRQ9
5	AD27	15	AD26	25	STOP#	35	CBE_L1	45	AD3	55	SD7
6	AD29	16	AD24	26	TRDY#	36	PAR	46	AD1	56	SD5
7	PIRQC#	17	AD18	27	FRAME#	37	CBE_L0	47	AD0		
8	PIRQA#	18	AD21	28	AD15	38	AD8	48	AD5		
9	AD23	19	CBE_L3	29	AD14	39	AD9	49	GPIO22		
10	AD25	20	AD19	30	AD13	40	AD11	50	GPIO26		

NAND tree 5: output signal PWRON#.

1	USBP3	11	SMBUSD	21	STRAPH2
2	USBN3	12	SLPBTN#	22	DCSTOP#
3	USBP2	13	PWRBTN#	23	STRAPL1
4	USBN2	14	EXTSMI#		
5	USBP1	15	PME#		
6	USBN1	16	STRAPH1		
7	USBP0	17	STRAPH0		
8	USBN0	18	RPWRON		
9	INTRUDER#	19	PCIRST#		
10	SMBUSC	20	RI#		

10 Appendixes

10.1 Appendix A: Glossary

#. This symbol at the end of a signal name or configuration bit indicates that it is active low.

FON. Full on system power state; see section 4.6.1.5.

IMB. Interrupt message bus. The bus used to transfer interrupt messages between processor local APICs and the IOAPIC of the IC. Includes signals PICCLK, PICD0# and PICD1#.

IOAPIC. IO advanced programmable interrupt controller.

MOFF. Mechanical off system power state; see section 4.6.1.5.

MP. Multiprocessor.

PIC. Programmable interrupt controller. The internal legacy dual-8259-based system interrupt controller.

PIT. Programmable interval timer. The internal legacy 8254 timer.

POS. Power on suspend system power state; see section 4.6.1.5.

Power button override event. This event occurs when PWRBTN# or SLPBTN# is held active for at least four seconds. See PM00[PBOR_STS].

RST_SOFT. This is the internal reset signal that is applied to the logic, registers, and pins that reside on the VDD_AUX power plane. See section 4.6.1.5.1.

SOFF. Soft off system power state; see section 4.6.1.5.

STD. Suspend to disk system power state; see section 4.6.1.5.

STR. Suspend to RAM system power state; see section 4.6.1.5.

USB. Universal serial bus.

10.2 Appendix B: References

Advanced Configuration and Power Interface Specification. Intel Corporation, Microsoft, and Toshiba.

AT Attachment With Packet Interface Extension. T13, a Technical Committee of Accredited Standards Committee NCITS.

Multiprocessor Specification. Intel Corporation, 1996.

OpenHCI for USB. Compaq, Microsoft, and National Semiconductor, 1997.

PCI IDE Controller Specification. PCI Special Interest Group, Hillsboro, OR, 1994.

PCI Local Bus Specification, Revision 2.2. PCI Special Interest Group, Hillsboro, OR, 1998.

Serial IRQ Specification Version 1.0. VESA (Video Electronics Standards Association), San Jose, CA.

System Management Bus Specification Revision 1.0. Benchmarq Microelectronics Inc., Duracell Inc., Energizer Power Systems, Intel Corporation, Linear Technology Corporation, Maxim Integrated Products, Mitsubishi Electric Corporation, National Semiconductor Corporation, Toshiba Battery Co., Varta Batterie AG, 1996.

Universal Serial Bus Specification Revision 1.0. Compaq, DEC, IBM, Intel Corporation, Microsoft, NEC, and Northern Telecom, 1996.

10.3 Appendix C: Conventions

Most values in this document are appended with "b" to indicate a binary value or "h" to indicate a hexadecimal value. Otherwise, the value is presumed to be a decimal value.

In this document, formulae follow Verilog numerical conventions. Here is a summary:

y'hx	'h indicates that the number that follows it, x, is in hexadecimal format. If there is a number before the 'h, y, it specifies the number of bits in x.
{}	Brackets are used to indicate a group of bits that are concatenated together.
|	Logical OR operator.
&	Logical AND operator.
~	Logical NOT operator.
==	Logical "is equal to" operator.
!=	Logical "is not equal to" operator.
*	Multiply.
//	This indicates the start of comments.

The order in which logical operators are applied is: ~ first, & second, and | last.

An X in a binary or hexadecimal value indicates that the bit(s) may be any value.