Clock Generator for Intel PCI-Express Desktop Chipset

Product Features

- 14.318 MHz Crystal Input
- Selectable of 100, 133, 166, 200, 266, 333, and 400MHz CPU Output Frequencies
- SMBus: Power Management Control
- Spread Spectrum support (-0.5% down spread)
- Packaging (Pb-free & Green available):
  -56-Pin SSOP (V)

Output Features

- Two Pairs of Differential CPU Clocks
- One selectable of CPU/SRC Clock
- Six Pairs of SRC Clocks
- Nine PCI Clocks
- One 48 MHz USB clock
- One REF clock
- One 96 MHz Differential clock

Product Description

PI6C410 is a high-speed, low-noise clock generator designed to work with Intel Desktop PCI-Express Chipset.
Spread Spectrum PLL based clock generator reduce EMI emission and support a wide range of frequencies.

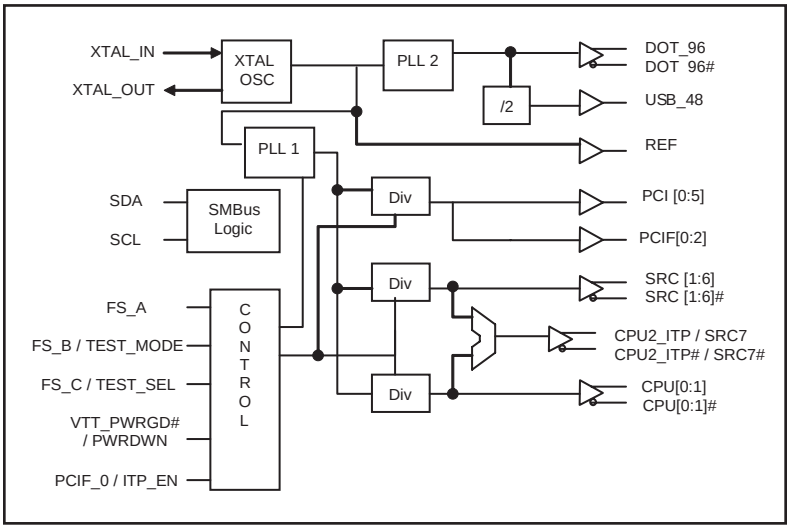
Jitter Performance

- < 85ps Cycle to Cycle CPU clock jitter
- < 350ps Cycle to Cycle 48MHz clock jitter
- < 500ps Cycle to Cycle PCI clock jitter
- < 125ps Cycle to Cycle SRC clock jitter
- < 1000ps Cycle to Cycle REF clock jitter

Skew Performance

- < 100ps Output to output CPU clock skew
- < 500ps Output to output PCI clock skew
- < 250ps Output to output SRC clock skew

Logic Block Diagram



Pin Description

VDD_PCI	1	56	PCI_2
VSS_PCI	2	55	PCI_1
PCI_3	3	54	PCI_0
PCI_4	4	53	FS_C / TEST_SEL
PCI_5	5	52	REF
VSS_PCI	6	51	VSS_REF
VDD_PCI	7	50	XTAL_IN
PCIF_0 / ITP_EN	8	49	XTAL_OUT
PCIF_1	9	48	VDD_REF
PCIF_2	10	47	SDA
VDD_48	11	46	SCL
USB_48	12	45	VSS_CPU
VSS_48	13	44	CPU_0
DOT_96	14	43	CPU_0#
DOT_96#	15	42	VDD_CPU
FS_B / TEST_MODE	16	41	CPU_1
VTT_PWRGD# / PWRDWN	17	40	CPU_1#
FS_A	18	39	IREF
SRC_1	19	38	VSS_A
SRC_1#	20	37	VDD_A
VDD_SRC	21	36	CPU2_ITP / SRC7
SRC_2	22	35	CPU2_ITP# / SRC7#
SRC_2#	23	34	VDD_SRC
SRC_3	24	33	SRC_6
SRC_3#	25	32	SRC_6#
SRC_4	26	31	SRC_5
SRC_4#	27	30	SRC_5#
VDD_SRC	28	29	VSS_SRC

Pin Description

Pin Name	Type	Pin No	Descriptions
REF	Output	52	3.3V 14.31818MHz output
XTAL_IN	Input	50	14.31818MHz crystal input
XTAL_OUT	Output	49	14.31818MHz crystal output
CPU[0:1] & CPU[0:1]#	Output	40, 41, 43, 44	Differential CPU outputs
SRC[1:6] & SRC[1:6]#	Output	19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33	Differential Serial Reference Clock outputs
CPU2_ITP / SRC_7 & CPU2_ITP# / SRC_7#	Output	35, 36	Selectable Differential CPU or SRC clock output ITP_EN = 0 @ Vtt_Pwrgd# assertion = SRC ITP_EN = 1 @ Vtt_Pwrgd# assertion = CPU
PCIF_0 / ITP_EN	Input / Output	8	33MHz clock output / CPU2 select when HIGH
PCIF[1:2]	Output	9, 10	33MHz clocks outputs (free running)
PCI[0:5]	Output	3, 4, 5, 54, 55, 56	33MHz clocks outputs
USB_48	Output	12	48MHz clock output
DOT_96 & DOT_96#	Output	14, 15	96MHz differential clock output
FS_A	Input	18	3.3V LVTTL inputs for CPU frequency selection
FS_B / TEST_MODE	Input	16	3.3V LVTTL inputs for CPU frequency selection / Test Mode select: 0 = HiZ, 1 = Ref/N
FS_C / TEST_SEL	Input	53	3.3V LVTTL inputs for CPU frequency selection / Test Mode select if pulled to 3.3V when Vtt_Pwrgd# is asserted LOW
IREF	Input	39	External resistor connection for internal current reference
VTT_PWRGD# / PWRDWN	Input	17	3.3V LVTTL Level sensitive strobe used to determine to latch the FS_A, FS_B/TEST_MODE, FS_C/TEST_SEL and PCIF0/ ITP_EN inputs (active low) / 3.3V LVTTL active high input for Power Down operation.
SDA	I/O	47	SMBus compatible SDATA
SCL	Input	46	SMBus compatible SCLOCK
VDD_PCI	Power	1, 7	3.3V Power Supply for Outputs
VDD_48	Power	11	3.3V Power Supply for Outputs
VDD_SRC	Power	21, 28, 34	3.3V Power Supply for Outputs
VDD_CPU	Power	42	3.3V Power Supply for Outputs
VDD_REF	Power	48	3.3V Power Supply for Outputs
VSS_PCI	Ground	2, 6	Ground for Outputs
VSS_48	Ground	13	Ground for Outputs
VSS_SRC	Ground	29	Ground for Outputs
VSS_CPU	Ground	45	Ground for Outputs
VSS_REF	Ground	51	Ground for Outputs
VDD_A	Power	37	3.3V Power Supply for PLL
VSS_A	Ground	38	Ground for PLL

Functionality

Frequency Selection

FS_C	FS_B	FS_A	CPU	SRC	PCIF / PCI	REF	DOT_96	USB_48	Note
1	0	1	100MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz	1
0	0	1	133MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz	1
0	1	1	166MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz	1
0	1	0	200MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz	1
0	0	0	266MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz	1
1	0	0	333MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz	1
1	1	0	400MHz	100MHz	33MHz	14.318MHz	96MHz	48MHz	1
1	1	1	Reserved	100MHz	33MHz	14.318MHz	96MHz	48MHz	1

Notes:
1. Refer to DC Electrical Characteristics for FS_A, FS_B and FS_C (Vih_FS, Vil_FS) threshold levels

Test Mode Selection

TEST_MODE	CPU	SRC	PCIF / PCI	REF	DOT_96	USB_48	Note
1	REF/N	REF/N	REF/N	REF	REF/N	REF/N	2
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	2

Notes:
2. Test mode will occur where the SMBus Bit 6 of Byte 6 = 1, or FS_C/TEST_SEL is set to logic high level.

PWRDWN Functionality

PWRDWN	CPU	CPU#	SRC	SRC#	PCIF / PCI	REF	DOT_96	DOT_96#	USB_48
0	Normal	Normal	Normal	Normal	33MHz	14.318MHz	Normal	Normal	48MHz
1	Iref × 2 or Float	Float	Iref × 2 or Float	Float	Low	Low	Iref × 2 or Float	Float	Low

Serial Data Interface (SMBus)

PI6C410 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	1/0

Data Protocol

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr	R/W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Notes:
1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Byte 0: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	Reserved	RW				
1	SRC_1 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_1	19, 20	NA
2	SRC_2 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_2	22, 23	NA
3	SRC_3 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_3	24, 25	NA
4	SRC_4 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_4	26, 27	NA
5	SRC_5 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_5	30, 31	NA
6	SRC_6 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	SRC_6	32, 33	NA
7	CPU_2 / SRC_7 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_2 / SRC_7	35, 36	NA

Data Byte 1: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	Spread Spectrum 1 = On, 0 = Off	RW	0 = Spread off	CPU[0:2], SRC[1:7], PCI[0:5], PCIF[0:2]	3, 4, 5, 8, 9, 10, 19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36, 40, 41, 43, 44, 54, 55, 56	NA
1	CPU_0 output enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_0, CPU_0#	43, 44	NA
2	CPU_1 output enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	CPU_1, CPU_1#	40, 41	NA
3	Reserved	RW				
4	REF Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	REF	52	NA
5	USB_48 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	USB_48	12	NA
6	DOT_96 Output Enable 1 = Enabled, 0 = Disabled (Hi-Z)	RW	1 = Enabled	DOT_96 & DOT96#	14, 15	NA
7	PCIF_0 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCIF_0	8	NA

Data Byte 2: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	PCIF_1 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCIF_1	9	NA
1	PCIF_2 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCIF_2	10	NA
2	PCI_0 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_0	54	NA
3	PCI_1 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_1	55	NA
4	PCI _2 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_2	56	NA
5	PCI _3 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_3	3	NA
6	PCI _4 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_4	4	NA
7	PCI _5 Output Enable 1 = Enabled, 0 = Disabled	RW	1 = Enabled	PCI_5	5	NA

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	Reserved	RW				
1	SRC_1 Output Control 0 = Free Running	RW	0 = Free running	SRC_1	19, 20	NA
2	SRC_2 Output Control 0 = Free Running	RW	0 = Free running	SRC_2	22, 23	NA
3	SRC_3 Output Control 0 = Free Running	RW	0 = Free running	SRC_3	24, 25	NA
4	SRC_4 Output Control 0 = Free Running	RW	0 = Free running	SRC_4	26, 27	NA
5	SRC_5 Output Control 0 = Free Running	RW	0 = Free running	SRC_5	30, 31	NA
6	SRC_6 Output Control 0 = Free Running	RW	0 = Free running	SRC_6	32, 33	NA
7	SRC_7 Output Control 0 = Free Running	RW	0 = Free running	SRC_7	35, 36	NA

Data Byte 4: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	CPU_0 Output Control 0 = Free Running	RW	0 = Free running	CPU_0	43, 44	NA
1	CPU_1 Output Control 0 = Free Running	RW	0 = Free running	CPU_1	40, 41	NA
2	CPU_2 Output Control 0 = Free Running	RW	0 = Free running	CPU_2	35, 36	NA
3	PCIF_0 Output Control 0 = Free Running	RW	0 = Free running	PCIF_0	8	NA
4	PCIF_1 Output Control 0 = Free Running	RW	0 = Free running	PCIF_1	9	NA
5	PCIF_2 Output Control 0 = Free Running	RW	0 = Free running	PCIF_2	10	NA
6	DOT_Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	DOT_96 & DOT_96#	14, 15	NA
7	Reserved	RW				

Data Byte 5: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	CPU_0 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	CPU_0 & CPU_0#	43, 44	NA
1	CPU_1 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	CPU_1 & CPU_1#	40, 41	NA
2	CPU_2 Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	CPU_2 & CPU_2#	35, 36	NA
3	SRC_Pwrdwn drive mode 1 = Hi-Z, 0 = Driven in Pwrdwn	RW	0 = Driven in power down	SRC[1:7] & SRC[1:7]#	19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36	NA
4	CPU_0 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU_Stop	RW	0 = Driven in CPU_Stop	CPU_0 & CPU_0#	43, 44	NA
5	CPU_1 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU_Stop	RW	0 = Driven in CPU_Stop	CPU_1 & CPU_1#	40, 41	NA
6	CPU_2 CPU_Stop drive mode 1 = Hi-Z, 0 = Driven in CPU_Stop	RW	0 = Driven in CPU_Stop	CPU_2 & CPU_2#	35, 36	NA
7	SRC_Stop drive mode 1 = Hi-Z, 0 = Driven in PCI_Stop	RW	0 = Driven in PCI_Stop	SRC[1:7] & SRC[1:7]#	19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36	NA

Data Byte 6: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin	Source Pin
0	FS_A Reflects the value of the FS_A pin sampled on power up 0 = FS_A was low during Vtt_Pwrgd# assertion	R	Externally Selected	CPU[0:2]	35, 36, 40, 41, 43, 44	NA
1	FS_B Reflects the value of the FS_B pin sampled on power up 0 = FS_B was low during Vtt_Pwrgd# assertion	R	Externally Selected	CPU[0:2]	35, 36, 40, 41, 43, 44	NA
2	FS_C Reflects the value of the FS_C pin sampled on power up 0 = FS_C was low during Vtt_Pwrgd# assertion	R	Externally Selected	CPU[0:2]	35, 36, 40, 41, 43, 44	NA
3	PCI_Stop Output Control 0 = Enabled, all stoppable PCI and SRC clocks are stopped 1 = Disabled	RW	1 = Disabled	All PCI & SRC clocks except PCIF and SRC clocks set to free-running	3, 4, 5, 8, 9, 10, 19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36	NA
4	REF Output Drive Strength 0 = 1x, 1 =2x	RW	1 = 2X	REF	52	NA
5	Reserved	RW				
6	Test Clock Mode Entry Control 0 = Disabled, 1 = REF/N or Hi-Z	RW	0 = Disabled			
7	Test Clock Mode 0 = Hi-Z, 1 = REF/N	RW	0 = Hi-Z	CPU[0:2], SRC[1:7], PCI[0:5], PCIF[0:2], REF, USB_48, DOT_96	3, 4, 5, 8, 9, 10, 12, 14, 15, 19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36, 40, 41, 43, 44, 52, 54, 55, 56	NA

Data Byte 7: Pericom ID Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Vendor ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4	Revision Code	R	1	NA	NA
5		R	0	NA	NA
6		R	1	NA	NA
7		R	0	NA	NA

Power Down (PWRDWN assertion)

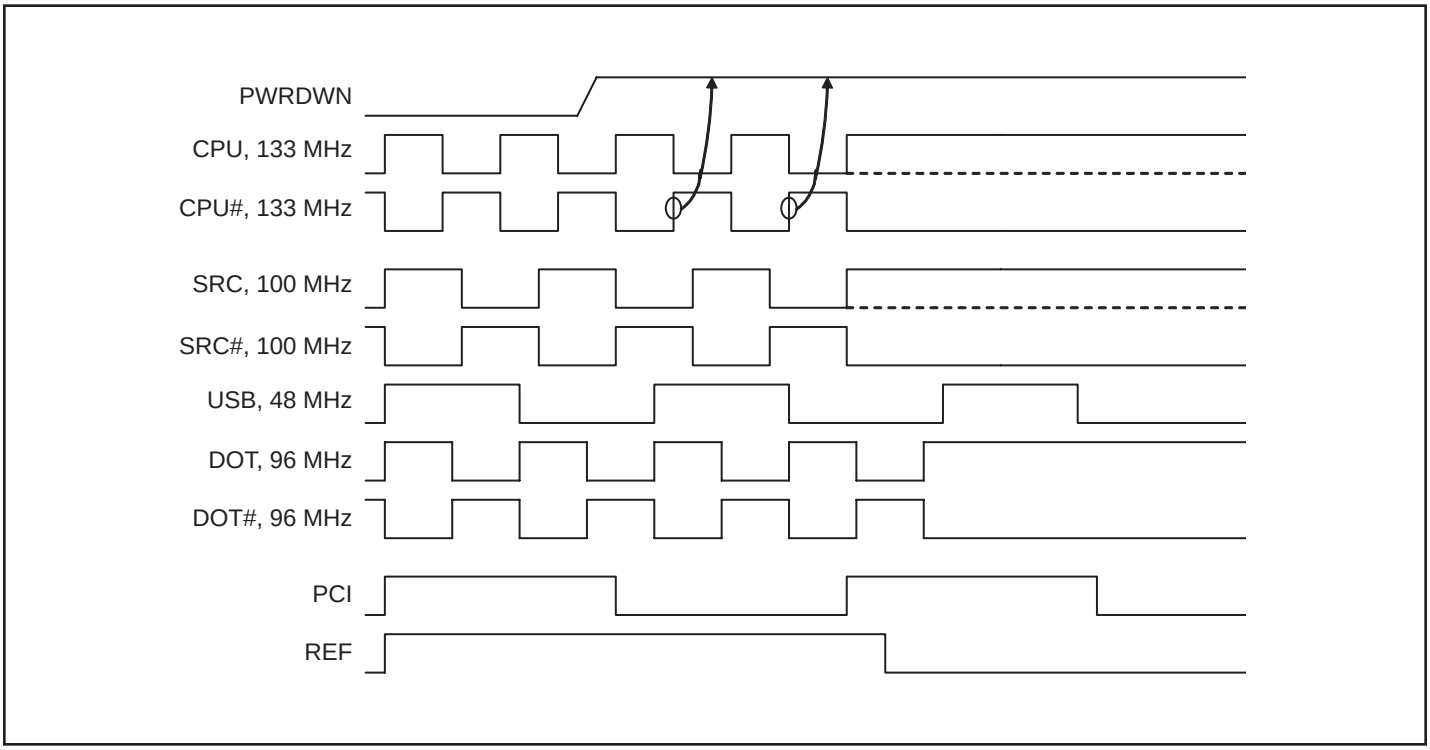


Figure 1, Power down sequence

Power Down (PWRDWN de-assertion)

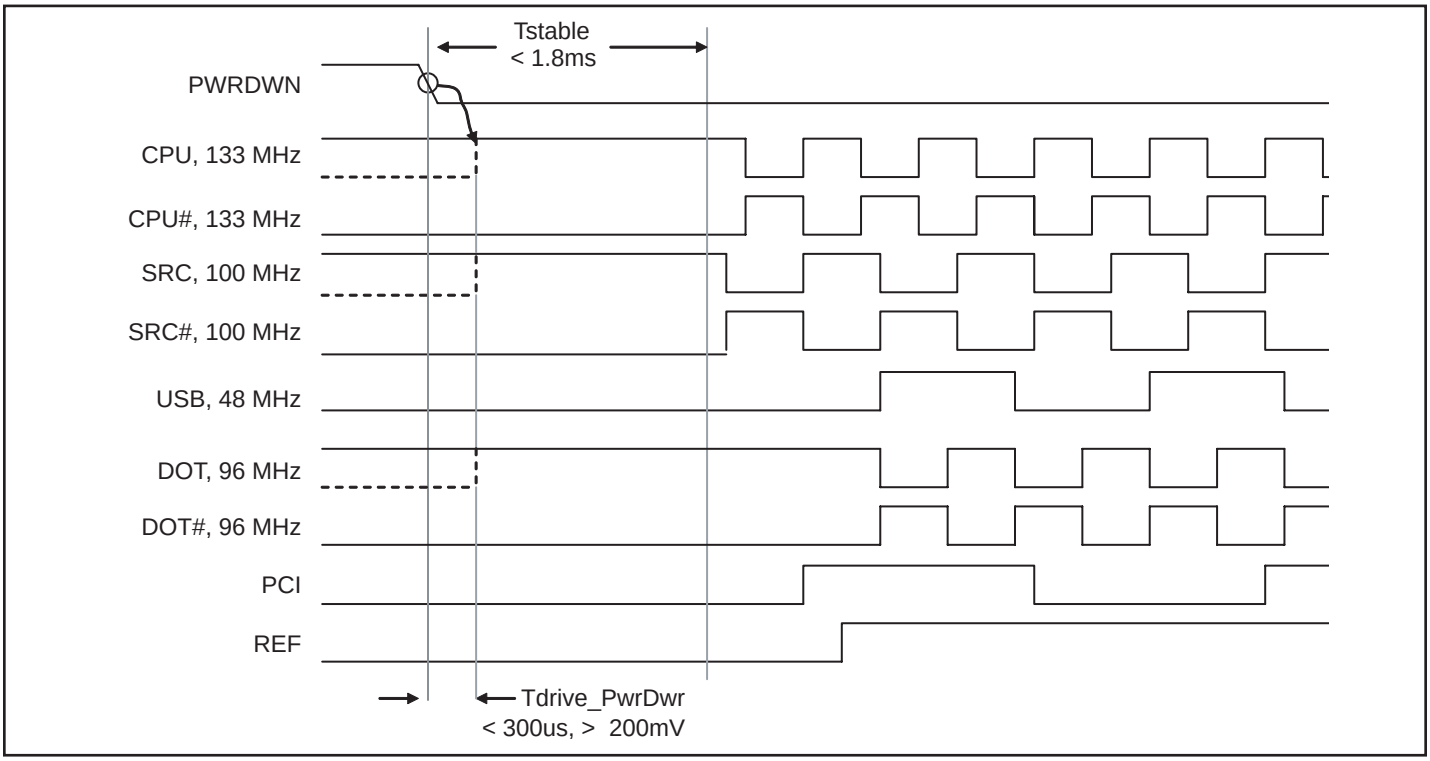


Figure 2, Power down de-assert sequence

Tristate Specifications

Signal	Pwrdwn pin	Pwrdwn Tristate Bit	Stoppable Outputs	Non-stop Outputs
CPU[0:2], SRC[1:7], DOT96	0	X	Running	Running
	1	0	Driven @ Iref x 2	Driven @ Iref x 2
	1	1	Tristate	Tristate

Spread Spectrum Specifications

PI6C410 supports Spread Spectrum clocking and can be enabled and disabled via SMBus control. The maximum Spread Spectrum Modulation is –0.5% down spread with frequency from 30KHz to 33KHz.

SSC ON	Tperiod		SSC OFF	Tperiod		Unit
	Min	Max		Min	Max	
CPU @ 399.000MHz	2.4993	2.5133	CPU @ 400.000MHz	2.4993	2.5008	ns
CPU @ 332.500MHz	2.9991	3.016	CPU @ 333.333MHz	2.9991	3.0009	
CPU @ 266.000MHz	3.7489	3.77	CPU @ 266.666MHz	3.7489	3.7511	
CPU @ 199.500MHz	4.9985	5.0266	CPU @ 200.000MHz	4.9985	5.0015	
CPU @ 166.250MHz	5.9982	6.032	CPU @ 166.666MHz	5.9982	6.0018	
CPU @ 133.000MHz	7.4978	7.54	CPU @ 133.333MHz	7.4978	7.5023	
CPU @ 99.750MHz	9.997	10.0533	CPU @ 100.000MHz	9.997	10.003	
SRC @ 99.750MHz	9.997	10.0533	SRC @ 100.000MHz	9.997	10.003	
PCIF / PCI @ 33.250MHz	29.991	30.1598	PCIF / PCI @ 33.333MHz	29.991	30.009	

Crystal Recommendations

Frequency	Cut	Loading	Load Cap	Drive Max.	Shunt Cap Max.	Motional Cap Max.	Tolerance Max.	Stability Max.	Aging Max.
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Notes:

1. External trim capacitors (Ce) are required by using this formula Ce = 2*CL – (Cs + Ci). Typical Ce = 33pF when Crystal Load = 20pF, Trace capacitance (Cs) = 2.8pF and XTAL pins capacitance = 4.5pF.

Current-mode output buffer characteristics of CPU, SRC, and DOT

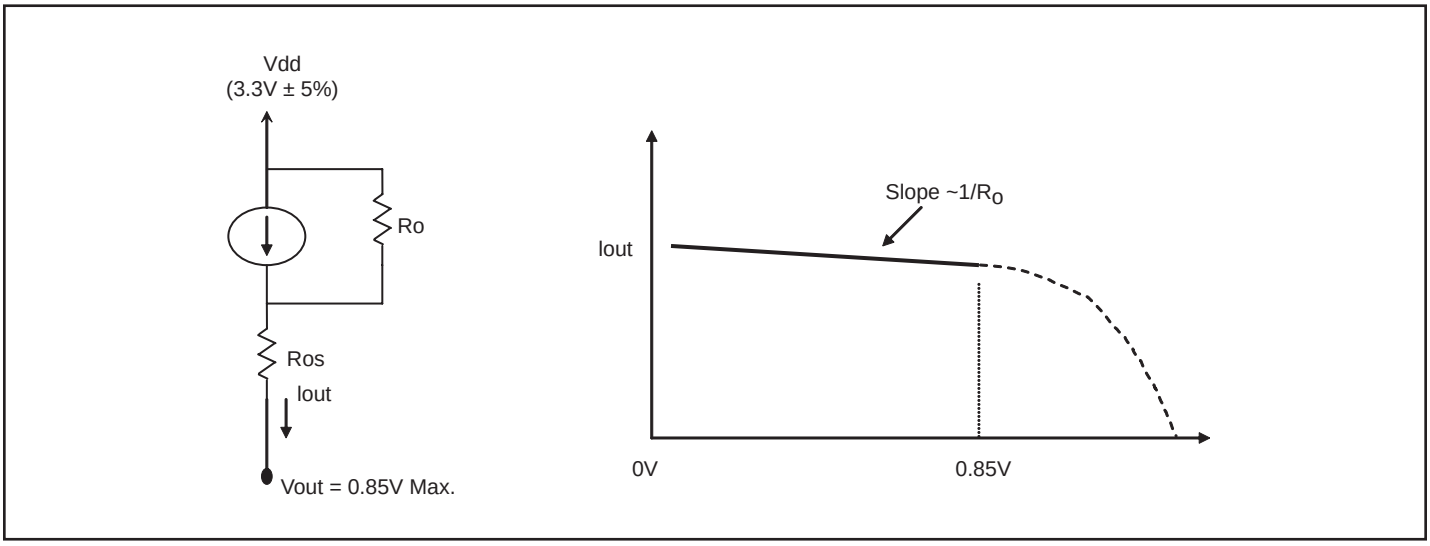


Figure 3. Simplified diagram of a current-mode output buffer

Host Clock Buffer Characteristics

	Minimum	Maximum
R_O	3000 Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	V_{DD} = 3.30 ±5%	Rref = 475Ω 1% Iref = 2.32mA	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Hot Clock Output Current

Board Target Trace/Term Z	Reference R, $I_{REF} = V_{DD}/(3xRr)$	Output Current	V_{OH} @ Z
100 Ω (100 Ω differential ≈ 8% coupling ratio)	R_{REF} = 475Ω 1%, I_{REF} = 2.32mA	I_{OH} = 6 x Iref	0.7V @ 50

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
VDD_A	3.3V Core Supply Voltage	-0.5	4.6	V
VDD	3.3V I/O Supply Voltage	-0.5	4.6	
V_{IH}	Input High Voltage		4.6	
V_{IL}	Input Low Voltage	-0.5		
Ts	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V

Notes:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Configuration test load board termination

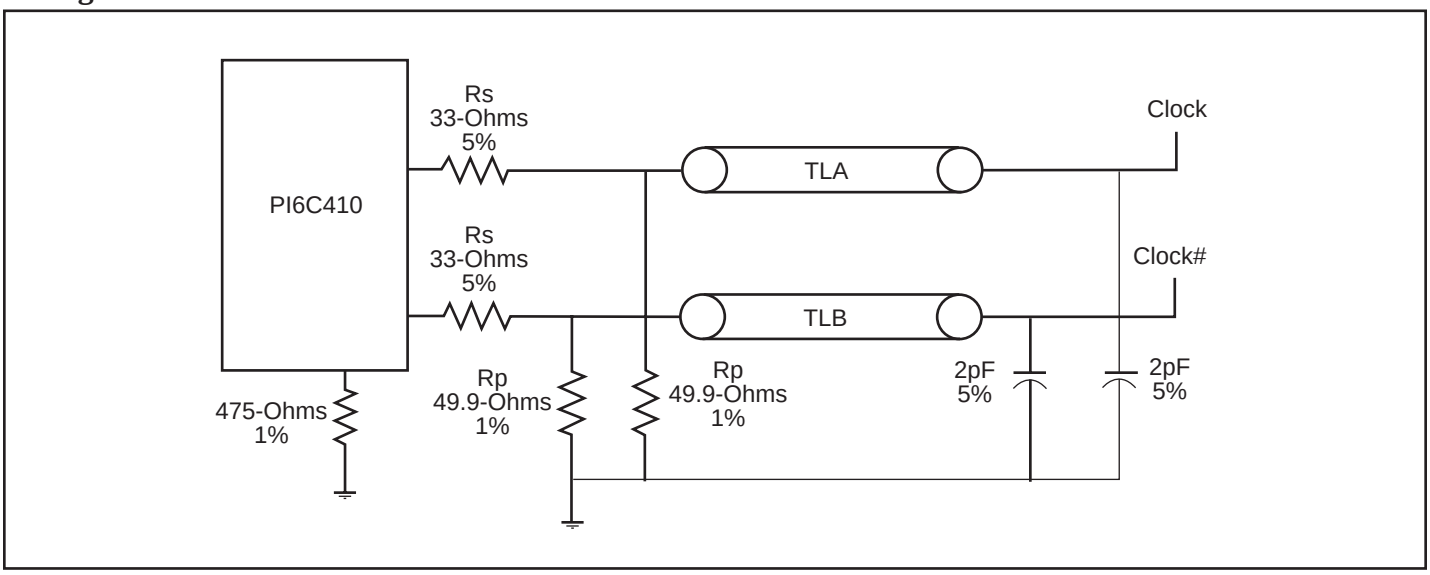


Figure 4. Configuration test load board termination

Notes:
1. Maximum 10" trace length for CPU @ 200 MHz, 16" trace for SRC @ 100 MHz.

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

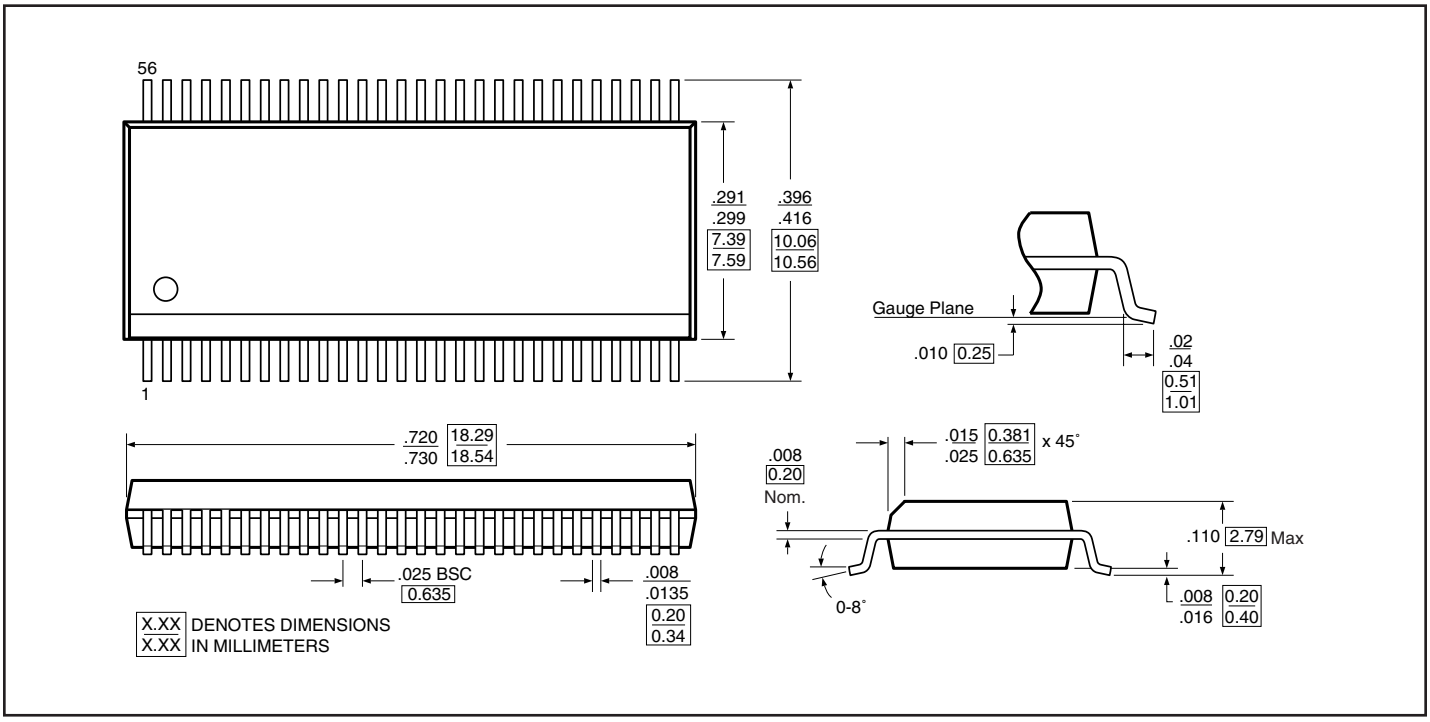
Symbol	Parameters	Condition		Min.	Max.	Units
VDD_A	3.3V Core Supply Voltage			3.135	3.465	V
VDD	3.3V I/O Supply Voltage			3.135	3.465	
V_{IH}	3.3V Input High Voltage	V_{DD}		2.0	V_{DD} + 0.3	
V_{IL}	3.3V Input Low Voltage			V_{SS} – 0.3	0.8	
I_{IK}	Input Leakage Current	0 < V_{IN} < V_{DD}		-5	+5	µA
V_{IH_FS}	3.3V Input High Voltage			0.7	V_{DD} + 0.3	V
V_{IL_FS}	3.3V Input Low Voltage			V_{SS} – 0.3	0.35	
V_{OH}	3.3V Output High Voltage	I_{OH} = -1mA		2.4		
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1mA			0.4	
I_{OH}	Output High Current	CPU, SRC, DOT: I_{OH} = 6 x Iref, Iref = 2.32mA		12.2		mA
					15.6	
		USB	V_{OH} = 1.0V	-29		
			V_{OH} = 3.135V		-23	
		REF, PCI	V_{OH} = 1.0V	-33		
			V_{OH} = 3.135V		-33	
I_{OL}	Output Low Current	USB	V_{OL} = 1.95V	29		
			V_{OL} = 0.4V		27	
		REF, PCI	V_{OL} = 1.95V	30		
			V_{OL} = 0.4V		38	
Cin	Input Pin Capacitance			3	5	pF
Cxtal	Xtal Pin Capacitance			3	5	
Cout	Output Pin Capacitance				6	
Lpin	Pin Inductance				7	nH
I_{DD}	Power Supply Current	V_{DD} = 3.465V, F_{CPU} = 400MHz			500	mA
I_{SS}	Power Down Current	Driven outputs			70	
I_{SS}	Power Down Current	Tristate outputs			12	
Ta	Ambient Temperature			0	70	°C

AC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

Symbol	Outputs	Parameters	Min	Max.	Units	Notes
T_{rise} / T_{fall}	CPU, SRC, DOT	Rise and Fall Time (measured between 0.175V to 0.525V)	175	700	ps	3, 4
T_{rise} / T_{fall}	PCI/PCIF, REF	Rise and Fall Time (measured between 0.4V to 2.4V)	0.5	2.0	ns	6
T_{rise} / T_{fall}	USB	Rise and Fall Time (measured between 0.4V to 2.4V)	1.0	2.0		7
ΔT_{rise} / ΔT_{fall}	CPU, SRC, DOT	Rise and Fall Time Variation		125	ps	3, 4
	CPU, SRC, DOT	Rise/Fall Matching		20	%	
T_{skew}	CPU	CPU – CPU Skew		100	ps	3, 5
T_{skew}	SRC	SRC – SRC Skew		250		
T_{skew}	PCI/PCIF, REF	PCI – PCI Skew / REF - REF Skew (measured at 1.5V)		500		6
T_{jitter}	CPU	Cycle – Cycle Jitter		85		3, 5
T_{jitter}	SRC	Cycle – Cycle Jitter		125		
T_{jitter}	DOT	Cycle – Cycle Jitter		250		
T_{jitter}	PCI/PCIF	Cycle – Cycle Jitter (measured at 1.5V)		500		6
T_{jitter}	USB	Cycle – Cycle Jitter (measured at 1.5V)		350		7
T_{jitter}	REF	Cycle – Cycle Jitter (measured at 1.5V)		1000		6
V_{HIGH}	CPU, SRC, DOT	Voltage High including overshoot	660	1150	mV	3, 4
V_{LOW}	CPU, SRC, DOT	Voltage Low including undershoot	-300			
Vcross	CPU, SRC, DOT	Absolute crossing poing voltages	250	550		
ΔVcross	CPU, SRC, DOT	Total Variation of Vcross over all edges		140		
T_{DC}	CPU, SRC, DOT	Duty Cycle	45	55	%	3, 5
T_{DC}	REF, USB, PCI/PCIF	Duty Cycle (measured at 1.5V)	45	55	%	6, 7
T_{stable}		All clock stabilization from power-up		<1.8	ms	Fig 2
T_{drive} Pwrdwn		Differential output enable after PwrDwn de-assertion		300	µs	
T_{rise} / T_{fall} Pwrdwn		PwrDwn rise and fall time		5.0	ns	

Notes:
3. Test configuration is Rs = 33.2 Ohms, Rp = 49.9 Ohms, and 2pF.
4. Measurement taken from Single Ended waveform.
5. Measurement taken from Differential waveform.
6. PCI, PCIF, and REF outputs minimum loading = 10pF, Maximum loading = 30pF.
7. USB output minimum loading = 10pF, Maximum loading = 20pF.

Packaging Mechcanical: 56-Pin SSOP (V)



Ordering Information:

Ordering Code	Packaging Code	Package Type
PI6C410V	V	56-Pin, 300mil wide, 0.64mm pitch SSOP
PI6C410VE	V	Pb-free & Green 56-Pin, 300mil wide, 0.64mm pitch SSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/