PLL Clock Driver for 2.5V DDR-SDRAM Memory

Product Features

- PLL clock distribution optimized for Double Data Rate SDRAM applications.
- Distributes one differential clock input pair to ten differential clock output pairs.
- Inputs (CLK,$\overline{\text{CLK}}$) and (FBIN,$\overline{\text{FBIN}}$): SSTL_2
- Input $\overline{\text{PWRDWN}}$: LVCMOS
- Outputs (Yx, $\overline{\text{Yx}}$), (FBOUT, $\overline{\text{FBOUT}}$): SSTL_2
- External feedback pins (FBIN,$\overline{\text{FBIN}}$) are used to synchronize the outputs to the clock input.
- Operates at AV_{DD} = 2.5V for core circuit and internal PLL, and V_{DDQ} = 2.5V for differential output drivers
- Package: Plastic 48-pin TSSOP (A)

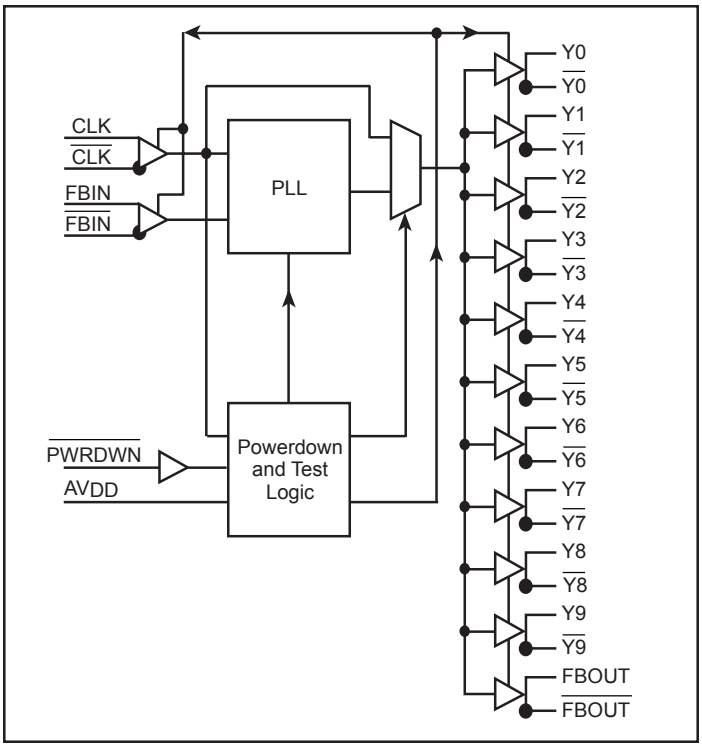
Product Description

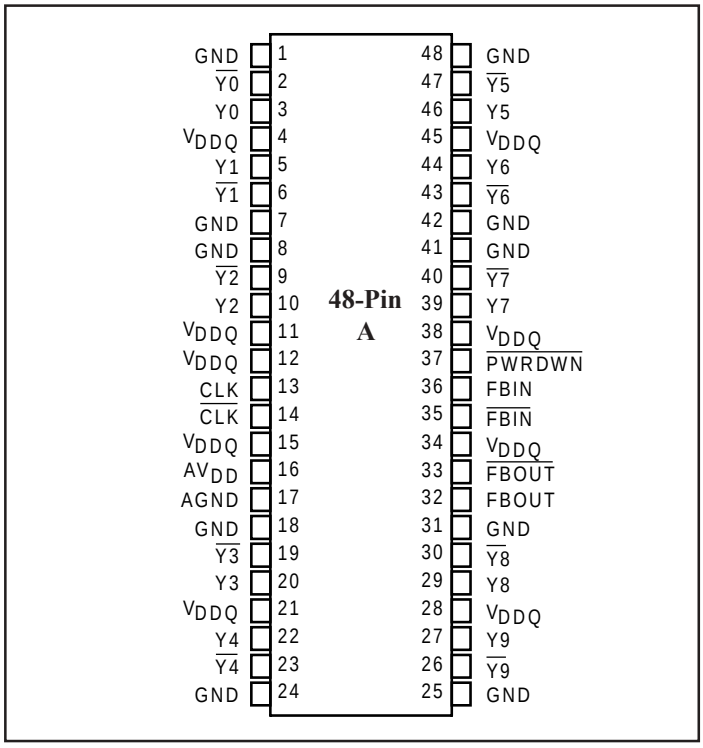
PI6CV857 PLL clock device is developed for registered DDR DIMM applications This PLL Clock Buffer is designed for 2.5 V_{DDQ} and 2.5V AV_{DD} operation and differential data input and output levels. Package options include plastic Thin Shrink Small-Outline Package (TSSOP).The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{\text{Y}}$[0:9]) and one differential pair feedback clock outputs (FBOUT,$\overline{\text{FBOUT}}$) . The clock outputs are controlled by the input clocks (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN,$\overline{\text{FBIN}}$), the 2.5V LVCMOS input ($\overline{\text{PWRDWN}}$) and the Analog Power input (AV_{DD}). When input $\overline{\text{PWRDWN}}$ is low while power is applied, the input receivers are disabled, the PLL is turned off and the differential clock outputs are 3-stated. When the AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes.

When the input frequency falls below a suggested detection frequency that is below the operating frequency of the PLL, the device will enter a low power mode. An input frequency detection circuit will detect the low frequency condition and perform the same low power features as when the $\overline{\text{PWRDWN}}$ input is low.

The PLL in the PI6CV857 clock driver uses input clocks (CLK, $\overline{\text{CLK}}$) and feedback clocks ($\overline{\text{FBIN}}$,FBIN) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], $\overline{\text{Y}}$[0:9]). PI6CV857 is also able to track Spread Spectrum Clocking for reduced EMI.

Block Diagram/Pin Configuration





Pinout Table

Pin Name	Pin No.	I/O Type	Description
CLK $\overline{CLK}$	13 14	I	Reference Clock input
Yx	3,5,10,20,22,27,29,39,44,46	O	Clock outputs.
$\overline{Yx}$	2,6,9,19,23,26,30,40,43,47		Complement Clock outputs.
FBOUT $\overline{FBOUT}$	32 33		Feedback output, and Complement Feedback Output
FBIN $\overline{FBIN}$	36 35	I	Feedback output, and Complement Feedback Output
$\overline{PWRDWN}$	37		Power down and output disable for all Yx and $\overline{Yx}$ outputs. When $\overline{PWRDWN}$ = 0, the part is powered down and the differential clock outputs are disabled to a 3-state. When $\overline{PWRDWN}$ = 1, all differential clock outputs are enabled and run at the same frequency as CLK.
V_{DDQ}	4,11,12,15,21,28,34,38,45	Power	Power Supply for I/O.
AV_{DD}	16		Analog /core power supply. AV_{DD} can be used to bypass the PLL for testing purposes. When AV_{DD} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	17	Ground	Analog/core ground. Provides the ground reference for the analog/core circuitry
GND	1,7,8,18,24,25,31,41,42,48		Ground

Function Table

Inputs				Outputs				PLL State
AV_{DD}	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
X	L	L	H	Z	Z	Z	Z	off
X	L	H	L	Z	Z	Z	Z	off
2.5V(nom)	H	L	H	L	H	L	H	on
2.5V(nom)	H	H	L	H	L	H	L	on
2.5V(nom)	X	<20 MHz (1)		Z	Z	Z	Z	off

Notes: For testing and power saving purposes, PI6CV857 will power down if the frequency of the reference inputs CLK, $\overline{CLK}$ is well below the operating frequency range. The maximum power down clock frequency is below 20 MHz. For example, PI6CV857 will be powered down when the CLK,$\overline{CLK}$ stop running.

Z = High impedance
X = Don't care

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_{DDQ}, AV_{DD}	I/O supply voltage range and analog/core supply voltage range	– 0.5	3.6	V
V_I	Input voltage range	– 0.5	V_{DDQ}+0.5	
V_O	Output voltage range	– 0.5		
Tstg	Storage temperature	– 65	150	°C

Note: Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Timing Requirements (Over recommended operating free-air temperature)

Symbol	Description	AV_{DD}, V_{DDQ} = 2.5V ±0.2V		Units
		Min.	Max.	
f_{CK}	Operating clock frequency(1,2)	60	170	MHz
	Application clock frequency(3)	95	170	
t_{DC}	Input clock duty cycle	40	60	%
t_{STAB}	PLL stabilization time after powerup		100	µs

Notes:
1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which the clock is not required to meet the other timing parameters. (Used for low-speed debug).
3. Application clock frequency indicates a range over which the PLL meets all of the timing parameters.

DC Specifications
Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units
AV_{DD}	Analog/core supply voltage	2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	
V_{IL}	Low-level input voltage for $\overline{PWRDWN}$ pin	–0.3		0.7	
V_{IH}	High-level input voltage for $\overline{PWRDWN}$ pin	1.7		V_{DDQ} +0.3	
V_{OH}	High-level output voltage	1.8		V_{DDQ}	
V_{OL}	Low-level output voltage	0		0.5	
V_{IX}	Input differential-pair crossing voltage	(V_{DDQ}/2) –0.2		(V_{DDQ}/2) +0.2	
V_{OX}	Output differential-pair crossing voltage at the DRAM clock input	(V_{DDQ}/2) –0.2		(V_{DDQ}/2) +0.2	
V_{IN}	Input voltage level	–0.3		V_{DDQ} +0.3	
V_{ID}	Input differential voltage between CK and $\overline{CK}$	0.36		V_{DDQ} +0.6	
V_{OD}	Output differential voltage between Y[n] and $\overline{Y[n]}$ and FBOUT and $\overline{FBOUT}$	0.70		V_{DDQ} +0.6	
T_A	Operating free air temperature	0		70	°C

Electrical Characteristics

Parameter		Test Conditions	AV_{DD}, V_{DDQ}	Min.	Typ.	Max.	Units
V_{IK}	All inputs	I_I = –18mA	2.3V			–1.2	V
V_{OH}	High output voltage	I_{OH} = –100µA	2.3V to 2.7V	V_{DDQ} –0.1			
		I_{OH} = –14mA	2.3V	1.7			
V_{OL}	Low output voltage	I_{OL} = 100µA	2.3V to 2.7V			0.1	
		I_{OL} = 14mA	2.3V			0.6	
I_I	CK, FBIN	$V_I = V_{DDQ}$ or GND	2.7V			±10	µA
	$\overline{PWRDWN}$	$V_I = V_{DDQ}$ or GND					
I_{DDQ}	Dynamic supply current of V_{DDQ}	V_{DD} = 2.7V (1)				300	mA
	Static supply current	CK & $\overline{CK}$ <20 MHz or $\overline{PWRDWN}$ = Low (2)				100	µA
I_{ADD}	Dynamic supply current of AV_{DD}	V_{DD} = 2.7V (1)				12	mA
	Static supply current	CK & $\overline{CK}$ <20 MHz or $\overline{PWRDWN}$ = Low (2)				100	µA
C_I	CK and $\overline{CK}$	$V_I = V_{DD}$ or GND	2.5V	2.0		3.0	pF
	FBIN and $\overline{FBIN}$						

Notes:
1. Driving 9 or 18 DDR SDRAM memory chips with 120-ohm termination resistor for each clock output pair at 134 MHz.
2. The maximum power down clock frequency is below 20 MHz.

AC Specifications

Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Description	Diagram	AV_{DD}, V_{DDQ} = 2.5V ±0.2V			Units
			Min.	Nom.	Max	
tjit(cc)	Cycle-to-cycle jitter	see Figure 3	–75		75	ps
t(θ)	Static phase offset(1)	see Figure 4	–50	0	50	
tsk(o)	Output clock skew	see Figure 5			100	
tjit(per)	Period jitter	see Figure 6	–75		75	
tjit(hper)	Half-period jitter	see Figure 7	–100		100	
tsl(i)	Input clock slew rate(2)	see Figure 8	1.0		2.0	V/ns
tsl(o)	Output clock slew rate(2)	see Figure 8	1.0		2.0	
The PLL on PI6CV857 meets the above parameters while supporting SSC synthesizers with the following parameters(3).						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
	PLL loop bandwidth			2		MHz
	Phase angle				–0.031	degrees

Notes:

1. Static Phase offset does not include Jitter.
2. The slew rate is determined from the IBIS model and not from the test load.
3. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

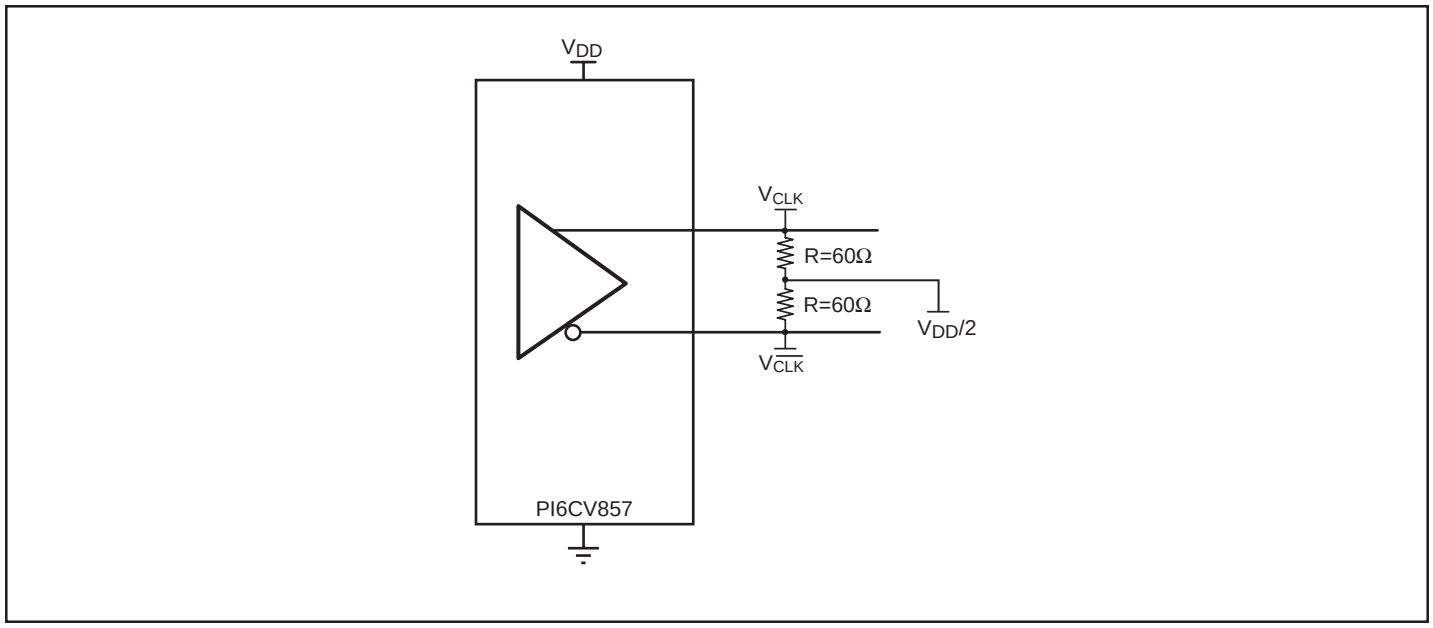


Figure 1. Output Load

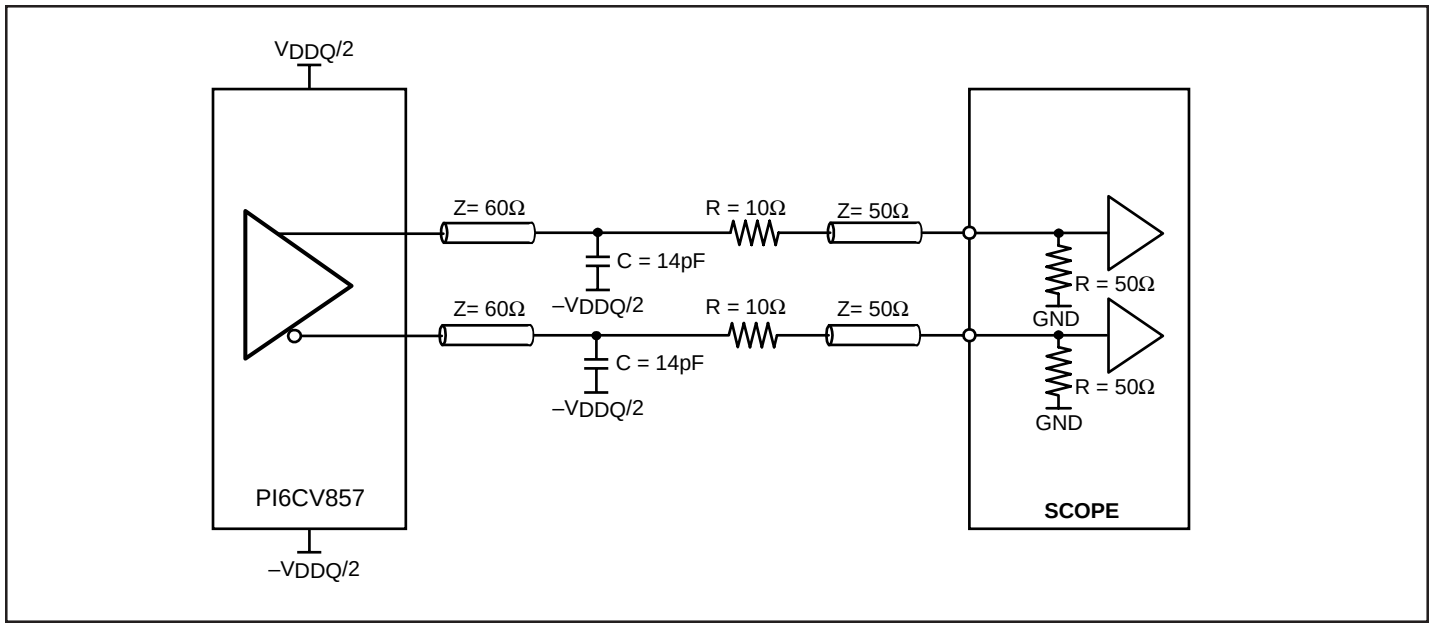


Figure 2. Output Load Test Circuit

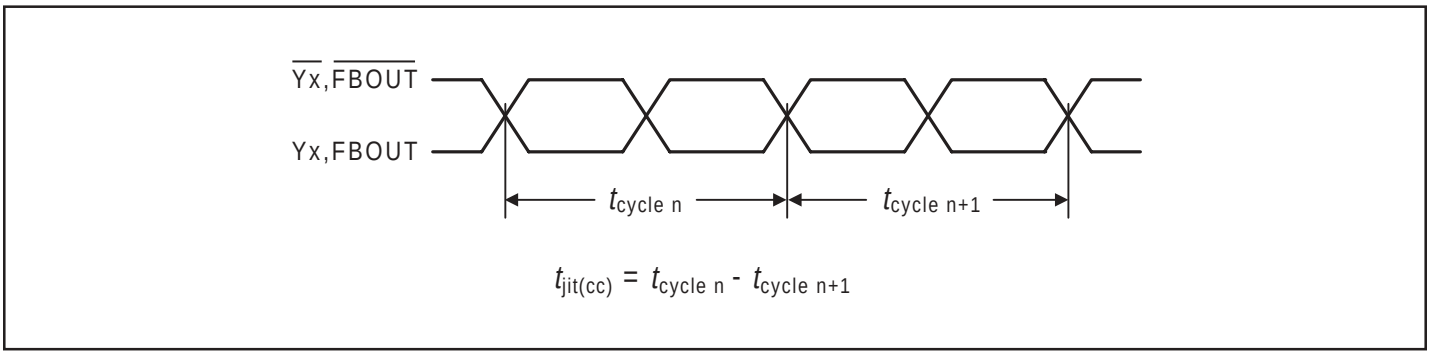


Figure 3. Cycle-to-Cycle Jitter

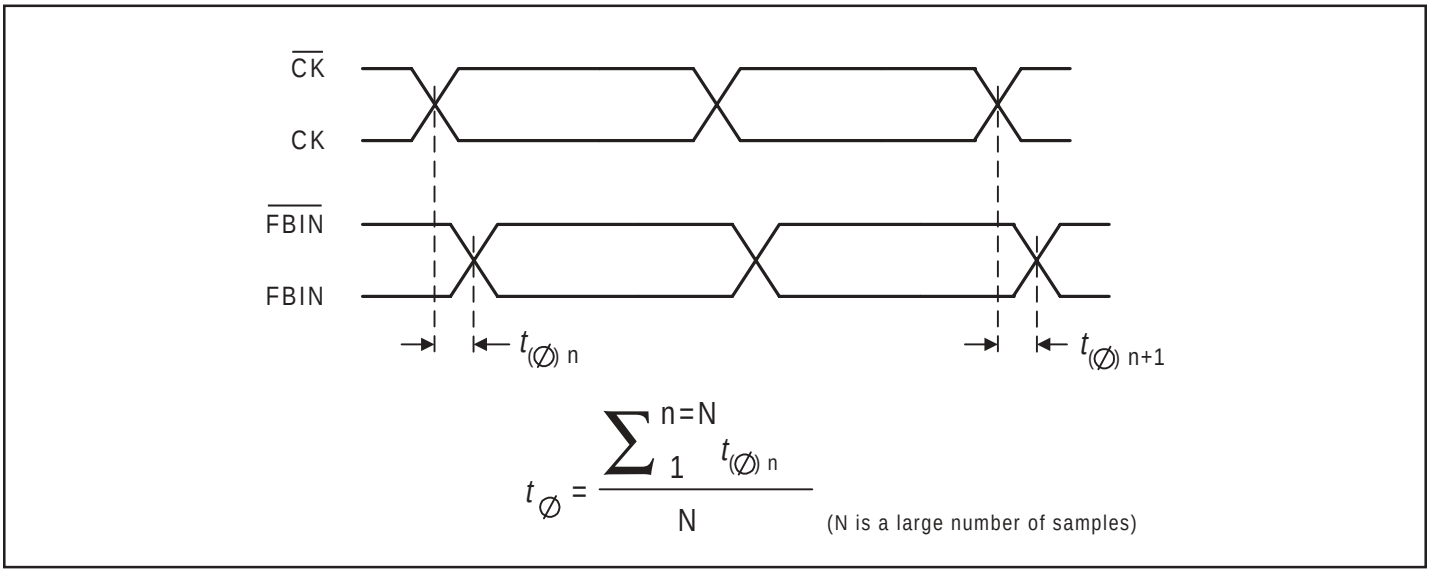


Figure 4. Static Phase Offset

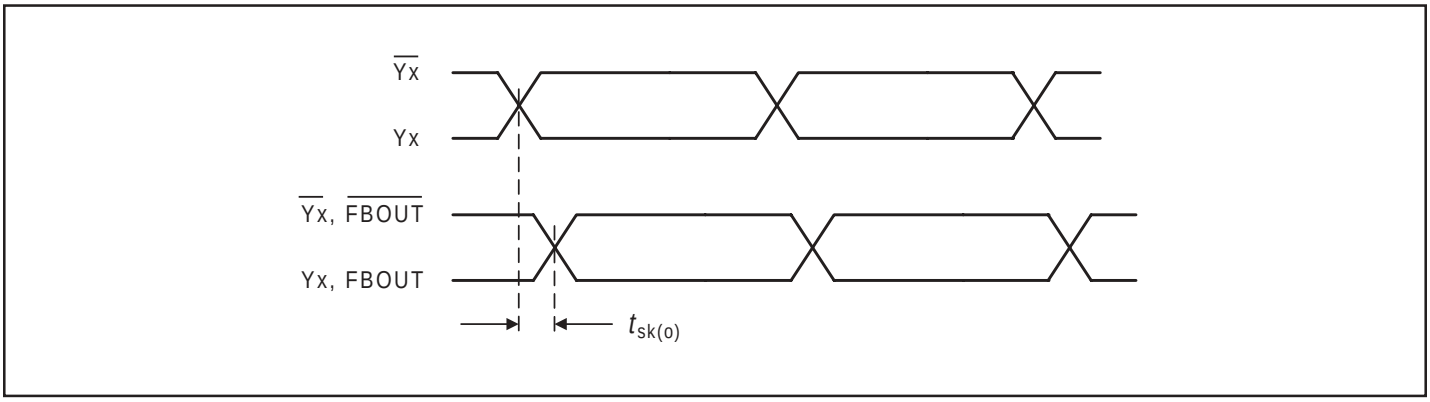


Figure 5. Output Skew

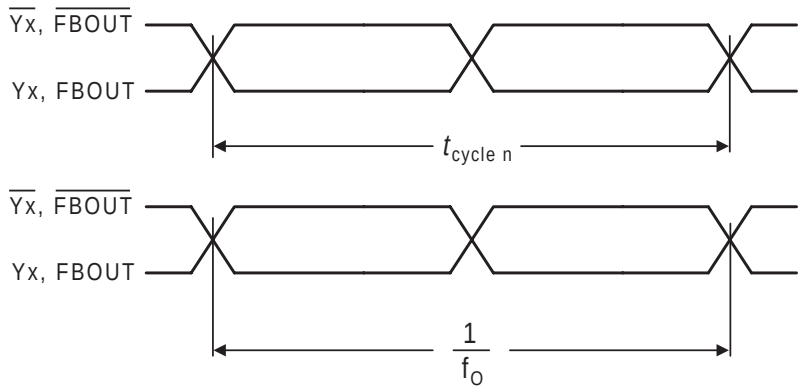


Figure 6. Period Jitter

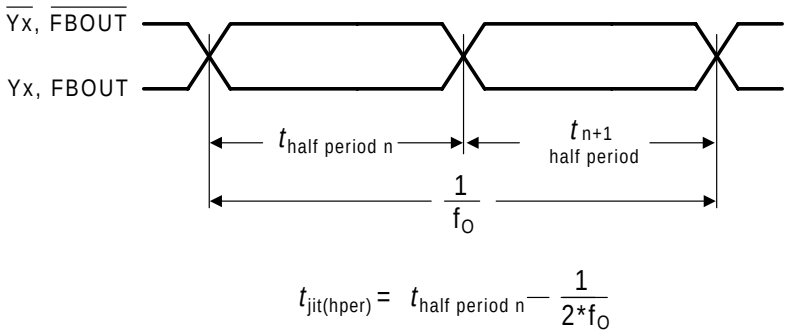


Figure 7. Half-Period Jitter

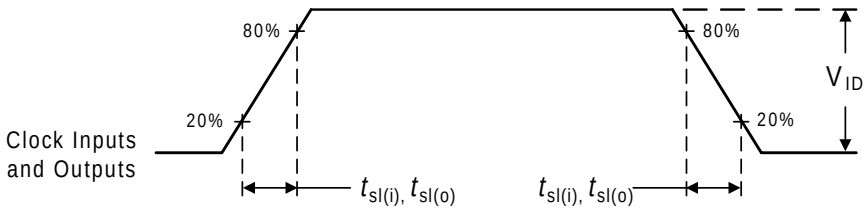
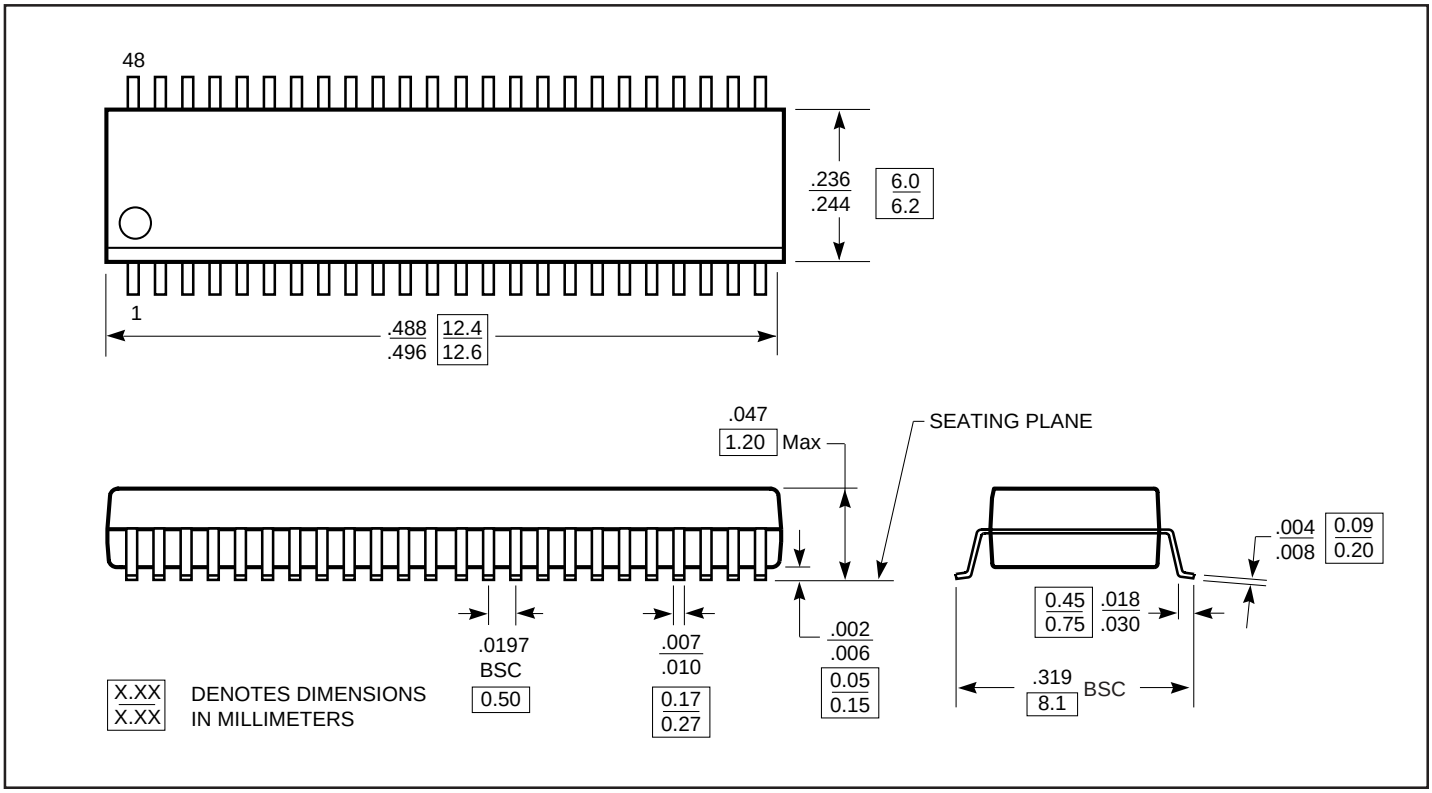


Figure 8. Input and Output Slew Rates

Packaging Mechanical: 48-Pin TSSOP (A)



Ordering Information

Ordering Code	Package Name	Package Type
PI6CV857A	A48	48-pin, 240-mil wide TSSOP