DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
NP161N04TUG

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP161N04TUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP161N04TUG-E1-AY Note	Pure Sn (Tin)	Tape 800 p/reel	TO-263-7pin (MP-25ZT) typ. 1.5 g
NP161N04TUG-E2-AY Note			

Note Pb-free (This product does not contain Pb in the external electrode).

FEATURES

- Super low on-state resistance
  $R_{DS(on)}$ = 1.35 mΩ TYP. / 1.8 mΩ MAX. (V_{GS} = 10 V, I_D = 80 A)
- High Current Rating
  $I_{D(DC)}$ = ±160 A

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±160	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±640	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	250	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current Note2	I_{AR}	70	A
Repetitive Avalanche Energy Note2	E_{AR}	650	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. T_{ch} = 150°C, V_{DD} = 25 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.6	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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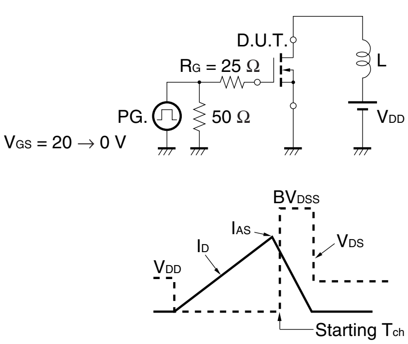
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

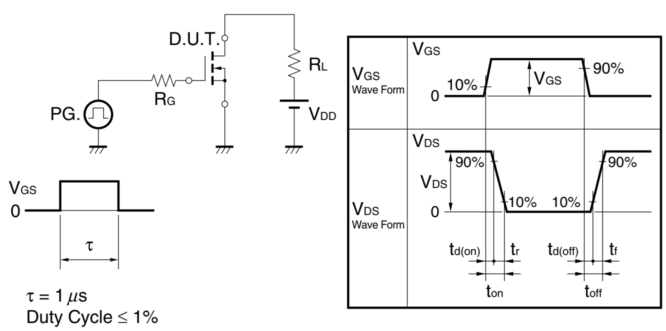
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 5 V, I_D = 40 A	35	88		S
Drain to Source On-state Resistance Note	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 80 A		1.35	1.8	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V,		13500	20250	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		1200	1800	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		750	1350	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20 V, I_D = 80 A,		50	110	ns
Rise Time	t_r	V_{GS} = 10 V,		40	100	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		110	220	ns
Fall Time	t_f			20	40	ns
Total Gate Charge	Q_G	V_{DD} = 32 V,		230	345	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		50		nC
Gate to Drain Charge	Q_{GD}	I_D = 160 A		75		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 160 A, V_{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 160 A, V_{GS} = 0 V,		60		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		100		nC

Note Pulsed test

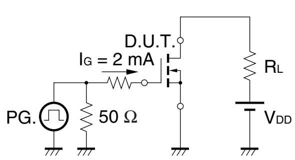
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

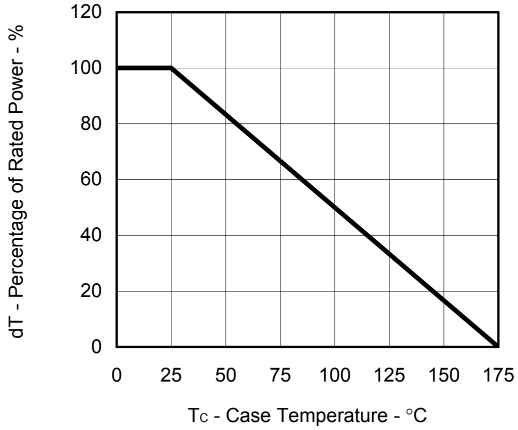


TEST CIRCUIT 3 GATE CHARGE

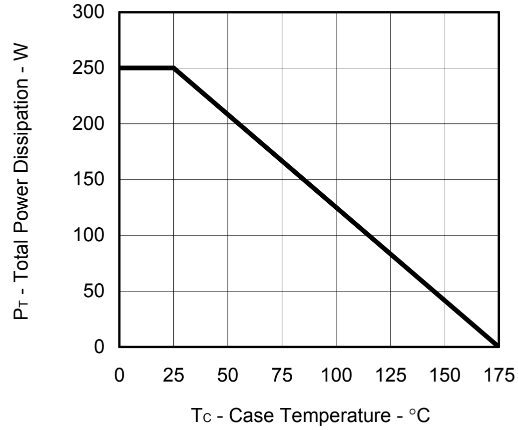


TYPICAL CHARACTERISTICS (T_A = 25°C)

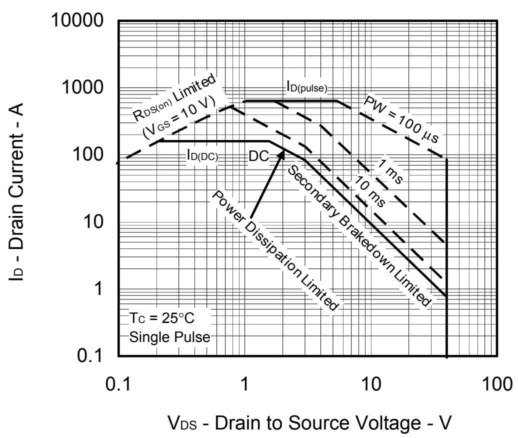
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



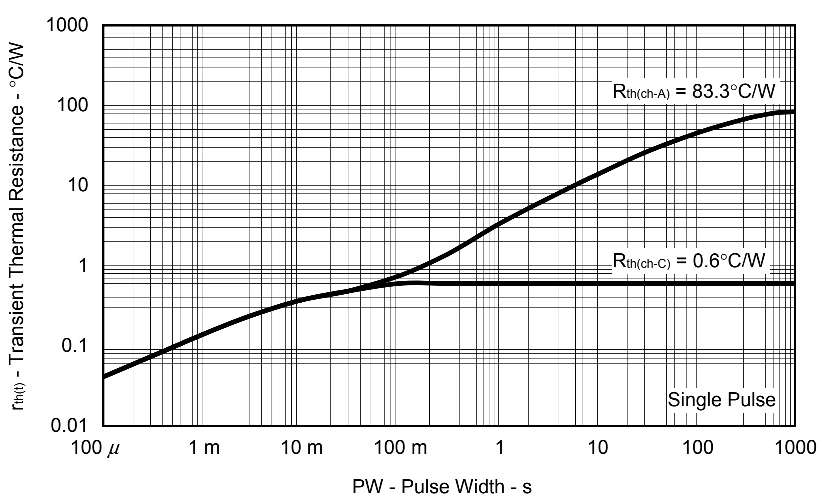
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



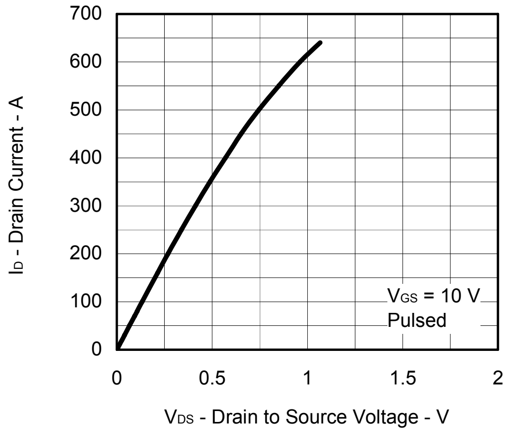
FORWARD BIAS SAFE OPERATING AREA



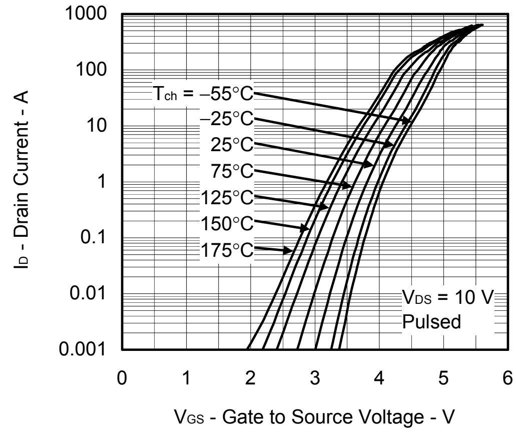
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



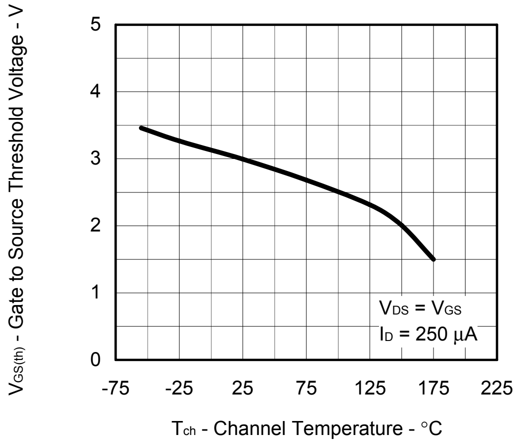
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



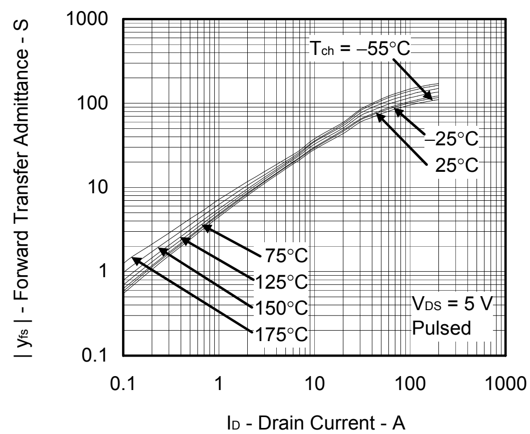
FORWARD TRANSFER CHARACTERISTICS



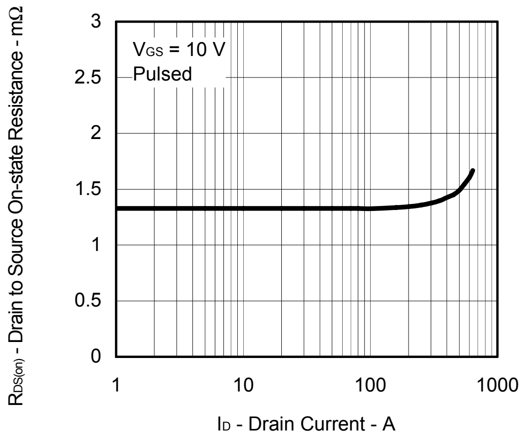
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



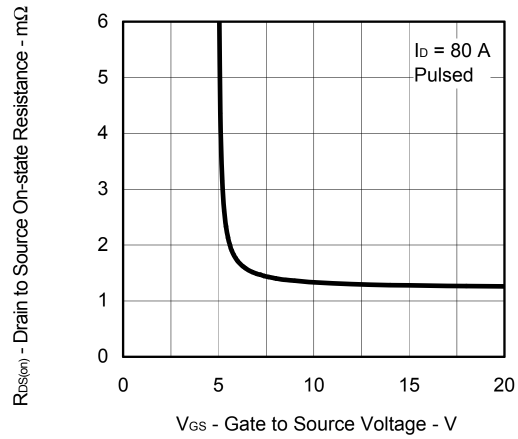
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



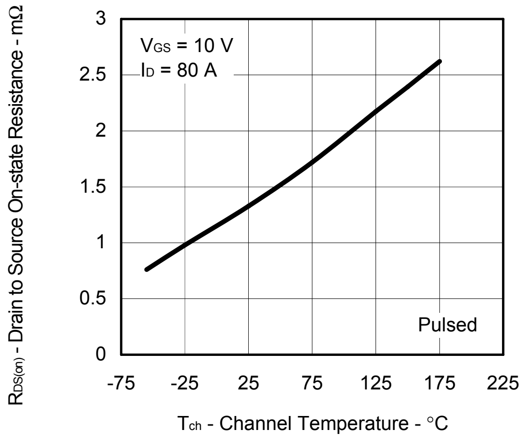
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



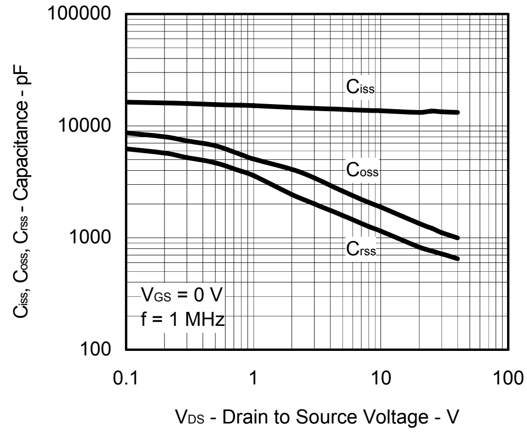
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



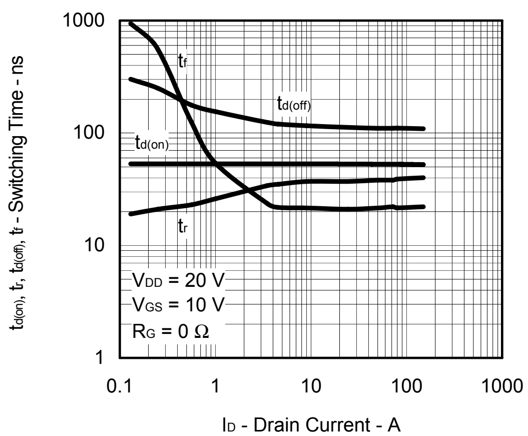
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



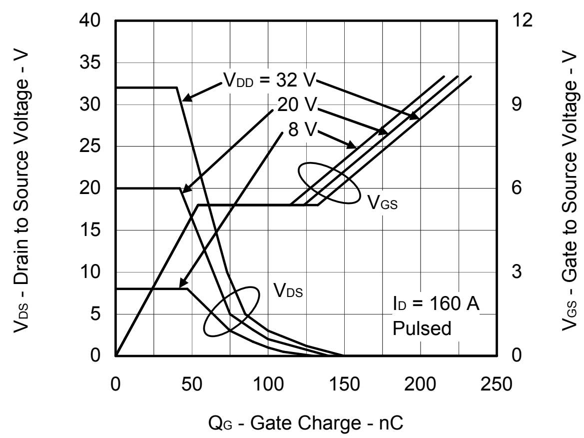
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



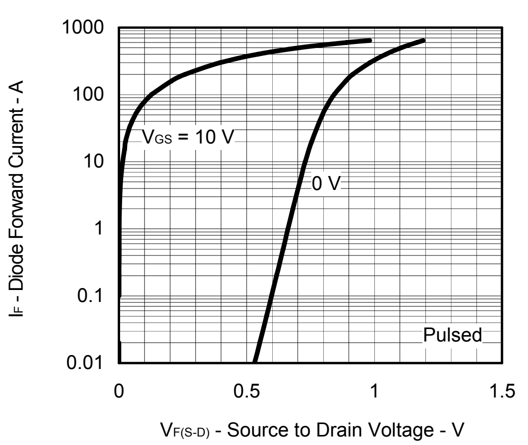
SWITCHING CHARACTERISTICS



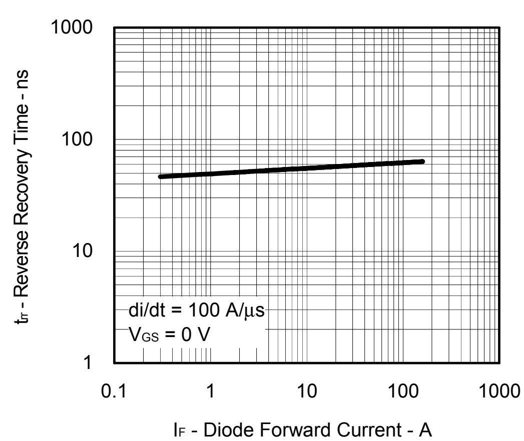
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE
FORWARD VOLTAGE

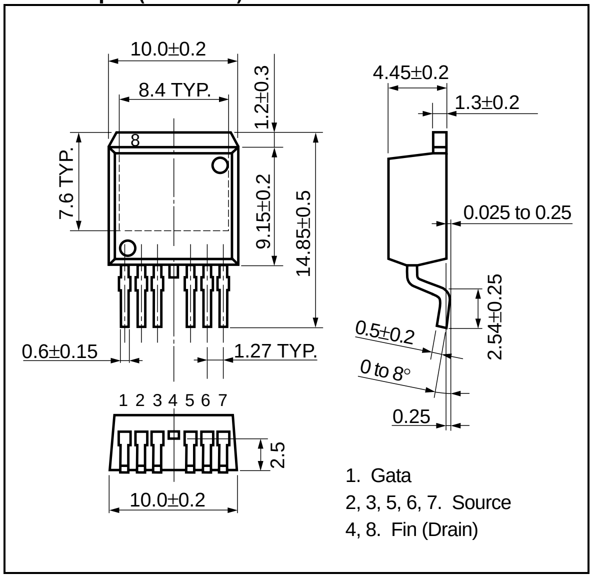


REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT

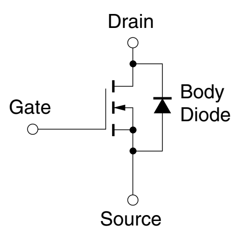


PACKAGE DRAWING (Unit: mm)

TO-263-7pin (MP-25ZT)



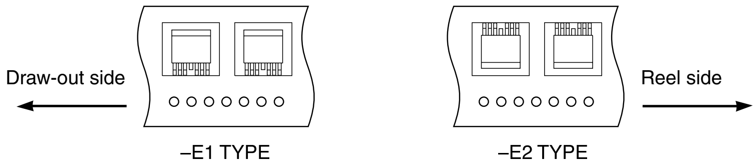
EQUIVALENT CIRCUIT



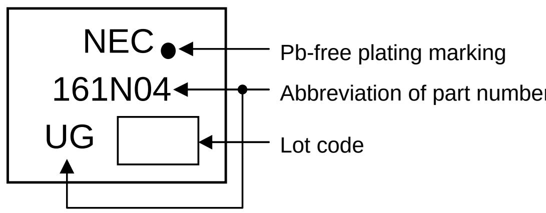
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP161N04TUG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution   Do not use different soldering methods together (except for partial heating).