

# International **IOR** Rectifier

## FULL-FEATURED POWER MODULE FOR HIGH VOLTAGE DIRECT DRIVE OF 3-PHASE BRUSHLESS DC MOTOR F-43 / MP3-43L Packages

### 25A Push-Pull 3-Phase Brushless DC Motor Controller / Driver Module in a Power Flatpack

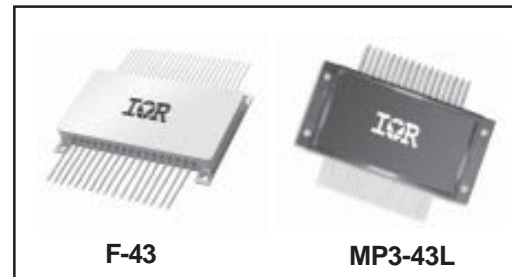
#### Description:

The OM9369 is one of a series of versatile, integrated three-phase brushless DC motor controller/driver subsystems housed in a 43 pin power flatpack. The OM9369 is best used as a two quadrant speed controller for controlling/driving fans, pumps, and motors in applications which require small size. Typical size brushless DC motors that the OM9369 can effectively control range from fractional HP up to several HP. The OM9369 is ideal for use on DC distribution buses up to and including 270Vdc. Many integral control features provide the user much flexibility in adapting the OM9369 to specific system requirements.

The small size of the complete subsystem is ideal for aerospace, military, and high-end industrial applications. Two package types provide a broad range of cost and screening options to fit any application.

PD-95806

**OM9369**  
**OM9369SF**  
**OM9369SP**



#### Features:

- Fully Integrated 3-Phase Brushless DC Motor Control Subsystem includes Power Stage, Non-Isolated Driver Stage and Controller Stage
- Rugged IGBT Power Output Stage with Soft Recovery Diode
- 25A Average Phase Current with 300V Maximum Bus Voltage
- Internal Precision Current Sense Resistor (6W Max. Dissipation)
- Speed and Direction Control of Motor
- Brake Input for Dynamic Braking of Motor
- Overvoltage/Coast Input for Shutdown of All Power Switches
- Soft Start for Safe Motor Starting
- Unique Hermetic or Plastic Ring Frame Power Flatpacks  
Hermetic (3.10" X 2.10" X 0.385")  
Plastic Ring Frame (4.13" X 2.00" X 0.49")

#### Applications:

- Fans and Pumps
- Hoists
- Actuator Systems

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Units
Motor Supply Voltage	$V_m$	300	V
Peak Motor Supply Voltage	$V_{m\text{pk}}$	500	
Average Phase Output Current	$I_o$	25	A*
Peak Phase Output Current	$I_{om}$	50	A <sub>peak</sub> **
Control Supply Voltage	$V_{cc}$	18	V
Logic Input Voltage (Note 1)		-0.3 to 8.0	
Reference Source Current		-30	mA
Error Amplifier Input Voltage Range	( EA1+ / EA1- )	-0.3 to 10	V
Error Amplifier Output Current		±8	mA
Spare Amplifier Input Voltage	( EA2+ / EA2- )	-0.3 to 10	V
Spare Amplifier Output Current		±8	mA
Current Sense Amplifier Input Voltage	( ISH / ISL )	-0.3 to 6.0	V
Current Sense Amplifier Output Current		±10	mA
Tachometer Output Current			
PWM Input Voltage		-0.3 to 6.0	V
Operating Junction Temperature		-55 to 150	°C
Storage Temperature Range		-65 to 150	
Lead Soldering Temperature, 10s maximum, 0.125" from case		300	
Package Isolation Voltage		600	V <sub>rms</sub>
Power Switch Junction-to-Case Thermal Resistance	$R_{\theta JC}$	0.48	°C/W

\*  $T_{CASE} = 25^{\circ}\text{C}$ \*\*  $T_{CASE} = 25^{\circ}\text{C}$ , Maximum pulse width = 10 mS**Recommended Operating Conditions (  $T_{case} = 25^{\circ}\text{C}$  )**

Parameter	Symbol	Value	Units
Motor Power Supply Voltage	$V_m$	270	V
Average Phase Output Current With Internal Current Sense Resistor ( Note2 ) Each Power Switch	$I_o$	25	A
Control Supply Voltage	$V_{cc}$	15±10%	V
Logic Low Input Voltage (maximum)	$V_{il}$	0.8	
Logic High Input Voltage (minimum)	$V_{ih}$	2.0	

Note 1: Logic Inputs: Direction, Hall Inputs (H1--- H3) Overvoltage - Coast, Speed, and Quad Select.

Note 2: The internal 5mΩ current sense resistor is limited to 6 Wdc power dissipation. Other values are available.  
Please contact International Rectifier for more information.

**Electrical Characteristics**

Parameter	Symbol	Test Conditions (Note 1)	Min.	Typ.	Max.	Units
<b>Power Output Section</b>						
IGBT Leakage Current	$I_{ces}$	$V_{ce} = 600V_{dc}, V_{ge} = 0V$	-	-	300	$\mu A$
IGBT c-e Saturation Voltage	$V_{ce(sat)}$	$I_c = 50A_{dc}, V_{ge} = 15V$	-	-	3.2	V
Diode Leakage Current	$I_r$	$V_r = 600V_{dc}$	-	-	100	$\mu A$
Diode Forward Voltage	$V_f$	$I_f = 37A$	-	-	1.7	V
Diode Reverse Recovery Time	$t_{rr}$	$I_o = 1.0A, di/dt = -100A/\mu sec, V_r = 30V$	-	-	50	nS
<b>Control Section</b>						
Control Supply Current	$I_{cc}$	$V_{cc}$ over operating range	-	-	100	mA
Control Turn-On Threshold	$V_{cc(+)}$	$T_c$ over operating range	9.45	-	-	V
Driver Turn-On Threshold			13	-	-	
<b>Reference Section</b>						
Output Voltage	$V_{ref}$	$T_c$ over operating range	4.9	5.0	5.1	V
Output Voltage			4.7	5.0	5.3	
Output Current	$I_o$		-	-	30	mA
Load Regulation		$I_{load} = 0mA$ to $-20mA$	-40	-5.0	-	mV
Short Circuit Current	$I_{sc}$	$T_c$ over operating range	50	100	150	mA
<b>Error / Spare Amplifier Sections</b>						
EA1 / EA2 Input Offset Current	$I_{os}$	$V(\text{pin } 2) = V(\text{pin } 4) = 0V,$ $V(\text{pin } 3) = V(\text{pin } 6) = 0V$	-30	-3.0	0	nA
EA1 / EA2 Input Bias Current	$I_{in}$	$V(\text{pin } 2) = V(\text{pin } 4) = 0V,$ $V(\text{pin } 3) = V(\text{pin } 6) = 0V$	-50	-45	0	
Input Offset Voltage	$V_{os}$	$0V < V_{common-mode} < 3.0V$	-	-	7.0	mV
Amplifier Output Voltage Range	-		0	-	6.0	V
<b>PWM Comparator Section</b>						
PWM Input Current	$I_{in}$	$V(\text{pin } 9) = 2.5V$	0	3.0	30	$\mu A$
<b>Current-Sense Amplifier Section</b>						
ISH / ISL Input Current	$I_{in}$	$V(\text{pin } 12) = V(\text{pin } 13) = 0V,$	-850	-320	0	$\mu A$
Input Offset Current	$I_{os}$	$V(\text{pin } 12) = V(\text{pin } 13) = 0V,$	-	$\pm 2.0$	$\pm 12$	
Peak Current Threshold Voltage	$V_{pk}$	$V(\text{pin } 12) = 0V, V(\text{pin } 13)$	0.14	0.20	0.26	V
Over Current Threshold Voltage	$V_{oc}$	Varied to Threshold	0.26	0.30	0.36	
ISH / ISL Input Voltage Range	-	( Note 2 )	-1.0	-	2.0	
Amplifier Voltage Gain	$A_v$	$V(\text{pin } 12) = 0.3V, V(\text{pin } 13) = 0.5V$ to $0.7V$	1.75	1.95	2.15	V/V
Amplifier Level Shift	-	$V(\text{pin } 12) = V(\text{pin } 13) = 0.3V$	2.4	2.5	2.65	V

## Electrical Characteristics - Continued

Parameter	Symbol	Test Conditions (Note 1)	Min.	Typ.	Max.	Units
<b>Logic Input Section</b>						
H1, H2, H3 Low Voltage Threshold	$V_{il}$	$T_c$ over operating range	0.8	1.0	1.2	V
H1, H2, H3 High Voltage Threshold	$V_{ih}$		1.6	1.9	2.0	
H1, H2, H3 Input Current	$I_{in}$	$T_c$ over operating range, $V(\text{pin } 20, 21, \text{ or } 22) = 0V$	-400	-250	-120	$\mu A$
Quad Select / Direction Threshold Voltage	$V_{th}$	$T_c$ over operating range	0.8	1.4	2.0	V
Quad Select Voltage Hysteresis	$V_h$		-	70	-	mV
Direction Voltage Hysteresis			-	0.6	-	V
Quad Select Input Current	$I_{in}$		-30	50	150	$\mu A$
Direction Input Current			-30	-1.0	30	
<b>Overvoltage / Coast Input Section</b>						
Overvoltage / Coast Inhibit Threshold Voltage	$V_{th}$	$T_c$ over operating range	1.65	1.75	1.85	V
Overvoltage / Coast Restart Threshold Voltage			1.55	1.65	1.75	
Overvoltage / Coast Hysteresis Voltage	$V_h$		0.05	0.10	0.15	
Overvoltage / Coast Input Current	$I_{in}$		-10	-1.0	0	$\mu A$
<b>Soft-Start Section</b>						
Soft-Start Pull-Up Current	$I_p$	$V(\text{pin } 18) = 0V$	-16	-10	-5.0	$\mu A$
Soft-Start Discharge Current	$I_d$	$V(\text{pin } 18) = 2.5V$	0.1	0.4	3.0	mA
Soft-Start Reset Threshold Voltage	$V_{th}$		0.1	0.2	0.3	V
<b>Tachometer/Brake Section</b>						
Tachometer Output High Level	$V_{oh}$	$T_c$ over operating range (pin15) 10K $\Omega$ to 2.5V	4.7	5.0	5.3	V
Tachometer Output Low Level	$V_{ol}$		-	-	0.2	
Tachometer On-Time	$t_{on}$		85	100	140	$\mu S$
Tachometer On-Time Variation	-	$T_c$ over operating range	-	0.1	-	%
Brake/Tach Timing Input Current	$I_{in}$	$V(\text{pin } 16) = 0V$	-4.0	-1.9	-	mA
Brake/Tach Timing Threshold Voltage	$V_{th}$	$T_c$ over operating range	0.8	1.0	1.2	V
Brake/Tach Timing Voltage Hysteresis	$V_h$		-	0.09	-	
Speed Input Threshold Voltage	$V_{th}$	$T_c$ over operating range	220	257	290	mV
Speed Input Current	$I_{in}$		-30	-5.0	30	$\mu A$
<b>Oscillator Section</b>						
Oscillator Frequency	$f_o$	Measured at pin 10	13.5	14.8	20	KHz

## Specification Notes:

- All parameters specified for  $T_a = 25^\circ C$ ,  $V_{cc} = 15V_{dc}$ ,  $R_{osc} = 75K\Omega$  (to Vref),  $C_{osc} = 1800pF$ , and all Phase Outputs unloaded ( $T_a - T_j$ ). All negative currents shown are sourced by (flow from) the pin under test.
- Either ISH or ISL may be driven over the range shown.
- Bold parameters tested over temperature range.

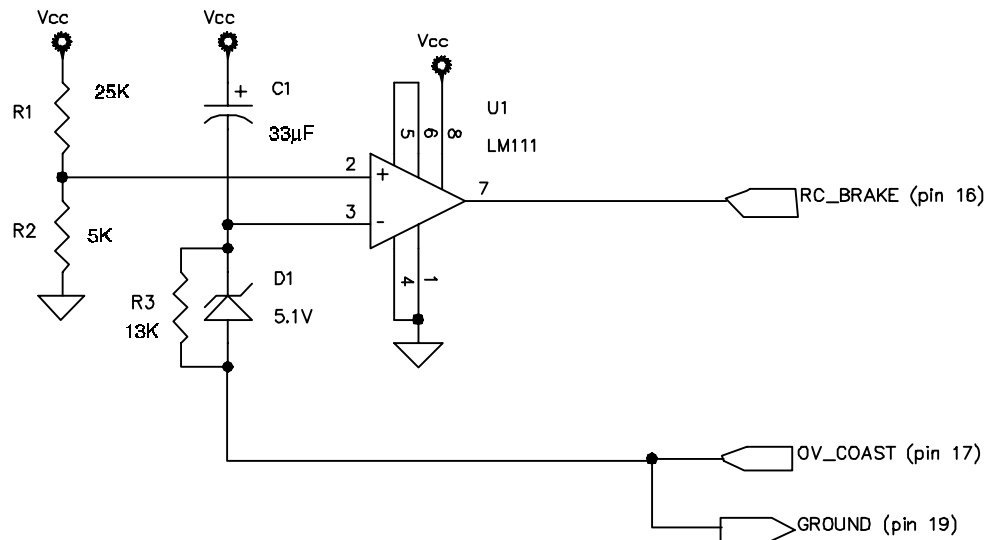
## APPLICATIONS

### Start-Up Conditions

The OM9369 3-phase brushless DC motor controller/driver is designed to drive fractional to integral horsepower motors. To ensure proper operation, it is necessary to ensure that the high-side bootstrap capacitors are charged during initial start-up. However, the method(s) used to ensure this may be dependant upon the application. For example, some applications may only require that OV\_COAST (pin 17) be connected to ground, either via a hardwire connection or via a switch (Enable/Disable), before applying Vcc. When Vcc is applied, the controller/driver is forced into brake mode for approximately 200 $\mu$ s (all high-side drivers are disabled and all low-side drivers are enabled).

This may not be adequate for other applications; while maintaining a constant speed command, (above zero), RC\_BRAKE (pin 16) may have to be momentarily connected to ground via a switch, either manually or electronically (ref. Figure 1). Note that with the component values shown in Figure 1, RC\_BRAKE is pulled for low for approximately 300ms after applying Vcc at pin 1.

Fig 1: Start-Up Circuit



**Modes of Operation**

Figures 2 and 3, shown on the following pages, provides schematic representations of typical voltage-mode and current -mode applications for the OM9369 controller/driver.

Figure 2 represents the implementation of a typical voltage-mode controller for velocity control. A voltage or speed command is applied to the noninverting input of the error amplifier which is configured as voltage follower. The output of the error amplifier is compared to a pulse width modulated ramp, and since motor speed is nearly proportional to the average phase output voltage, the average speed is controlled via duty cycle control. If a speed feedback loop is required, the tachometer output can be connected to the inverting input of the error amplifier via a loop compensation network.

Figure 2 also shows the implementation of the cycle-by-cycle current limit/overcurrent protection feature of the OM9369. The load current is monitored via the controller's internal sense resistor. The current sense signal is filtered and fed into the current sense amplifier where the absolute value of ISH-ISL is multiplied by two and biased up by 2.5V. The output of the current sensor amplifier is compared to a fixed reference, thus providing cycle-by-cycle current limiting and/or overcurrent protection as necessary. The typical peak current threshold (ISL-ISH) is 0.2V; the typical over current threshold (ISH-ISL) is 0.3V.

**Fig 2: Implementation of a Voltage -Mode Controller**

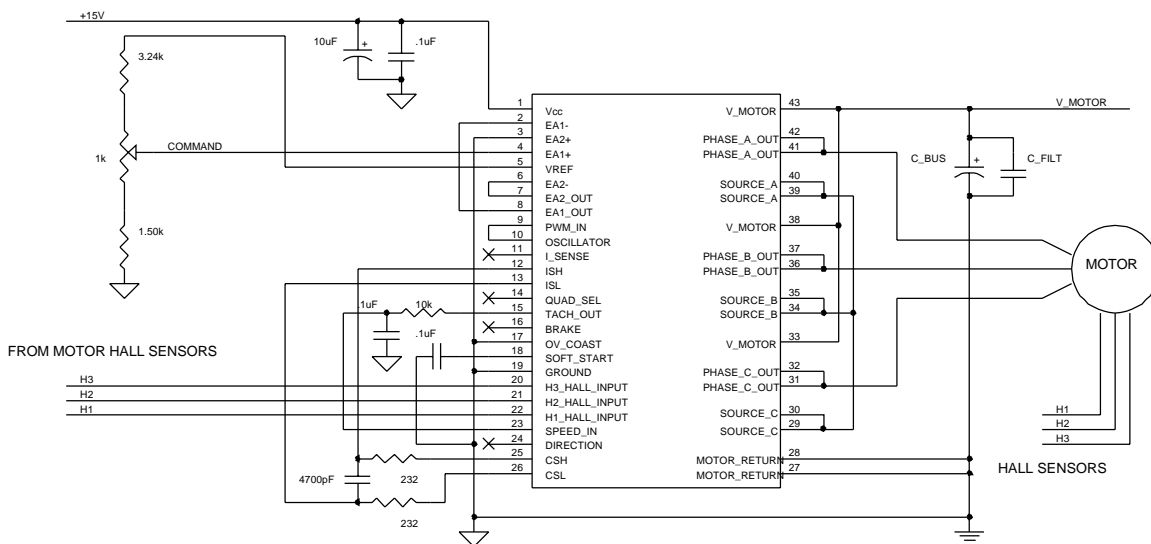
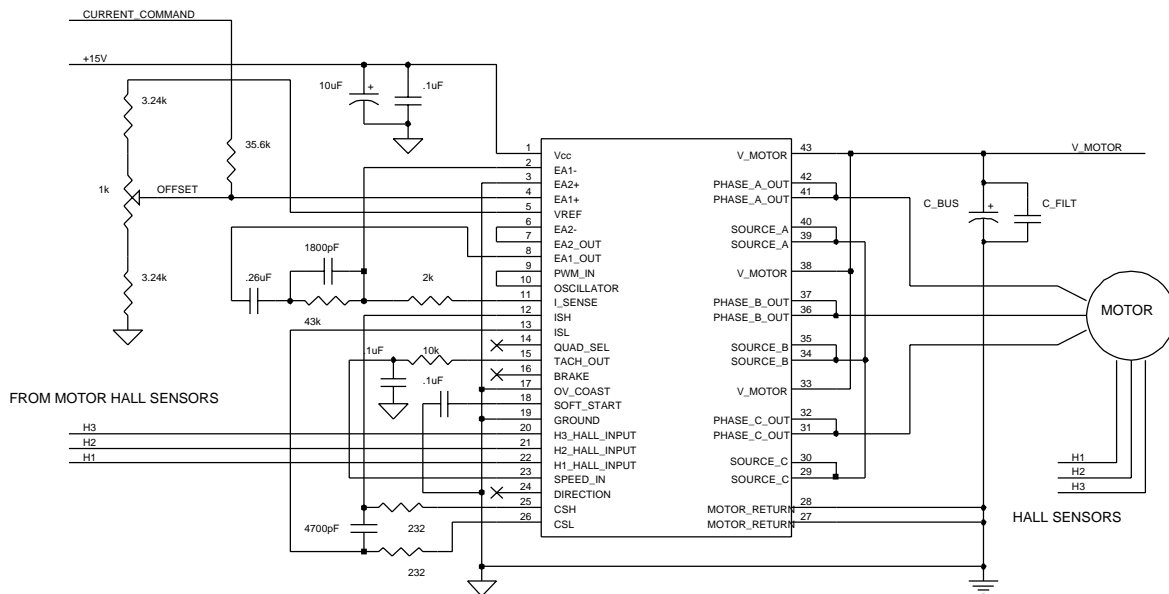


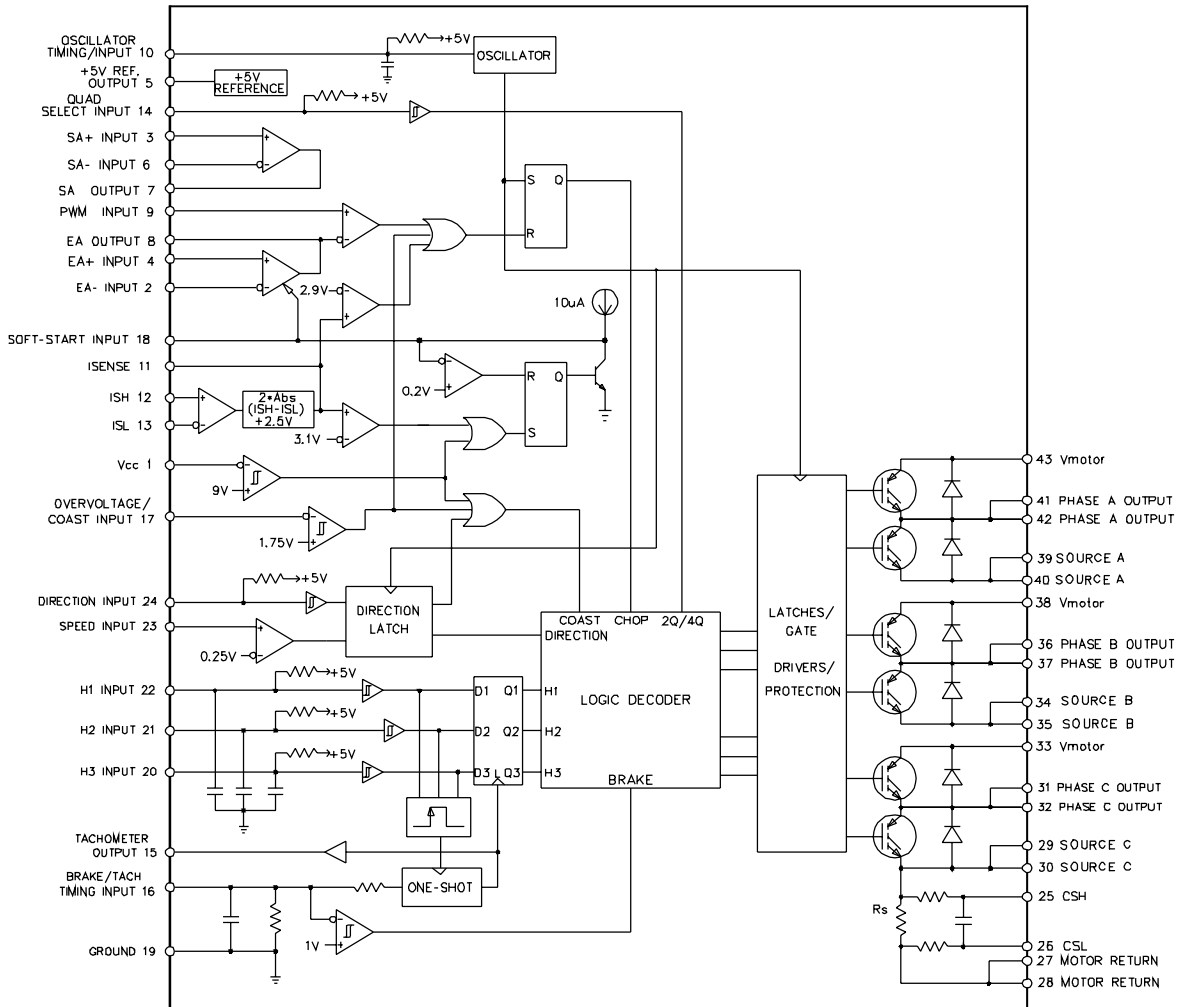
Figure 3 represents the implementation of a typical current-mode controller for torque control. The load current is monitored via the controller's internal sense resistor. The current sense signal is filtered and fed into the current sense amplifier where the absolute value of ISH-ISL is multiplied by two and biased up by 2.5V. Besides the implementation of the cycle-by-cycle current limit/overcurrent protection feature of the OM9369 discussed in the preceding paragraph, the

output of the current sense amplifier is fed into the error amplifier which is configured as a differential amplifier. An error signal representing the difference between the current command input and the value of the amplified current sense signal is produced. Then it is compared to a pulse width modulated ramp and since torque is nearly proportional to the average phase output current, the torque is controlled via duty cycle control.

**Fig 3: Implementation of a Current-Mode Controller**



Simplified Block Diagram





## Pin Descriptions / Functionality

**VCC (Pin 1)** -- The Vcc Supply input provides bias voltage to all of the internal control electronics within the OM9369, and should be connected to a nominal +15Vdc power source. High frequency bypass capacitors (10uF polarized in parallel with 0.1uF ceramic are recommended) should be connected as close as possible to pin 1 and Ground (pin 19).

**ERROR AMPLIFIER (EA1- Input, Pin 2; EA1+ Input, Pin 4; EA1 Output, Pin 8)** -- The Error Amplifier is an uncommitted LM158-type operational amplifier, providing the user with many external control loop compensation options. This amplifier is compensated for unity gain stability, so it can be used as a unity gain input buffer to the internal PWM comparator when pin 2 is connected to pin 8. The output of the Error Amplifier is internally connected to the PWM comparator's "-" input, simplifying external layout connections.

**+5V REFERENCE OUTPUT (Pin 5)** -- This output provides a temperature-compensated, regulated voltage reference for critical external loads. It is recommended that this pin be used to power the external Hall-effect motor position sensors. By design, the +5V reference must be in regulation before the remainder of the control circuitry is activated. This feature allows the Hall-effect sensors to become powered and enabled before any Phase Output is enabled in the OM9369 preventing damage at turn-on. High-frequency bypass capacitors (10uF polarized in parallel with 0.1uF ceramic are recommended) should be connected as close as possible to pin 5 and Ground (pin 19).

**SPARE AMPLIFIER (EA2- Input, Pin 6; EA2+ Input, Pin 3; EA2 Output, Pin 7)** -- The Spare Amplifier is an uncommitted LM158-type operational amplifier, and in addition to the internal error amplifier, provides the user with additional external control loop compensation options. This amplifier is also compensated for unity gain stability and it can be used as a unity gain input buffer when pin 6 is connected to pin 7. If the Spare Amplifier is unused, pin 3 should be connected to Ground, and pin 6 should be connected to pin 7.

**PWM INPUT (Pin 9)** -- This pin is connected to the "+" input of the internal PWM comparator. The PWM output clears the internal PWM latch, which in turn commands the Phase Outputs to chop. For voltage-mode control systems, pin 9 may be connected to the Oscillator Timing Input, pin 10.

**OSCILLATOR TIMING INPUT (Pin 10)** -- The Oscillator Timing Input sets a fixed PWM chopping frequency by means of an internal resistor (Rosc), whose value is set to 75kΩ, connected from pin 10 to the +5V Reference Output, and an internal capacitor (Cosc), whose value is 1800pF, connected from pin 10 to Ground. In custom applications, the recommended range of values for Rosc is 10kΩ to 100kΩ, and for Cosc is 0.001uF to 0.01uF, and the maximum operating frequency should be kept below 20kHz. The approximate oscillator frequency is:

$$f_o = \frac{2}{(\text{Rosc} \times \text{Cosc})} \text{ [ Hz ]}$$

The voltage waveform on pin 10 is a ramp whose magnitude is approximately 1.2Vp-p, centered at approximately 1.6Vdc. In addition to the voltage-mode PWM control, pin 10 may be used for slope compensation in current-mode control applications.

**ISENSE (Pin 11)** -- This pin is connected to the output of the internal current-sense amplifier. It drives a peak-current (cycle-by-cycle) comparator which controls Phase Output chopping, and a fail-safe current comparator which, in the event of an output overcurrent condition, activates the soft-start feature and disables the Phase Outputs until the overcurrent condition is removed. The magnitude of the voltage appearing at pin 11 is dependent upon the voltages present at the current-sense amplifier inputs, ISH and ISL:

$$V(\text{Isense}) = 2.5\text{V} + [2 \times \text{ABS}(\text{ISH} - \text{ISL})] \text{ [ V ]}$$

### CURRENT SENSE INPUTS (ISH, Pin 12; ISL, pin 13)

These inputs to the current-sense amplifier are interchangeable and they can be used as differential inputs. The differential voltage applied between pins 12 and 13 should be kept below +/-0.5Vdc to avoid saturation.

**QUAD SELECT INPUT (Pin 14)** -- This input is used to set the OM9369 in a half control or full control chopping regime. When driven with a logic low level, the OM9369 is in the half control mode, whereby only the three lower (pull-down) power switches associated with the Phase Outputs are allowed to chop. Alternately, when driven with a logic high level, the OM9369 is in the full control mode, where all six power switches (pull-up and pull-down) associated with the Phase Outputs are chopped by the PWM. During motor braking, changing the logic state of the Quad Select Input has no effect on the operation of the OM9369.

**TACHOMETER OUTPUT (Pin 15)** -- This output provides a fixed width 5V pulse when any Hall-effect Input (1, 2 or 3) changes state. The pulse width of the Tachometer Output is set internally in the OM9369 to 113µs (nominal). The average value of the output voltage on pin 15 is directly proportional to the motor's speed, so this output may be used (with an external averaging filter) as a true tachometer output, and fed back to the Speed Input (pin 23) to sense the actual motor speed.

**Note:** Whenever pin 15 is high, the internal Hall-effect position latches are inhibited (i.e. "latched"), to reject noise during the chopping portion of the commutation cycle, and this makes additional commutations impossible. This means that in order to prevent false commutation at a speed less than the desired maximum speed, the highest speed as observed at the Tachometer Output should be set above the expected maximum value.

**BRAKE / TACH TIMING INPUT (Pin 16)** -- The Brake/Tach Timing Input is a dual-purpose input. Internal to the OM9369 are timing components tied from pin 16 to Ground (a 51kΩ resistor and a 3300pF capacitor). These components set the minimum pulse width of the Tachometer Output to 113µs, and this time may be adjusted using external components, according to the equation:

$$T(\text{tach}) = 0.67 \times (C_t + 3300\text{pf}) \times \left( \frac{R_t \times 51\text{k}\Omega}{R_t + 51\text{k}\Omega} \right) (\mu\text{s})$$

The recommended range of external resistance (to Ground) is 15kΩ to ∞, and the range of external capacitance (to Ground) is 0pF to 0.01µF. With each Tachometer Output pulse, the capacitor tied to pin 16 is discharged from approximately 3.33V to

approximately 1.67V by an internal timing resistor. The Brake / Tach Timing Input has another function. If this pin is pulled below the brake threshold voltage, the OM9369 will enter the brake mode. The brake mode is defined as the disabling of all three high-side (pull-up) drivers associated with the Phase Outputs, and the enabling of all three low-side (pull-down) drivers.

**OVERVOLTAGE / COAST INPUT (Pin 17)** -- This input may be used as a shutdown or an enable/disable input to the OM9369. Also, since the switching inhibit threshold is so tightly defined, this input can be directly interfaced with a resistive divider which senses the voltage of the motor supply, V<sub>m</sub>, for overvoltage conditions. A high level (greater than the inhibit threshold) on pin 17 causes the coast condition to occur, whereby all Phase Outputs revert to a Hi-Z state and any motor current which flowed prior to the Overvoltage/ Coast command is commutated via the power "catch" rectifiers associated with each Phase Output.

**SOFT-START INPUT (Pin 18)** -- The Soft-Start input is internally connected to a 10µA (nominal) current source, the collector of an NPN clamp/discharge transistor, and a voltage comparator whose soft-start/restart threshold is 0.2Vdc (nominal). An external capacitor is connected from this pin to Ground (pin 19). Whenever the V<sub>cc</sub> supply input drops below the turn-on threshold, approximately 9Vdc, or the sensed current exceeds the over-current threshold, approximately 0.3V at the current sense amplifier, the soft-start latch is set. This drives the NPN clamp transistor which discharges the external soft-start capacitor. When the capacitor voltage drops below the soft-start/restart threshold and a fault condition does not exist, the soft-start latch is cleared; the soft-start capacitor charges via the internal current source.

In addition to discharging the soft-start capacitor, the clamp transistor also clamps the output of the error amplifier internal to the controller IC, not allowing the voltage at the output of the error amplifier to exceed the voltage at pin 18, regardless of the inputs to the amplifier. This action provides for an orderly motor start-up either at start-up or when recovering from a fault condition.

**GROUND (Pin 19)** - The voltages that control the OM9369 are referenced with respect to this pin. All bypass capacitors, timing resistors and capacitors, loop compensation components, and the Hall-effect filter capacitors must be referenced as close as possible to pin 19 for proper circuit operation. Additionally, pin 19 must be connected as close as physically possible to the Motor Return, pins 27 and 28.

**HALL-EFFECT INPUTS (H1, Pin 22; H2, Pin 21; H3, Pin 20)** - Each input has an internal pull-up resistor to the +5V Reference. Each input also has an internal 180pF noise filter capacitor to Ground. In order to minimize the noise which may be coupled from the motor commutation action to these inputs, it is strongly recommended that additional external filter capacitors, whose value is in the range of 2200pF, be connected from each Hall-Effect Input pin to Ground. Whatever capacitor value is used, the rise/fall times of each input must be guaranteed to be less than 20us for proper tachometer action to occur. Motors with 60 degree position sensing may be used if one or two of the Hall-effect sensor signals is inverted prior to connection to the Hall-Effect Inputs.

**SPEED INPUT (Pin 23)** - This pin is connected to the "+" input of a voltage comparator, whose threshold is 0.25Vdc. As long as the Speed Input is less than 0.25V, the direction latch is transparent. When the Speed Input is greater than 0.25V, then the direction latch inhibits all changes in direction. It is recommended, especially while operating in the half control mode, that the Tachometer Output is connected to the Speed Input via a low-pass filter, **such that the direction latch is transparent only when the motor is spinning very slowly**. In this case, the motor has too little stored energy to damage the power devices during direction reversal.

**DIRECTION INPUT (Pin 24)** - This input is used to select the motor direction. This input has an internal protection feature: the logic-level present on the Direction Input is first loaded into a direction latch, then shifted through a two-bit shift register before interfacing with the internal output phase driver logic decoder. Also, protection circuitry detects when the input and the output of the direction latch or the 2-bit shift register are different, and inhibits the Phase Outputs (i.e. Hi-Z) during those times. This

feature may be used to allow the motor to coast to a safe speed before a direction reversal takes place. Power stage cross-conduction (current "shoot-through" from Vmotor to Ground through simultaneously enabled pull-up and pull-down drivers) is prevented by the shift register as it is clocked by the PWM oscillator, so that a fixed delay of between one and two PWM oscillator clock cycles occurs. This delay or "dead-time" guarantees that power-stage cross-conduction will not occur.

**CURRENT SENSE OUTPUTS (CSH, Pin 25; CSL, Pin 26)** - The Current Sense Outputs produce a differential voltage equal to the motor current times the sense resistance value (5mΩ nominal). There is an internal 1000pF filter capacitor across pins 25 and 26, and two 100Ω series resistors, one between each pin and each end of the current sense resistor. To configure the current sense amplifier for cycle-by-cycle current limiting and/or overcurrent protection, connect pin 25 to pin 12 (ISH) and pin 26 to pin 13 (ISL).

**MOTOR RETURN (Pins 27 and 28)** - These pins are connected to the most negative terminal of the motor supply (Vm-). This connection is electrically isolated from the logic ground internal to the OM9369 package to minimize, if not eliminate, noise on the logic ground. The connection to the logic ground is made by the user external to the package (refer to Ground (pin 19)). In order to minimize packaging losses and parasitic effects, it is essential that both of these pins be firmly connected to the motor supply Ground, with as short a connection as physically possible.

**SOURCE (Pins 29, 30, 34, 35, 39 and 40)** - The source pins form the low-side connection of the pull-down switches associated with each Phase Output. Because of the switching current capability of the OM9369, all 6 pins should be externally connected together with a low impedance bus to minimize losses and voltage differentials. Also, due to layout design considerations, pin 29 and pin 30 are internally connected to the "top" of the internal current-sense resistor.

**PHASE OUTPUTS (Phase A, Pins 41 and 42; Phase B, Pins 36 and 37; Phase C, Pins 31 and 32)**

These outputs are connected to either  $V_{\text{motor}}$  via the pull-up driver or Source via the pull-down driver, depending upon the Hall-Effect and Direction Inputs (see Commutation Truth Table). The two pins associated with each Phase Output must be connected to one of the three phases of the motor driven by the OM9369.

**$V_{\text{MOTOR}}$  (Pins 33, 38, and 43)** - These pins are connected to the most positive terminal of the motor supply ( $V_{\text{m+}}$ ). For proper operation, all three pins

must be connected together externally with a low impedance power bus. The  $V_{\text{motor}}$  power bus should be bypassed with an adequately voltage-rated ceramic capacitor, 0.1 $\mu\text{F}$  (typical), and a low-ESR electrolytic capacitor, whose capacitance can be selected by the following: 10 $\mu\text{F}$ -per-Ampere of average motor current from  $V_{\text{motor}}$  to Motor Return.

**Note: All connections, including the power bus capacitor connections, must be made as close as possible to the  $V_{\text{motor}}$  and Motor Return pins to minimize parasitic effects.**

**Pin Designation**

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
1	$V_{\text{CC}}$	12	ISH	23	Speed Input	34	Source B
2	EA1 "-" Input	13	ISL	24	Direction Input	35	Source B
3	EA2 "+" Input	14	Quad Select Input	25	CSH	36	Phase B Output
4	EA1 "+" Input	15	Tachometer Output	26	CSL	37	Phase B Output
5	+5V Reference Output	16	Brake/Tach Timing Input	27	Motor Return	38	$V_{\text{motor}}$
6	EA2 "-" Input	17	Overvoltage/Coast Input	28	Motor Return	39	Source A
7	EA2 Output	18	Soft-Start Input	29	Source C	40	Source A
8	EA1 Output	19	Ground	30	Source C	41	Phase A Output
9	PWM Input	20	H3 Input	31	Phase C Output	42	Phase A Output
10	Oscillator Timing Input	21	H2 Input	32	Phase C Output	43	$V_{\text{motor}}$
11	Isense	22	H1 Input	33	$V_{\text{motor}}$	Case	(No Connection)

### Commutation Truth Table

Table 1 shows the Phase Output state versus the state of the Hall-Effect and Direction Inputs. Please note that the OM9369 Hall-Effect Inputs are Grey-encoded; that is, only one input is allowed to change from one input state to another at a time.

The commutation coding shown reflects Hall-Effect sensors that are spaced at 120° mechanical increments. Also, internal protection logic disables all three Phase Outputs when the Hall-Effect Inputs are set to an illegal condition (i.e. all logic low or all logic high).

**Table 1 - Commutation Truth Table**

Digital Inputs				Phase Outputs		
Dir	H1	H2	H3	A	B	C
1	0	0	1	Hi-Z	Sink	Source
1	0	1	1	Sink	Hi-Z	Source
1	0	1	0	Sink	Source	Hi-Z
1	1	1	0	Hi-Z	Source	Sink
1	1	0	0	Source	Hi-Z	Sink
1	1	0	1	Source	Sink	Hi-Z
0	1	0	1	Sink	Source	Hi-Z
0	1	0	0	Sink	Hi-Z	Source
0	1	1	0	Hi-Z	Sink	Source
0	0	1	0	Source	Sink	Hi-Z
0	0	1	1	Source	Hi-Z	Sink
0	0	0	1	Hi-Z	Source	Sink
X	0	0	0	Hi-Z	Hi-Z	Hi-Z
X	1	1	1	Hi-Z	Hi-Z	Hi-Z

### Package and Screening Options

The OM9369 is offered in F-43, a hermetic flatpack package as well as in MP3-43L, a plastic ring frame, low profile flatpack package.

The hermetic version is offered in two standard screening levels: a full military temperature range of -55°C to +125°C with limited screening and with

MIL-STD-883 screening. The plastic ring frame version is offered in an industrial temperature range of -40°C to +85°C with limited screening.

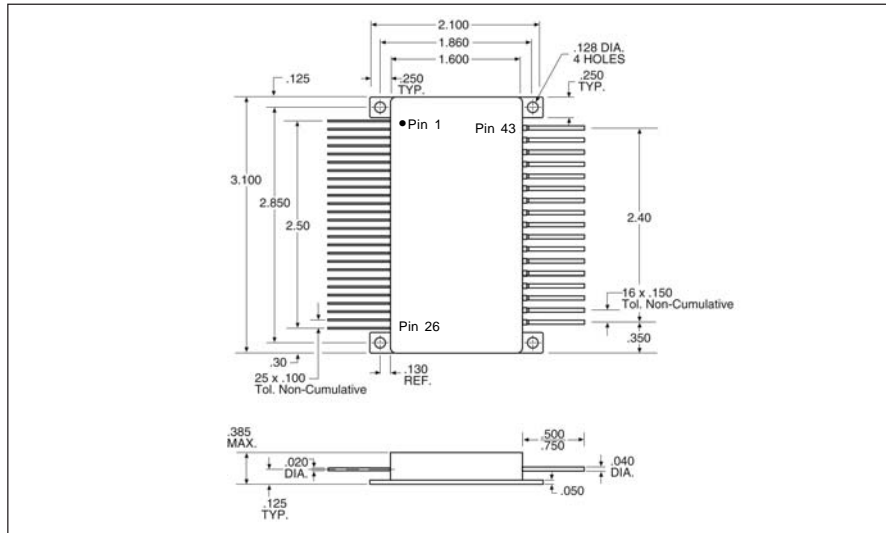
The screening levels for the SFB, SFP and SPP versions are listed in the table below. All tests and inspections are in accordance with those listed in MIL-STD-883.

Test / Inspection	SFB	SFP	SPP
Precap Visual Inspection	100%	100%	100%
Temperature Cycle	100%	NA	NA
Mechanical Shock	100%	NA	NA
Hermeticity ( Fine and Gross Leak )	100%	100%	NA
Pre Burn-In Electrical	100%	NA	NA
Burn-In ( 160 hours )	100%	NA	NA
Final Electrical Test	-55°C, 25°C, +125°C	+25°C	+25°C
Group A Testing	100%	NA	NA
Final Visual Inspection	100%	100%	100%

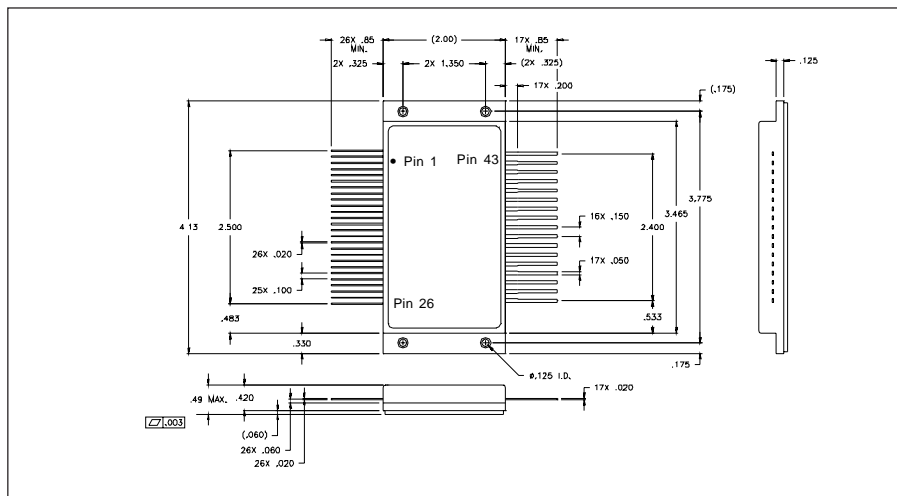
OM9369

International  
**IR** Rectifier

**Mechanical Outline - F-43 ( OM9369SF )**



**Mechanical Outline - MP3-43L ( OM9369SP )**



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**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

IR LEOMINSTER: 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776

Visit us at [www.irf.com](http://www.irf.com) for sales contact information.

Data and specifications subject to change without notice. 11/03