DATA SHEET

TPM754A

Microcontroller with TrackPoint™ microcode from IBM

Preliminary specification
Replaces datasheet TPM754 of 1997 Dec 03
IC28 Data Handbook

1999 Nov 11

Philips
Semiconductors

PHILIPS

Microcontroller with TrackPoint™ microcode from IBM TPM754A

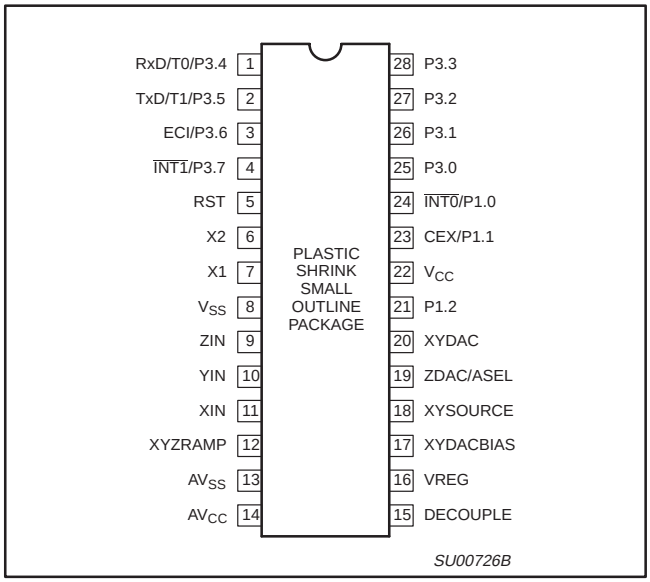
The Philips Semiconductors TPM754 is a small package, low cost, ROM-coded 80C51 with IBM®'s TrackPoint™ pointing algorithms and control code. TrackPoint is the result of years of human factors research and innovation at IBM. The result is a "velocity sensitive" pointing solution more efficient and easier to use than "position sensitive" devices such as the mouse, the trackball, or the touchpad.

IBM has licensed Philips Semiconductors to sell microcontrollers with TrackPoint code. By purchasing a TPM from Philips, the purchaser becomes a sub-licensee of Philips. The selling price of Philips' TPM includes the royalties for IBM's intellectual property, which Philips in turn pays to IBM. Customers for TPMs do not need to sign any licensing agreement with either IBM or Philips. This code is the intellectual property of IBM, which is covered by numerous patents, and must be treated accordingly.

The TPM754 contains IBM® TrackPoint™ code, a single module PCA, a 256 × 8 RAM, 21 I/O lines, two 16-bit counter/timers, a two-priority level interrupt structure, a full duplex serial channel, an on-chip oscillator, and an 8-bit D/A converter.

For identical device without TrackPoint code, see the 8XC754 datasheet.

PIN CONFIGURATION



FEATURES

- 80C51-based architecture
- Small package sizes – 28-pin SSOP
- Power control modes:
  - Idle mode
  - Power-down mode
- 256 × 8 RAM
- Two 16-bit auto reloadable counter/timers
- Single module PCA counter/timer
- Full duplex serial channel
- Boolean processor
- CMOS and TTL compatible

ORDERING INFORMATION

ORDERING CODE	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
PTPM754A DB	0 to +70, 28-pin Shrink Small Outline Package	3.5 to 12 MHz	SOT341-1

NOTE:
1. PTPM754A has improved start-up from low-voltage power down.

IBM is a registered trademark, and TrackPoint is a trademark of IBM Corporation.

PIN DESCRIPTION

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
V_{SS}	8	I	**Circuit Ground Potential.**
V_{CC}	22	I	**Supply voltage during normal, idle, and power-down operation.**
P1.0–P1.2	21, 23, 24	I/O	**Port 1:** Port 1 is a 3-bit bidirectional I/O port with internal pull-ups on P1.0 and P1.1. Port 1 pins that have 1s written to them can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups (P1.0, P1.1). (See DC Electrical Characteristics: I_{IL}). Port 1 also serves the special function features listed below (Note: P1.0 does **not** have the strong pullup that is on for 2 oscillator periods.):
	24	I	**$\overline{INT0}$ (P1.0):** External interrupt 0.
	23	O	**CEX (P1.1):** PCA clock output.
P3.0–P3.7	1–4, 25–28	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). (Note: P3.5 does **not** have the strong pullup that is on for 2 oscillator periods.)
			Port 3 also serves the special function as listed below:
	3	I	**ECI (P3.6):** External PCA clock input.
	1	I	**RxD/T0 (P3.4):** Serial port receiver data input. Timer 0 external clock input.
	4	I	**$\overline{INT1}$:** External interrupt 1.
	2	I	**TxD/T1 (P3.5):** Serial port transmitter data. Timer 1 external clock input.
RST	5	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running resets the device. **(NOTE: The TPM754 does not have an internal reset resistor.)**
X1	7	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
X2	6	O	**Crystal 2:** Output from the inverting oscillator amplifier.
AV_{CC} [1]	14	I	**Analog supply voltage and reference input.**
AV_{SS} [1]	13	I	**Analog supply and reference ground.**
ZIN	9	I	**ZIN:** Input to analog multiplexer.
YIN	10	I	**YIN:** Input to analog multiplexer.
XIN	11	I	**XIN:** Input to analog multiplexer.
XYZRAMP	12	O	**XYZRAMP:** Provides a low impedance pulldown to V_{SS} under S/W control.
DECOUPLE	15	O	**DECOUPLE:** Output from regulated supply for connection of decoupling capacitors.
VREG	16	O	**VREG:** Provides regulated analog supply output.
XYDACBIAS	17	O	**XYDACBIAS:** Provides source voltage for bias of external circuitry.
XYSOURCE	18	O	**XYSOURCE:** Provides source voltage from regulated analog supply.
ZDAC	19	O	**ZDAC:** Switchable output from the internal DAC.
XYDAC	20	O	**XYDAC:** Non-switchable output from the internal DAC.

NOTE:
1. AV_{SS} (reference ground) must be connected to 0 V (ground). AV_{CC} (reference input) cannot differ from V_{CC} by more than ±0.2 V, and must be in the range 4.5 V to 5.5 V.

OSCILLATOR CHARACTERISTICS

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

The TPM754 includes the 80C51 power-down and idle mode features. In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals except the D/A stays active. The functions that continue to run while in the idle mode are the timers and the interrupts. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset. Upon powering-up the circuit, or exiting from idle mode, sufficient time must be allowed for stabilization of the internal analog reference voltages before a D/A conversion is started.

I/O Ports

The I/O pins provided by the TPM754 consist of port 1 and port 3.

Port 1

Port 1 is a 3-bit bidirectional I/O port and includes alternate functions on some pins of this port. Pins P1.0 and P1.1 are provided with internal pullups while the remaining pin (P1.2) has an open drain output structure. The alternate functions for port 1 are:

$\overline{INT0}$ – External interrupt 0.
CEX – PCA clock output.

Port 3

Port 3 is an 8-bit bidirectional I/O port structure.

The alternate functions for port 3 are:

RxD – Serial port receiver data input.
T1 – Timer 1 external clock input.
$\overline{INT1}$ – External interrupt 1.
TxD – Serial port transmitter data.
T0 – Timer 0 external clock input.
ECI – PCA external clock input.

Analog Section

The analog section of the TPM754, shown in Figure 1, consists of four major elements: a bandgap referenced voltage regulator, an 8-bit DAC, an input multiplexer and comparator, and a low impedance pulldown device.

The bandgap voltage regulator uses the AV_{CC} pin as its supply and produces a regulated output on the VREG pin. The regulator also supplies the analog supply voltage for the DAC. The regulator may be switched on/off by means of the AC1 bit in the analog control register (ACON0). The regulator output may also be supplied to the XYDACBIAS and XYSOURCE pins by means of bits AC3 and AC4, respectively. The DECOUPLE pin is provided for decoupling the regulator output.

The DAC is an 8-bit device and its output appears on the XYDAC pin. In addition, the DAC output may also be routed to the ZDAC pin by means of bit AC6 in the ACON0 register. The DAC output is not buffered, so external load impedances should be taken into consideration when using either of these outputs.

A 3-input multiplexer is provided, whose output is connected to the positive reference of a comparator. The multiplexer output is controlled by bits MUX2:0 of ACON1. A bandgap reference supplies the negative reference of the comparator. The output of the comparator may be used the trigger the capture input of module 4 of the PCA.

A low impedance pulldown is supplied at the XYZRAMP pin and is controlled by bit AC5 of ACON0.

The functions of the analog section are controlled by the IBM® TrackPoint™ code embedded within the Philips TPM754.

PC BOARD LAYOUT CONSIDERATIONS

The TrackPoint is a low-level analog circuit. While not difficult to implement, careful consideration should be given to circuit board layout to obtain proper operation of the TrackPoint. The considerations are similar to that used for radio frequency application. The circuit should be located far from the CPU and video lines, and should also be shielded from any digital signals. A 100μV pulse picked up every 3 or 4 seconds is sufficient to cause cursor drift. A good circuit board layout will result in a circuit that is very stable and will hold the cursor on a pixel for days at a time. However, the autorouters of most software board layout packages will not do an adequate job, and manual routing of this portion of the motherboard is recommended.

The TPM754 has excellent supply regulation for the analog portions of the TrackPoint circuit. However, care should be taken with respect to the circuit ground to avoid voltage shifts due to non-TrackPoint loads. The analog part of the circuit **must** have its own ground plane, isolated from everything else and connected to the main ground at just one point (no ground loops). All of the analog portion of the TrackPoint circuit, **and nothing else**, must be over this ground island.

No digital traces can pass though the analog area **on any level** from the ground plane out. The circuit should be confined to one side of the ground plane, preferably on the first interior layer, with the ground plane next. The circuit should be powered only at a single point (pin 14), and that power should be filtered to ground before it comes onto the analog area.

The signal lines from the TrackPoint sensor stick can be sensitive to pickup, and should be run close together, and not too close to digital lines. A grounded guard trace is a good idea. **Most important**, the stick common line **is not a ground** line, but rather a **signal** line, although it will eventually connect to the analog ground. A common and **serious** error is to treat it as ground, connecting it to a general ground at some convenient point.

The layout should be designed to keep things compact and minimize trace lengths. The whole circuit, analog and digital, will fit comfortably within 2cm × 3cm. In some situations, it may be desirable to put the circuit on a separate card instead of on the motherboard. In this case, a shielded cable should provide the best means of connecting the stick signals to the circuit card.

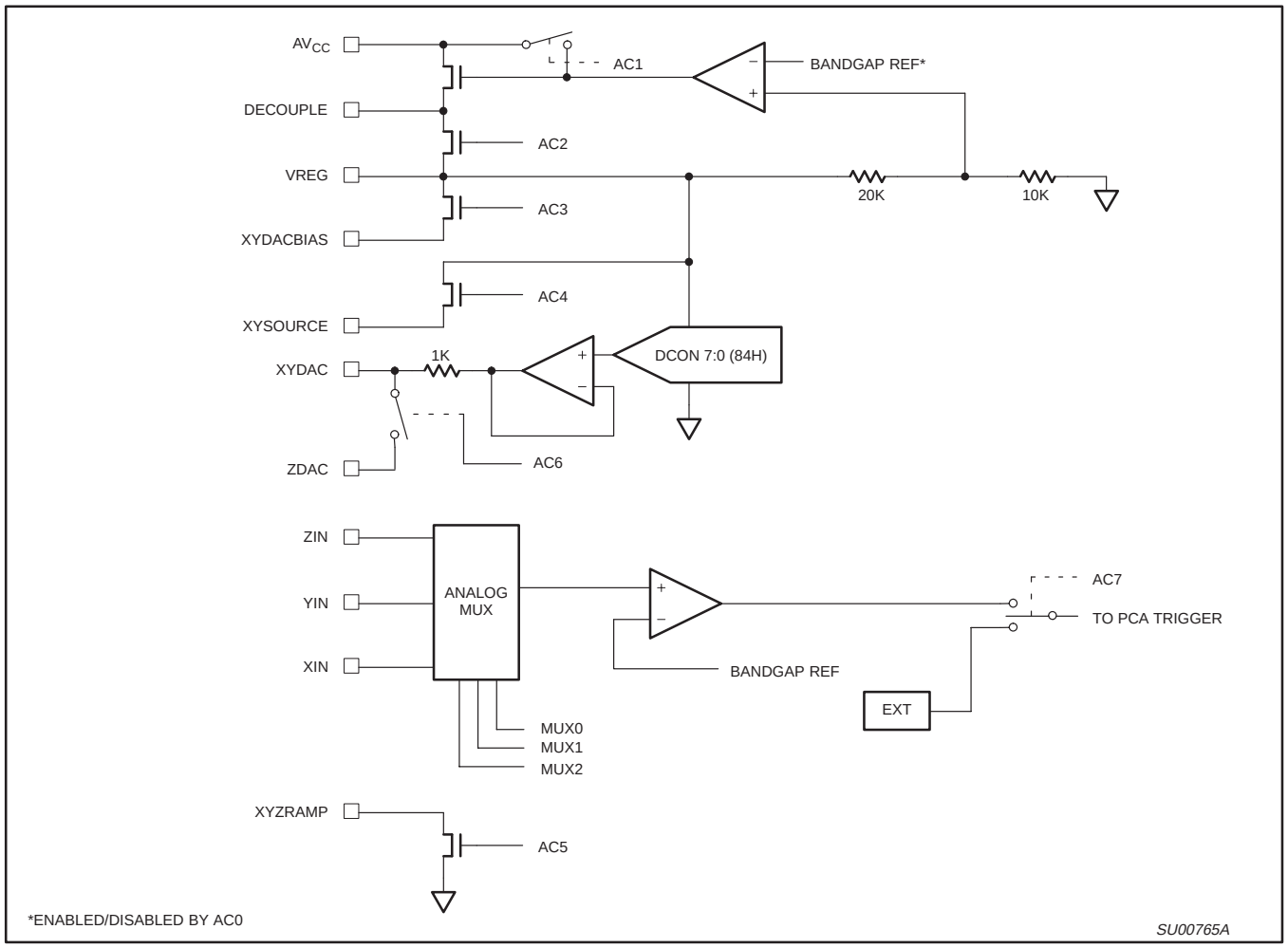


Figure 1. Analog Section

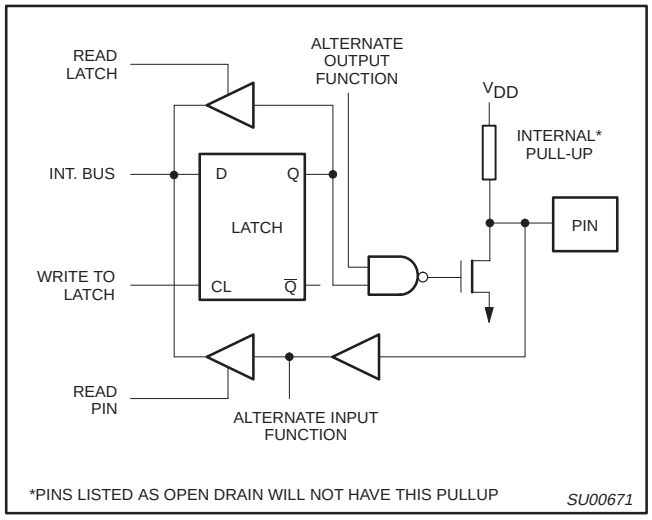


Figure 2. Typical Port Bit Latches and I/O Buffers

ABSOLUTE MAXIMUM RATINGS[1, 3, 4]

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage from V_{CC} to V_{SS}	–0.5 to +6.5	V
Voltage from any pin to V_{SS}	–0.5 to V_{CC} + 0.5	V
Power dissipation	1.0	W

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, AV_{CC} = 5 V ±5, AV_{SS} = 0 V[4]
V_{CC} = 5 V ± 10%, V_{SS} = 0 V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[4]			UNIT
			MIN	TYP[1]	MAX	
I_{CC}	Supply current (see Figure 5)					
Inputs						
V_{IL}	Input low voltage, port 1, 3		–0.5		$0.2V_{CC}$–0.1	V
V_{IH}	Input high voltage, port 1, 3		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, X1, RST		$0.7V_{CC}$		V_{CC}+0.5	V
Outputs						
V_{OL}	Output low voltage, port 3, 1.2	I_{OL} = 1.6 mA[2]			0.45	V
V_{OL1}	Output low voltage, port 1.0, 1.1	I_{OL} = 3.2 mA[2]			0.45	V
V_{OH}	Output high voltage, ports 3, 1.0, 1.1	I_{OH} = –60 µA,	2.4			V
I_{LI}	Input leakage current, port 1, 3, RST	0.45 < V_{IN} < V_{CC}			±10	µA
C_{IO}	Pin capacitance	Test freq = 1 MHz, T_{amb} = 25°C			10	pF

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. Under steady state (non-transient) conditions, IOL must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 67mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
5. Power-down I_{CC} is measured with all output pins disconnected; X2, X1 n.c.; RST = V_{SS}.
6. I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; X2 n.c.; RST = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.
7. Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; X2 n.c.; RST = V_{SS}.
8. Pin 9, 10, 11, and 21; $V_{IN} \leq V_{REG}$.

ANALOG SECTION ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C; V_{CC} = 5 V ± 10%, V_{SS} = 0 V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[4]			UNIT
			MIN	TYP[1]	MAX	
Analog Inputs						
AV_{CC}	Analog supply voltage		4.5	–	5.5	V
	Sensor resistor		330	–	3K	Ω
IAV_{CC}		AC0 = 0 IC only	–	1.2	2.5	mA
		AC0 = 1	–	–	10	µA
Regulator						
VREG		IVREG = 13 mA	3.6	3.8	4.3	V
ICHARGE	Decouple current	C_{DEC} = 10 µF	–	60	100	mA
CDECOUPLE		Stability requirement	–	10	–	µF
RDSONQ1			–	7	12	Ω
ILEAKAGEQ1			–10		+10	µA
ILEAKAGEQ2			–10		+10	µA
PSRR		100 Hz	–	–40	–	dB
MUX and Comparator						
	Comparator trip point		1.14	1.26	1.38	V
	MUX impedance		–	1	4	kΩ
ILEAKAGEMUX	$V_{IN} \leq V_{REG}$		–10		+10	µA
Digital-to-Analog Conversion						
	ZDAC, XYDAC monotonicity		8	–	–	bits
	ZDAC switch impedance		–	75	200	Ω
	DAC output resistance		–	2.7	5	kΩ
	ZDAC switch leakage		–10		+10	µA
Switches						
	XYZRAMP impedance		–	33	100	Ω
	XYZRAMP leakage		–10		+10	µA
	XYDACBIAS impedance		–	13	25	Ω
	XYDACBIAS leakage		–10		+10	µA
	XYSOURCE impedance		–	200	400	Ω
	XYSOURCE leakage		–10		+70	µA

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V[4]

SYMBOL	PARAMETER	VARIABLE CLOCK		UNIT
		MIN	MAX	
$1/t_{CLCL}$	Oscillator frequency:	3.5	12	MHz
External Clock (Figure 3)				
t_{CHCX}	High time	20		ns
t_{CLCX}	Low time	20		ns
t_{CLCH}	Rise time		20	ns
t_{CHCL}	Fall time		20	ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal.
The designations are:

C – Clock
D – Input data
H – Logic level high
L – Logic level low
Q – Output data
T – Time
V – Valid
X – No longer a valid logic level
Z – Float

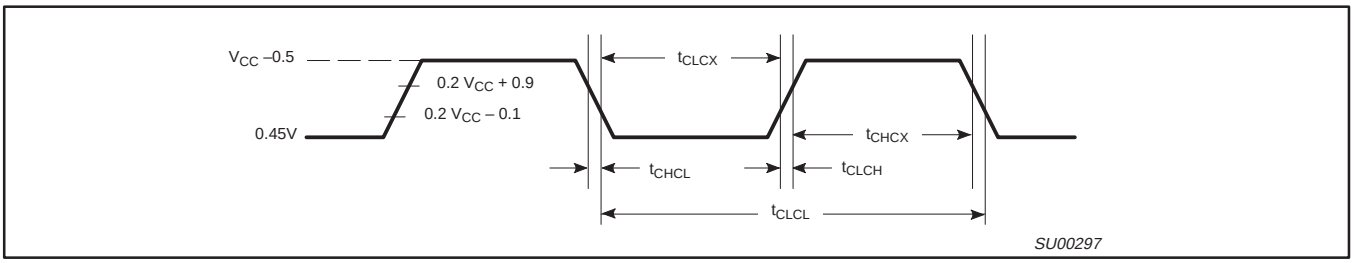


Figure 3. External Clock Drive

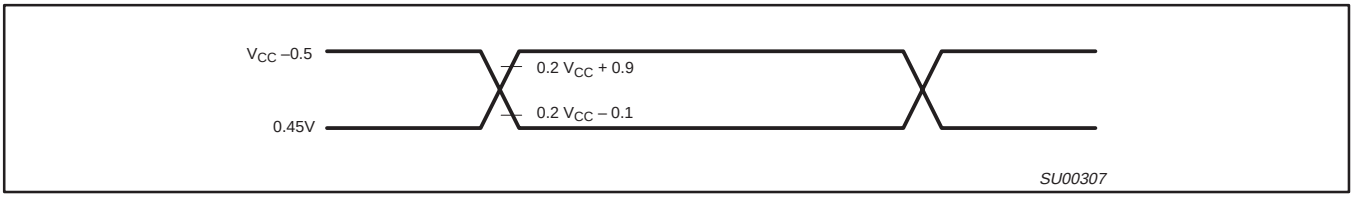


Figure 4. AC Testing Input/Output

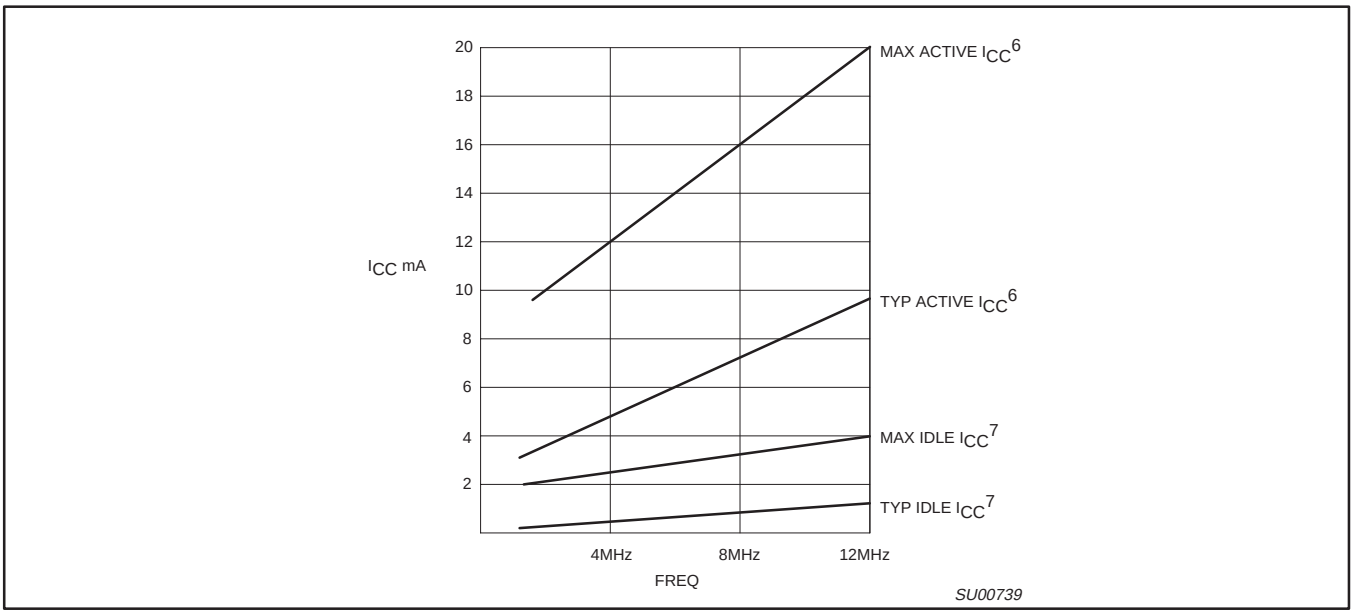
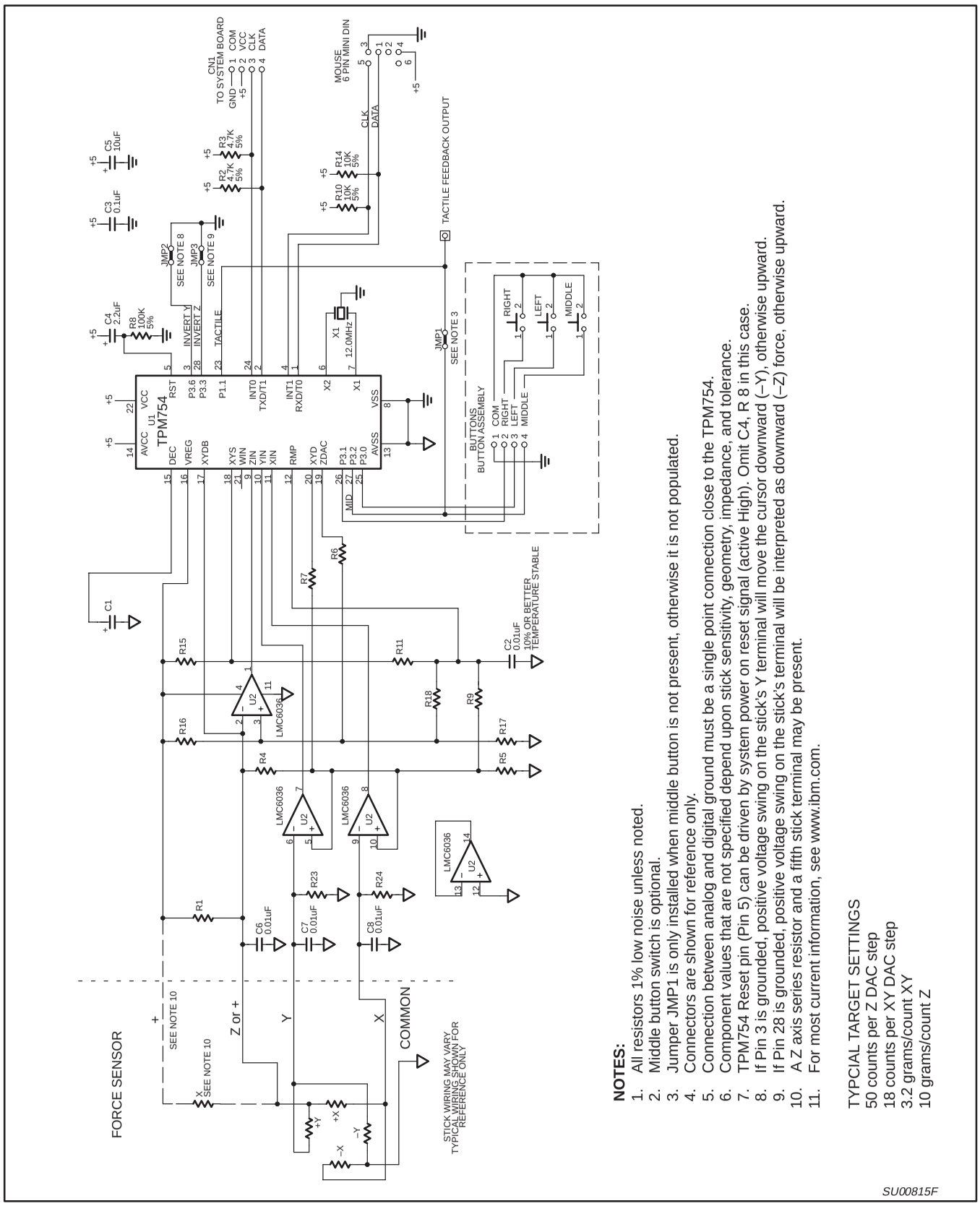


Figure 5. I_{CC} vs. FREQ
Maximum I_{CC} values taken at V_{CC} = 5.5V and worst case temperature.
Typical I_{CC} values taken at V_{CC} = 5.0V and 25°C.
Notes 6 and 7 refer to AC Electrical Characteristics.

SCHEMATIC OF TRACKPOINT SYSTEM



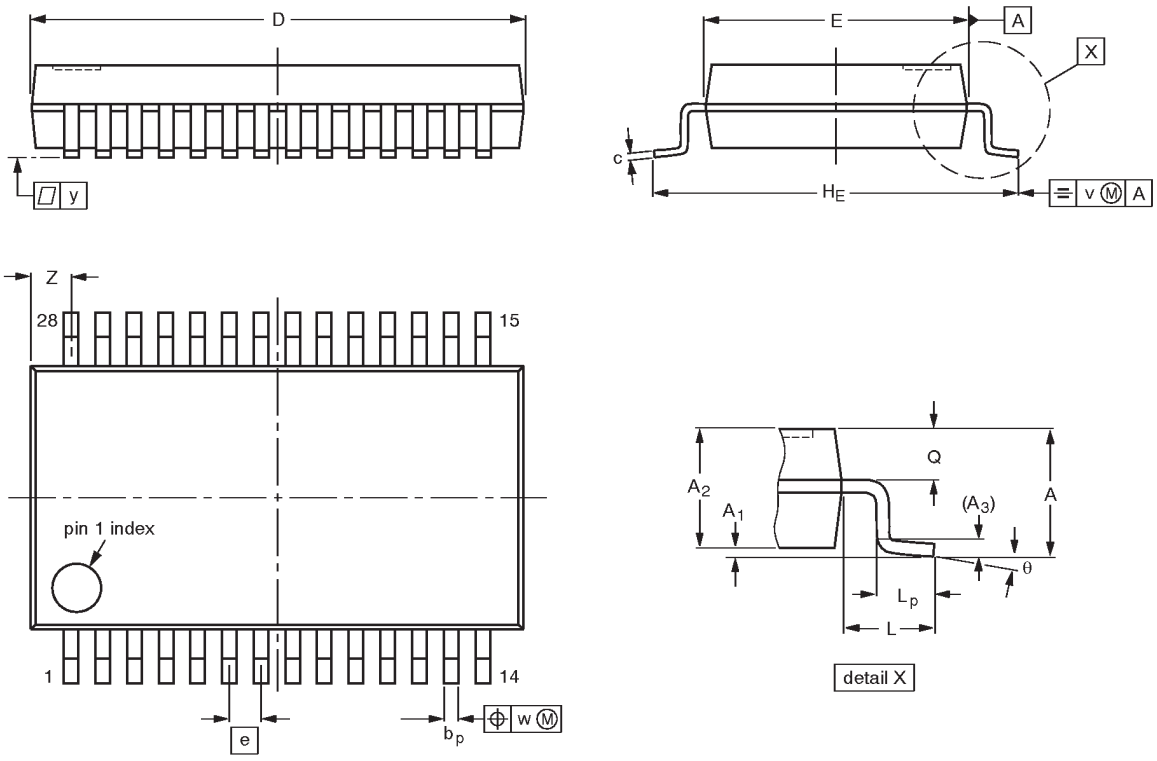
NOTES:

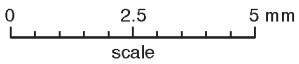
1. All resistors 1% low noise unless noted.
2. Middle button switch is optional.
3. Jumper JMP1 is only installed when middle button is not present, otherwise it is not populated.
4. Connectors are shown for reference only.
5. Connection between analog and digital ground must be a single point connection close to the TPM754.
6. Component values that are not specified depend upon stick sensitivity, geometry, impedance, and tolerance.
7. TPM754 Reset pin (Pin 5) can be driven by system power on reset signal (active High). Omit C4, R 8 in this case.
8. If Pin 3 is grounded, positive voltage swing on the stick's Y terminal will move the cursor downward (–Y), otherwise upward.
9. If Pin 28 is grounded, positive voltage swing on the stick's terminal will be interpreted as downward (–Z) force, otherwise upward.
10. A Z axis series resistor and a fifth stick terminal may be present.
11. For most current information, see www.ibm.com.

TYPCIAL TARGET SETTINGS
50 counts per Z DAC step
18 counts per XY DAC step
3.2 grams/count XY
10 grams/count Z

SU00815F

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3mm **SOT341-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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