128M [x8/x16] SINGLE 3V PAGE MODE FLASH MEMORY

FEATURES

- 2.7V to 3.6V operation voltage
- Block Structure
  - 128 x 128Kbyte Erase Blocks
- Fast random / page mode access time
  - 150/25 ns Read Access Time
- 128-bit Protection Register
  - 64-bit Unique Device Identifier
  - 64-bit User Programmable OTP Cells
- 32-Byte Write Buffer
  - 6 us/byte Effective Programming Time
- Enhanced Data Protection Features Absolute Protection with VPEN = GND
  - Flexible Block Locking
  - Block Erase/Program Lockout during Power Transitions

Performance

- Low power dissipation
  - typical 15mA active current for page mode read
  - 80uA/(max.) standby current
  - Deep power-down current: 5uA
- High Performance
  - Block erase time: 2s typ.
  - Byte programming time: 210us typ.
  - Block programming time: 0.8s typ. (using Write to Buffer Command)
- Program/Erase Endurance cycles: 10,000 cycles

Software Feature

- Support Common Flash Interface (CFI)
  - Flash device parameters stored on the device and provide the host system to access.
- Automation Suspend Options
  - Block Erase Suspend to Read
  - Block Erase Suspend to Program
  - Program Suspend to Read

Hardware Feature(Not for 48-TSOP/48-RTSOP)

- A0 pin
  - Select low byte address when device is in byte mode. Not used in word mode.
- STS pin
  - Indicates the status of the internal state machine.
- VPEN pin
  - For Erase /Program/ Block Lock enable.
- VCCQ Pin
  - The output buffer power supply, control the device 's output voltage.

Packaging

- 48-Lead TSOP
- 48-Lead RTSOP
- 56-Lead TSOP
- 64-ball CSP

Technology

- MX28F128J3 using Nbit (0.25u) Flash Technology

GENERAL DESCRIPTION

The MXIC's MX28F128J3 series Flash use the most advance 2 bits/cell Nbit technology, double the storage capacity of memory cell. The device provide the high density Flash memory solution with reliable performance and most cost-effective.

The device organized as by 8 bits or by 16 bits of output bus. The device is packaged in 48-Lead TSOP, 48-Lead RTSOP, 56-Lead TSOP, and 64-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The device offers fast access time and allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the device has separate chip enable (CE0, CE1, CE2) and output enable ($\overline{OE}$) controls. The device augment EPROM functionality with in-circuit electrical erasure and programming. The device uses a command register to manage this functionality.

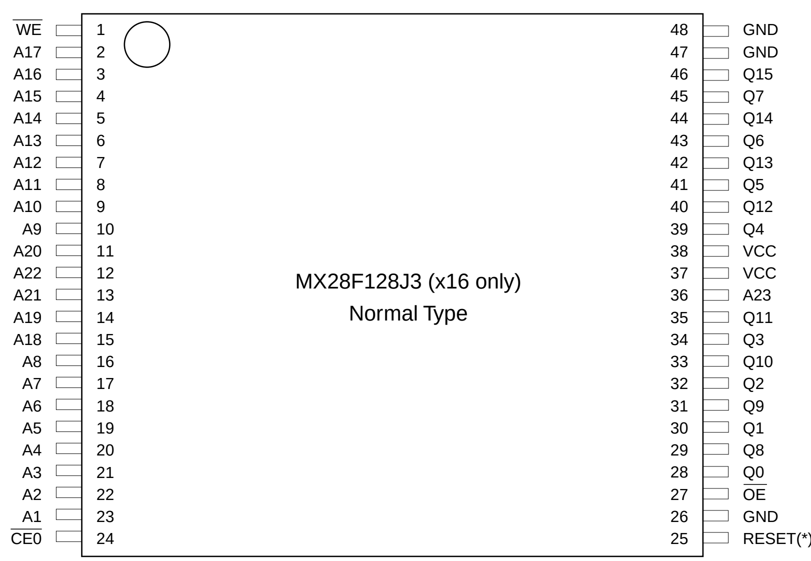
The MXIC's Nbit technology reliably stores memory contents even after the specific erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms by utilizing the dielectric's character to trap or release charges from ONO layer.

The device uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved

PIN CONFIGURATION

48-TSOP (12mm x 20mm) (for MX28F128J3 word mode only)



(* RESET pin : high enable)

48-RTSOP (12mm x 20mm) (for MX28F128J3 word mode only)

MX28F128J3 (x16 only)
Reverse Type

Signal	Pin	Pin	Signal
GND	48	1	$\overline{WE}$
GND	47	2	A17
Q15	46	3	A16
Q7	45	4	A15
Q14	44	5	A14
Q6	43	6	A13
Q13	42	7	A12
Q5	41	8	A11
Q12	40	9	A10
Q4	39	10	A9
VCC	38	11	A20
VCC	37	12	A22
A23	36	13	A21
Q11	35	14	A19
Q3	34	15	A18
Q10	33	16	A8
Q2	32	17	A7
Q9	31	18	A6
Q1	30	19	A5
Q8	29	20	A4
Q0	28	21	A3
$\overline{OE}$	27	22	A2
GND	26	23	A1
RESET(*)	25	24	$\overline{CE0}$

(* RESET pin : high enable)

56 TSOP (14mm x 20mm)

Signal	Pin	Pin	Signal
A22	1	56	NC
CE1	2	55	$\overline{WE}$
A21	3	54	$\overline{OE}$
A20	4	53	STS
A19	5	52	Q15
A18	6	51	Q7
A17	7	50	Q14
A16	8	49	Q6
VCC	9	48	GND
A15	10	47	Q13
A14	11	46	Q5
A13	12	45	Q12
A12	13	44	Q4
CE0	14	43	VCCQ
VPEN	15	42	GND
$\overline{RESET}$	16	41	Q11
A11	17	40	Q3
A10	18	39	Q10
A9	19	38	Q2
A8	20	37	VCC
GND	21	36	Q9
A7	22	35	Q1
A6	23	34	Q8
A5	24	33	Q0
A4	25	32	A0
A3	26	31	$\overline{BYTE}$
A2	27	30	**A23**
A1	28	29	CE2

64 Ball CSP (10x13x1.2mm, 1.0mm-ball pitch)

	1	2	3	4	5	6	7	8
A	A1	A6	A8	VPEN	A13	VCC	A18	A22
B	A2	GND	A9	CE0	A14	DU	A19	CE1
C	A3	A7	A10	A12	A15	DU	A20	A21
D	A4	A5	A11	$\overline{\text{RESET}}$	DU	DU	A16	A17
E	Q8	Q1	Q9	Q3	Q4	DU	Q15	STS
F	$\overline{\text{BYTE}}$	Q0	Q10	Q11	Q12	DU	DU	$\overline{\text{OE}}$
G	A23	A0	Q2	VCCQ	Q5	Q6	Q14	$\overline{\text{WE}}$
H	$\overline{\text{CE2}}$	DU	VCC	GND	Q13	GND	Q7	NC

13 mm

10mm

Notes:
1. Don't Use (DU) pins refer to pins that should not be connected.

PIN DESCRIPTION

SYMBOL	PIN NAME
A0	Byte Select Address
A1~A23	Address Input
Q0~Q15	Data Inputs/Outputs
CE0, CE1, CE2	Chip Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{RESET}}$	Reset/Deep Power Down mode (low enable for 56-TSOP & 64-CSP)
RESET	Reset/Deep Power Down mode (high enable for 48-TSOP & 48-RTSOP)

SYMBOL	PIN NAME
STS	STATUS Pin
$\overline{\text{BYTE}}$	Byte Mode Enable
VPEN	ERASE/PROGRAM/BLOCK Lock Enable
VCCQ	Output Buffer Power Supply
VCC	Device Power Supply
GND	Device Ground
NC	Pin Not Connected Internally
DU	Don't Use

ORDERING INFORMATION

PLASTIC PACKAGE

Part NO.	Access Time (ns)	Package type
MX28F128J3TBC-15	150/25	48-TSOP
MX28F128J3RBC-15	150/25	48-RTSOP
MX28F128J3TC-15	150/25	56-TSOP
MX28F128J3XCC-15	150/25	64-CSP