



# MX23C4096

## 4M-BIT [256K x 16] CMOS MASK ROM

### FEATURES

- 256K x 16 organization (JEDEC pin out)
- Single +5V power supply
- Fast access time: 100/120/150/200ns
- Totally static operation
- Completely TTI compatible

- Operating current: 60mA
- Standby current: 100uA
- Package
  - 40 pin DIP (600 mil)
  - 44 pin PLCC

### GENERAL DESCRIPTION

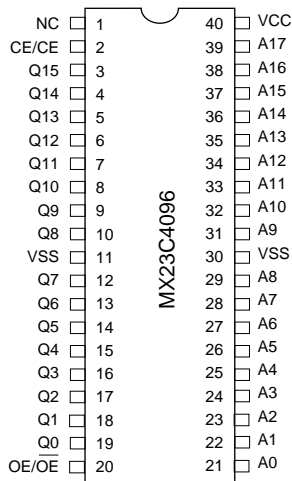
The MX23C4096 is a 5V only, 4M-bit, Read Only Memory. It is organized as 512Kx16 bit. MX23C4096 has a static standby mode, and has an access time of 100/120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

MX23C4096 offers automatic power-down, with power-down controlled by the chip enable (CE/CE) input. When CE/CE is not selected, the device automatically powers down and remains in a low-power standby mode as long as CE/CE stays in the unselected mode.

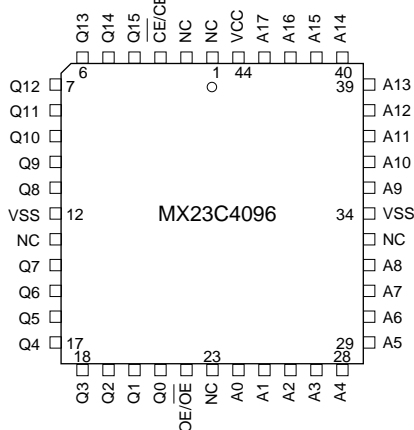
The OE/OE inputs as well as CE/CE input may be programmed either active High or Low.

### PIN CONFIGURATION

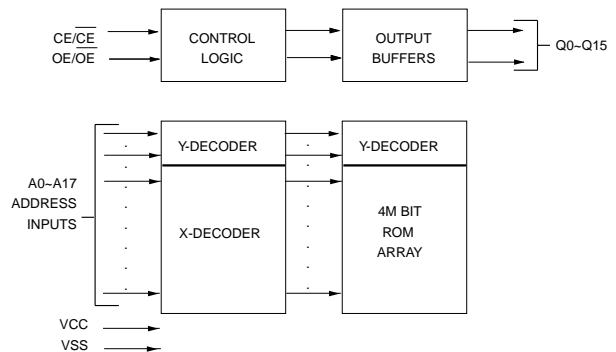
#### 40PDIP



#### 44 PLCC



### BLOCK DIAGRAM



### PIN DESCRIPTION

Symbol	Pin Function
A0~A17	Address Inputs
Q0~Q15	Data Outputs
CE/CE	Chip Enable Input
OE/OE	Output Enable Input
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

**ABSOLUTE MAXIMUM RATINGS\***

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V

**\*Notice:**

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

**DC CHARACTERISTICS** (TA = -10°C ~ 70°C, VCC = 5.0V ± 10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	VIN=0 to 5.5V
Output Leakage Current	ILO	-	10uA	VOUT=0 to 5.5V
Power-Down Supply Current	ICC3	-	100uA	$\overline{CE} > VCC - 0.2V$
Standby Supply Current	ICC2	-	1.0mA	$\overline{CE} = VIH$
Operating Supply Current	ICC1	-	60mA	Note1

**CAPACITANCE** (TA = 25°C, f = 1.0 MHz (Note 2))

Symbol	Parameter	Min.	Max.	Unit	Conditions
CIN	Input Capacitance		10	pF	VIN=0V
COUT	Output Capacitance		10	pF	VOUT=0V



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## AC CHARACTERISTICS (TA = -10°C ~ 70°C, VCC = 5.0V ± 10%)

PARAMETER	SYMBOL	23C4096-10		23C4096-12		23C4096-15		23C4096-20		CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Cycle Time	tCYC	100ns	-	120ns	-	150ns	-	200ns	-	
Address Access Time	tAA	-	100ns	-	120ns	-	150ns	-	200ns	
Output Hold Timer After Address Change	tOH	10ns	-	10ns	-	10ns	-	10ns	-	
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns	-	200ns	
Output Enable/Chip Select Access Time	tAOE	-	50ns	-	60ns	-	70ns	-	90ns	
Output Low Z Delay	tLZ	0ns	-	0ns	-	0ns	-	0ns	-	Note 3
Output High Z Delay	tHZ	-	30ns	-	30ns	-	30ns	-	30ns	Note 4

Note :

1. Measured with device selected at f=5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% tested.
3. Output low-impedance delay (tLZ) is measured from  $\overline{CE/OE}$  going low.
4. Output high-impedance delay (tHZ) is measured from  $\overline{CE/OE}$  going high.

## AC TEST CONDITIONS

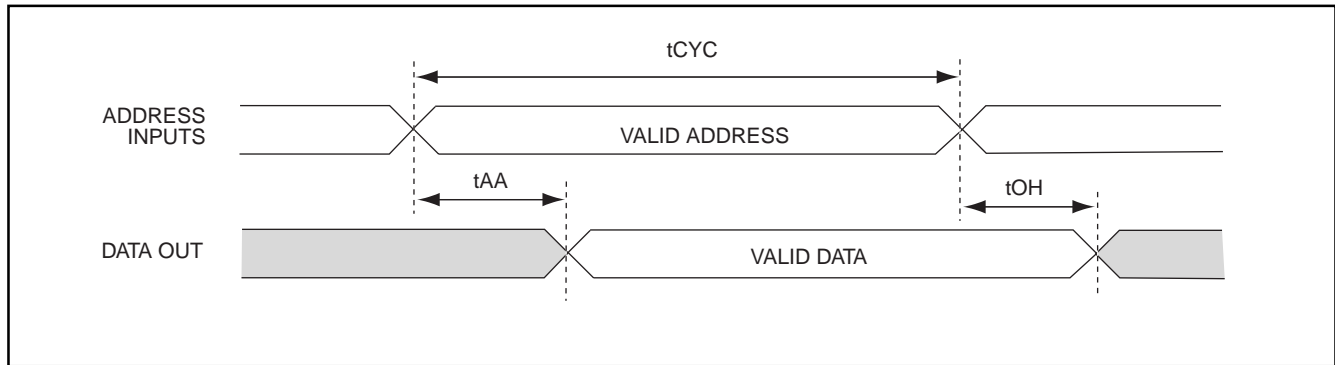
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure1



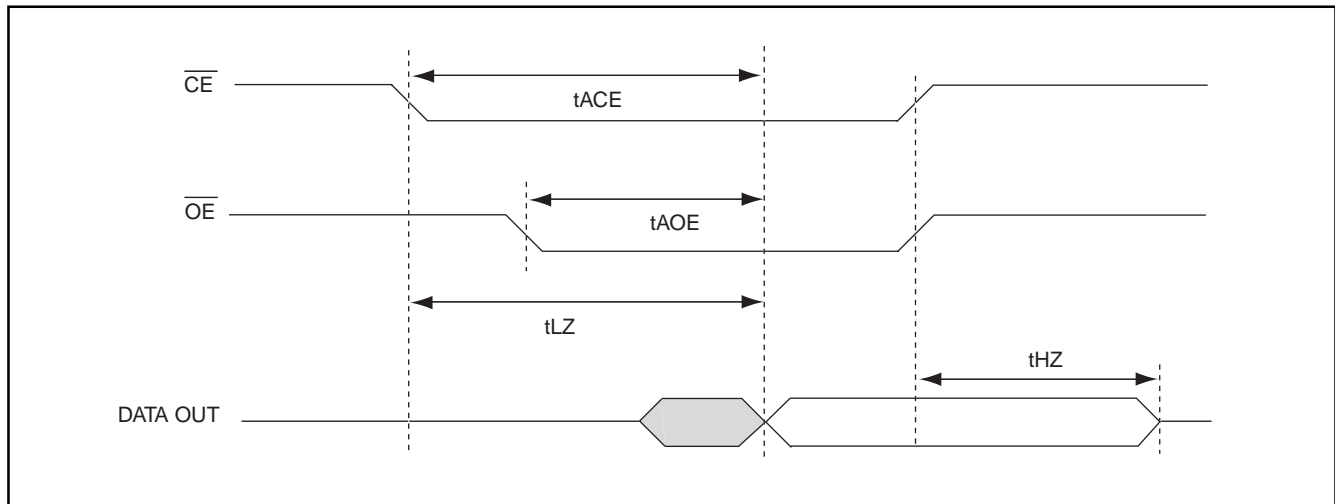
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## TIMING DIAGRAM

### PROPAGATION DELAY FROM ADDRESS ( $\overline{CE}/\overline{OE}$ =ACTIVE)



### PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



## ORDER INFORMATION

Part No.	Access Time	Operating Current MAX.	Standby Current MAX.	Package
MX23C4096PC-10	100ns	60mA	100uA	40 pin DIP
MX23C4096PC-12	120ns	60mA	100uA	40 pin DIP
MX23C4096PC-15	150ns	60mA	100uA	40 pin DIP
MX23C4096PC-20	200ns	60mA	100uA	40 pin DIP
MX23C4096QC-10	100ns	60mA	100uA	44 pin PLCC
MX23C4096QC-12	120ns	60mA	100uA	44 pin PLCC
MX23C4096QC-15	150ns	60mA	100uA	44 pin PLCC
MX23C4096QC-20	200ns	60mA	100uA	44 pin PLCC

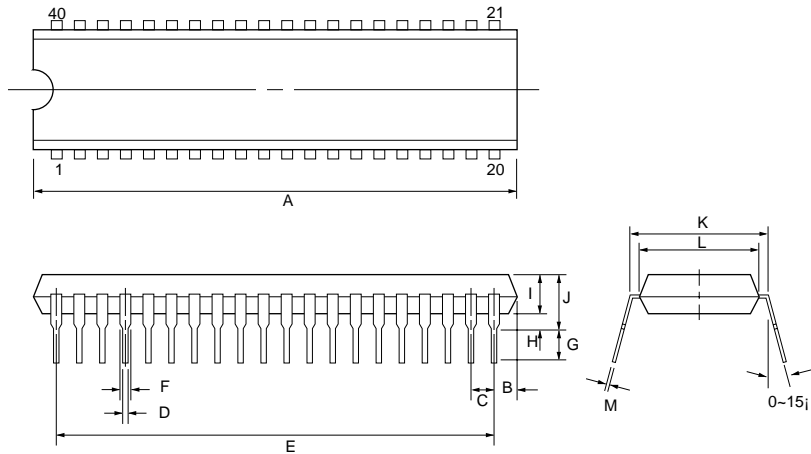


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## PACKAGE INFORMATION

### 40-PIN PLASTIC DIP (600 mil)

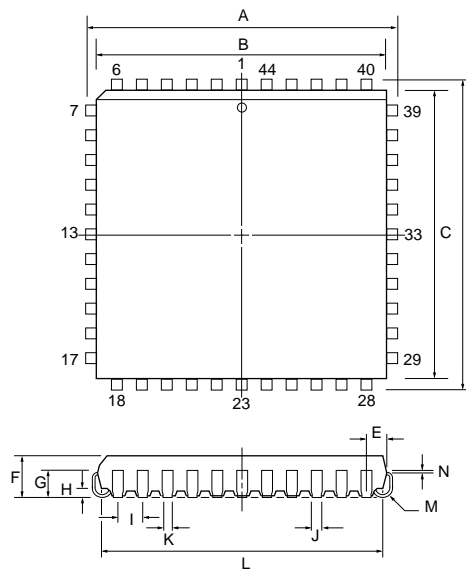
ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	48.22	1.900
F	1.52 [Typ.]	.060 [Typ.]
G	3.30±.25	.130±.010
H	.51 [REF]	.020 [REF]
I	3.94±.25	1.55±.010
J	5.33 max.	.210 max.
K	15.22±.25	.600±.010
L	13.97±.25	.550±.010
M	.25 [Typ.]	.010 [Typ.]



**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

### 44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	17.53±.12	.690±.005
B	16.59±.12	.653±.005
C	16.59±.12	.653±.005
D	17.53±.12	.690±.005
E	1.95	.077
F	4.70 max.	.185 max.
G	2.55±.25	.100±.010
H	.51 min.	.020 min.
I	1.27 [Typ.]	.050 [Typ.]
J	.71±.10	.028±.004
K	.46±.10	.018±.004
L	15.50±.51	.610±.020
M	.63 R	.025 R
N	.25 [Typ.]	.010 [Typ.]



**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

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