Precision Low Power 2.048 V SOT-23 Voltage Reference

ADR370

FEATURES

Initial accuracy: ±4 mV maximum
Initial accuracy error: ±0.2%
Low TCVO
  ±50 ppm/°C maximum from −40°C to +125°C
  30 ppm/°C maximum from +25°C to +70°C
Load regulation: 400 µV/mA, 100 ppm/mA
Line regulation: 25 µV/V, 20 ppm/V
Wide operating range: V_{IN} = 2.3 V to 15 V
Low power: 72 µA maximum
High output sink/source current: ±5 mA minimum
Wide temperature range: −40°C to +125°C
Tiny 3-lead SOT-23 package with standard pin configuration

APPLICATIONS

Battery-powered instrumentation
Portable medical instruments
Data acquisition systems
Industrial process control systems
Automotive

PIN CONFIGURATION

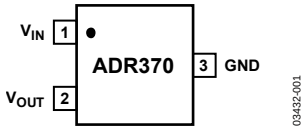

Figure 1. 3-Lead SOT-23

Table 1. ADR370 Products

Products	Output Voltage (V_O)	Initial Accuracy ± (mV)	Initial Accuracy ± (%)	Temperature Coefficient (ppm/°C)
ADR370BRT-REEL7	2.048	4	0.2	50
ADR370ART-REEL7	2.048	10	0.5	100

GENERAL DESCRIPTION

The ADR370[1] is a low cost, 3-terminal (series) band gap voltage reference featuring high accuracy, high stability, and low power consumption packaged in a tiny 3-lead SOT-23 package. Precise matching and thermal tracking of on-chip components, as well as patented temperature drift curvature correction design techniques, have been employed to ensure that the ADR370 provides an accurate 2.048 V output.

This micropowered, low dropout voltage device sources or sinks up to 5 mA of load current while providing a stable 2.048 V output. The compact footprint, high accuracy, and operating range of 2.3 V to 12 V make the ADR370 ideal for use in 3 V and 5 V systems where there can be wide variations in supply voltage and a need to minimize power dissipation.

The ADR370 is offered in A and B grades; all devices are specified over the extended industrial range of −40°C to +125°C.

[1] Protected by U.S. Patent No. 5,969,657; other patents pending.

Rev. B
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$T_A = T_{MIN}$ to T_{MAX}, $V_{IN} = 5$ V, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE (@ 25°C)	V_O		2.044	2.048	2.052	V
INITIAL ACCURACY ERROR	V_{OERR}					
A Grade			−10		+10	mV
			−0.5		+0.5	%
B Grade			−4		+4	mV
			−0.2		+0.2	%
OUTPUT VOLTAGE TEMPERATURE DRIFT[1]	TCV_O					
A Grade		−40°C to +125°C			100	ppm/°C
B Grade		−40°C to +125°C			50	ppm/°C
		25°C to 70°C			30	ppm/°C
SUPPLY HEADROOM	$V_{IN} - V_{OUT}$		200			mV
LOAD REGULATION		0 mA < I_{OUT} < 5 mA @ 25°C			+0.400	mV/mA
		−3 mA < I_{OUT} < 0 mA @ 25°C			+0.600	mV/mA
		−0.1 mA < I_{OUT} < +0.1 mA			+4.75	mV/mA
LINE REGULATION		V_{OUT} = 200 mV < V_{IN} < 15 V I_{OUT} = 0 mA			20	ppm/V
RIPPLE REJECTION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 5 V ± 100 mV (f = 120 Hz)	80			dB
QUIESCENT CURRENT					72	µA
SHORT-CIRCUIT CURRENT TO GROUND					15	mA
NOISE VOLTAGE (@ 25°C)		0.1 Hz to 10 Hz		70		µV p-p
		10 Hz to 10 kHz		50		µV rms
TURN-ON SETTLING TIME	C_L = 0.2 µF			100		µs
LONG-TERM STABILITY		1000 hours @ 25°C			100	ppm/1000 hrs
OUTPUT VOLTAGE HYSTERESIS				115		ppm
TEMPERATURE RANGE			−40		+125	°C

[1] Guaranteed by characterization.

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ABSOLUTE MAXIMUM RATINGS

Ratings at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	18 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature	
Soldering, 60 sec	215°C
Infrared, 15 sec	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
3-Lead SOT-23 (RT)	220	102	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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TYPICAL PERFORMANCE CHARACTERISTICS

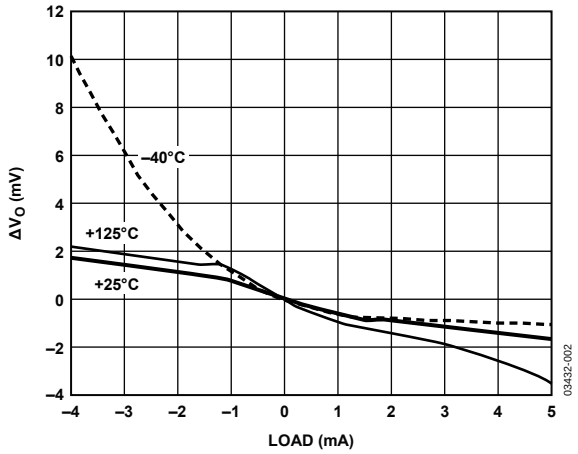

Figure 2. Load Regulation vs. Load Current

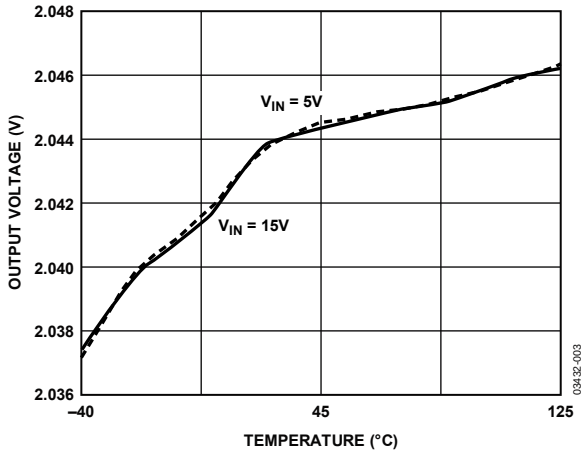

Figure 3. Output Voltage vs. Temperature

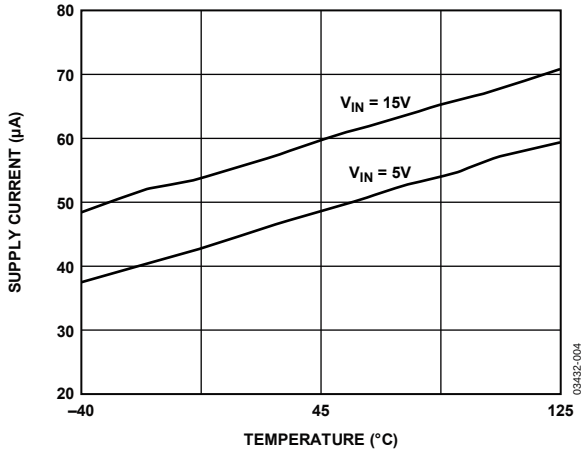

Figure 4. Supply Current vs. Temperature

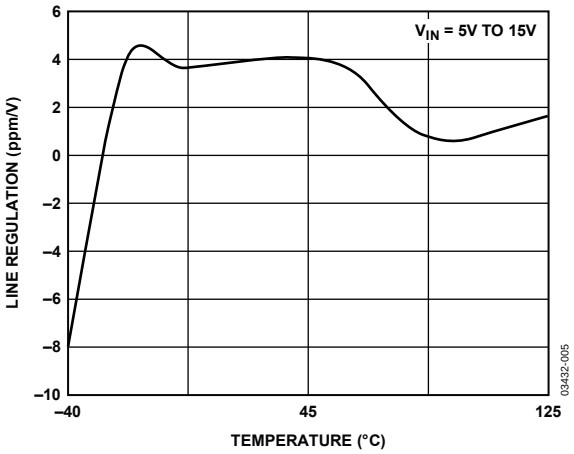

Figure 5. Line Regulation vs. Temperature

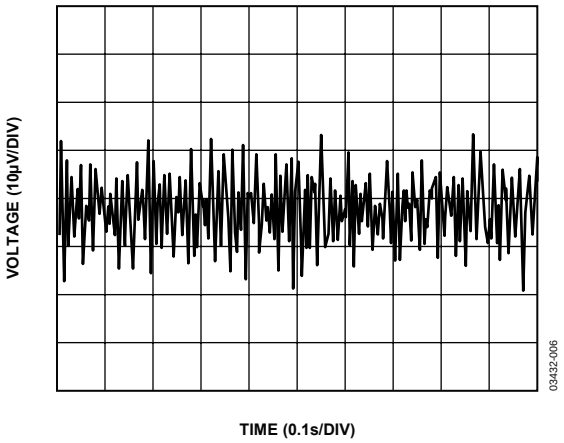

Figure 6. Voltage Noise 0.1 Hz to 10 Hz

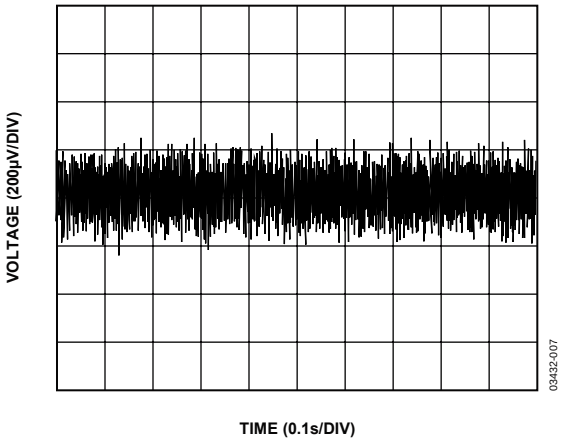

Figure 7. Voltage Noise 10 Hz to 100 kHz

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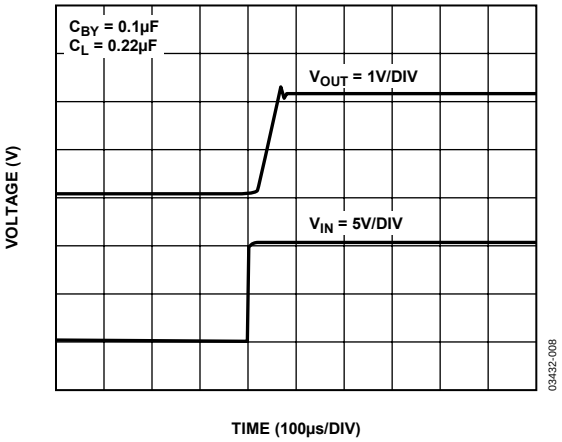

Figure 8. Turn-On Response

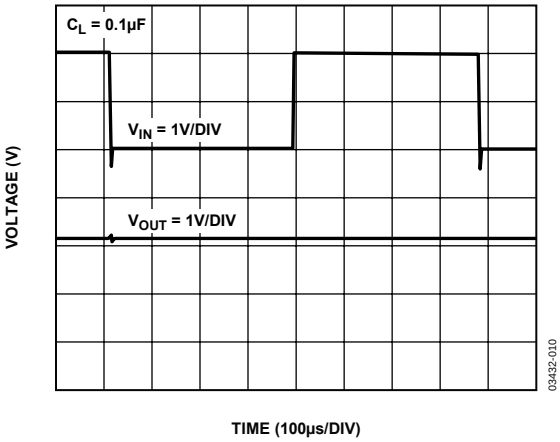

Figure 10. Line Transient Response

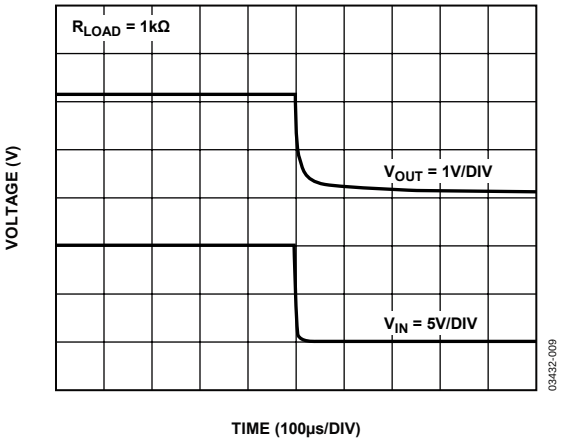

Figure 9. Turn-Off Response

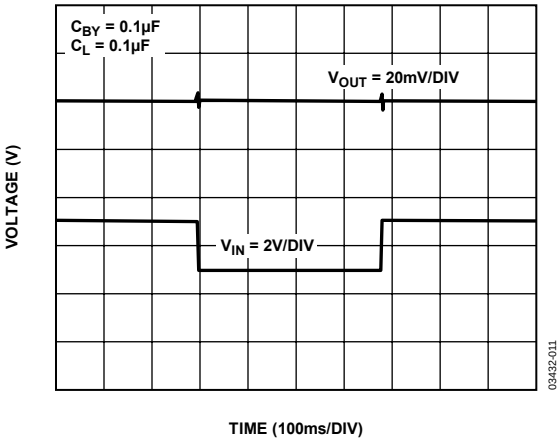

Figure 11. Load Transient Response

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TERMINOLOGY

Temperature Coefficient

Temperature coefficient is the change of output voltage with respect to operating temperature changes, normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and can be determined with the following equation

$$TCV_O\left[\frac{\text{ppm}}{°\text{C}}\right]=\frac{V_O(T_2)-V_O(T_1)}{V_O(25°\text{C})\times(T_2-T_1)}\times10^6 \quad (1)$$

where:

V_O (25°C) = V_O at 25°C.
V_O (T_1) = V_O at Temperature 1.
V_O (T_2) = V_O at Temperature 2.

Line Regulation

Line regulation is the change in output voltage due to a specified change in input voltage. This parameter accounts for the effects of self-heating. Line regulation is expressed in either percent per volt, parts-per-million per volt, or microvolts per volt change in input voltage.

Load Regulation

Load regulation is the change in output voltage due to a specified change in load current. This parameter accounts for the effects of self-heating. Load regulation is expressed in either microvolts per milliampere, parts-per-million per milliampere, or ohms of dc output resistance.

Long-Term Stability

Long-term stability is the typical shift of output voltage at 25°C on a sample of parts subjected to a test of 1000 hours at 25°C.

$$\Delta V_O=V_O(t_1)-V_O(t_2)$$
$$\Delta V_O[\text{ppm}]=\frac{V_O(t_1)-V_O(t_2)}{V_O(t_1)}\times10^6 \quad (2)$$

where:

V_O (t_1) = V_O at 25°C at Time 0.
V_O (t_2) = V_O at 25°C after 1000 hours operation at 25°C.

Thermal Hysteresis

Thermal hysteresis is defined as the change of output voltage after the device is cycled through temperature from +25°C to −40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle.

$$V_{O\_HYS}=V_O(25°\text{C})-V_{O\_TC}$$
$$V_{O\_HYS}[\text{ppm}]=\frac{V_O(25°\text{C})-V_{O\_TC}}{V_O(25°\text{C})}\times10^6 \quad (3)$$

where:

V_O (25°C) = V_O at 25°C.
V_{O_TC} = V_O at 25°C after temperature cycle of +25°C to −40°C to +125°C and back to +25°C.

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THEORY OF OPERATION

The ADR370 uses the band gap concept to produce a stable, low temperature coefficient voltage reference suitable for high accuracy data acquisition components and systems. This device makes use of underlying temperature characteristics of a silicon transistor's base-emitter voltage (V_{BE}) in the forward-biased operating region. Under this condition, all such transistors have a −2 mV/°C temperature coefficient (TC) and a V_{BE} that, when extrapolated to absolute zero, 0 K, (with collector current proportional to absolute temperature) approximates the silicon band gap voltage. By summing a voltage that has an equal and opposite temperature coefficient of 2 mV/°C with a V_{BE} of a forward-biased transistor, an almost zero TC reference can be developed. The simplified circuit diagram in Figure 12 shows how a compensating voltage, V1, is achieved by driving two transistors at different current densities and amplifying the resulting V_{BE} difference (ΔV_{BE}, which has a positive TC). The sum (V_{BG}) of V_{BE} and V1 is then buffered and amplified to produce a stable reference voltage of 2.048 V at the output.

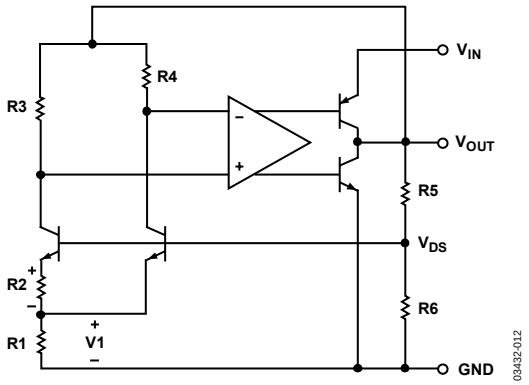

Figure 12. Simplified Schematic

APPLYING THE ADR370

To achieve the specified performance, two external components should be used in conjunction with the ADR370: a 4.7 µF capacitor and a 1 µF capacitor. The 4.7 µF capacitor should be applied to the input, and the 1 µF capacitor should be applied to the output. Figure 13 shows the ADR370 with both the input and output capacitors attached.

For further transient response optimization, an additional 0.1 µF capacitor in parallel with the 4.7 µF input capacitor can be used.

A 1 µF output capacitor provides stable performance for all loading conditions. The ADR370 can, however, operate under low (−100 µA < I_{OUT} < +100 µA) current conditions with just a 0.2 µF output capacitor and a 1 µF input capacitor.

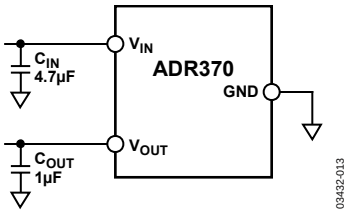

Figure 13. Typical Connection Diagram

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APPLICATIONS INFORMATION

LOW COST NEGATIVE REFERENCE

A low cost negative reference can be obtained by leveraging the current sinking capability of the ADR370. By simply tying the V_{OUT} terminal to ground and adding a bias resistor (R_{SET}) to the GND pin of the device, a negative voltage reference can be obtained as shown in Figure 14. R_{SET} should be chosen such that I_{SET} remains between 1 mA to 5 mA.

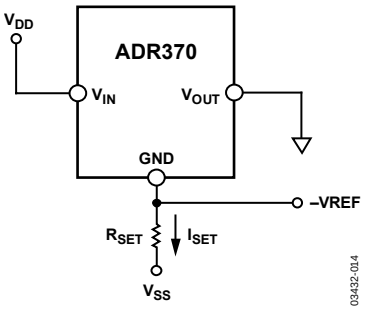

Figure 14. Low Cost Negative Reference

PRECISION NEGATIVE REFERENCE

Without using any matching resistors, a precision negative reference can be obtained using the configuration shown in Figure 15. The voltage difference between V_{OUT} and GND of the ADR370 is 2.048 V. Because V_{OUT} is at virtual ground, U2 closes the loop by forcing the GND pin to be the negative reference node. U2 should be a low offset voltage precision op amp, such as the OP1177.

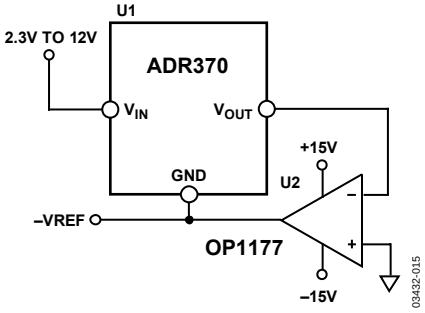

Figure 15. Precision Negative Reference

LOW COST CURRENT SOURCE

Figure 16 illustrates how a simple, low cost current source can be configured using the ADR370. The load current, I_L, is simply the sum of I_{SET} and the quiescent current, I_q. I_{SET} is simply the reference voltage generated by the ADR370 divided by R_{SET}.

$$I_{SET} = \frac{2.048\ \text{V}}{R_{SET}} \tag{4}$$

The quiescent current, I_q, varies slightly with load. The variation in I_q limits the use of this circuit to general-purpose applications.

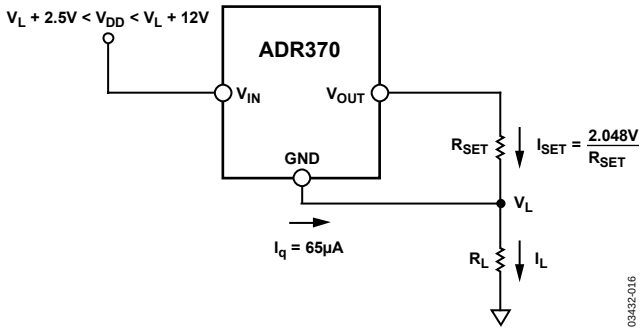

Figure 16. Low Cost Current Source

PRECISION CURRENT SOURCE WITH ADJUSTABLE OUTPUT

A precision current source can be implemented with the circuit shown in Figure 17. By adding a mechanical or digital potentiometer, this circuit becomes an adjustable current source. If a digital potentiometer, such as the AD5201 is used, the load current is simply the voltage across terminals B-to-W of the digital potentiometer divided by R_{SET}.

$$I_L = \frac{V_{REF} \times D}{R_{SET} \times 256} \tag{5}$$

where D is the decimal equivalent of the digital potentiometer input code.

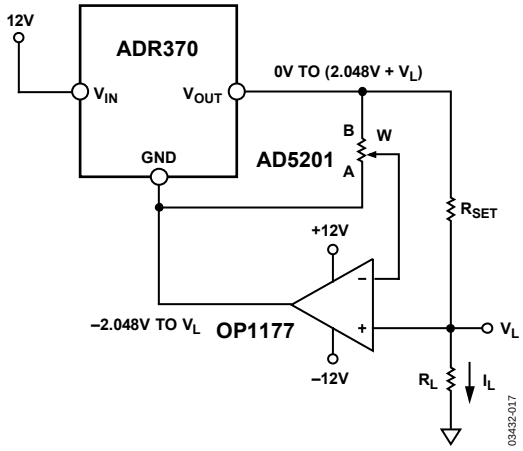

Figure 17. Programmable 0 mA to 5 mA Current Source

To optimize the resolution of this circuit, dual-supply op amps should be used because the ground potential of the ADR370 can swing from –2.048 V at zero scale to V_L at full scale of the potentiometer setting.

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12-BIT PRECISION PROGRAMMABLE CURRENT SOURCE

By replacing the potentiometer in Figure 17 with a 12-bit precision DAC, such as the AD5322, a higher precision programmable current source can be achieved. Figure 18 illustrates the implementation of this circuit. The load current can be determined with the following equation:

$$I_L = \frac{V_{REF}(1-D)}{R_{SET} \times 4096} \quad (6)$$

The compliance voltage should be kept low so that the supply voltage to U2, between V_{DD} and GND, does not fall below 2.5 V.

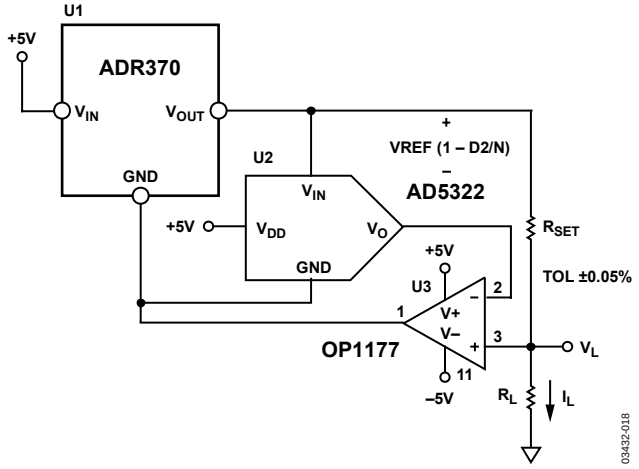

Figure 18. 12-Bit Programmable Current Source

PRECISION BOOSTED OUTPUT REGULATOR

A precision voltage output with boosted current can be realized with the circuit shown in Figure 19. In this circuit, V_O is maintained by the ADR370 at 2.048 V.

The ADR370 sources a maximum of 5 mA if the load current (I_L) is more than 5 mA, and if the current is furnished by the transistor (Q1) and the input voltage supply (V_{DD}).

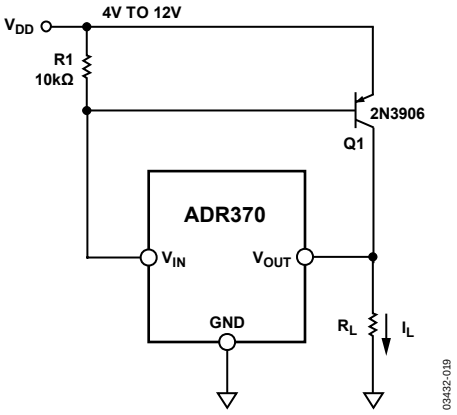

Figure 19. Precision Boosted Output Regulator

Q1 is turned on to regulate current as needed. R1 is required to bias the base of Q1 and must be large enough to comply with the supply current requirements of the ADR370. The supply voltage can be as low as 4 V.

The maximum current output of this circuit is limited by the power dissipation of the bipolar transistor, Q1.

$$P_{DISS} = (V_{DD} - 2.048) \times I_L \quad (7)$$

Using the 2N3906 PNP transistor shown in Figure 19 and a 4 V power supply (R_L) should be chosen so that a maximum of 100 mA is drawn from the circuit, which limits the power dissipation of Q1 to ~200 mW.

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OUTLINE DIMENSIONS

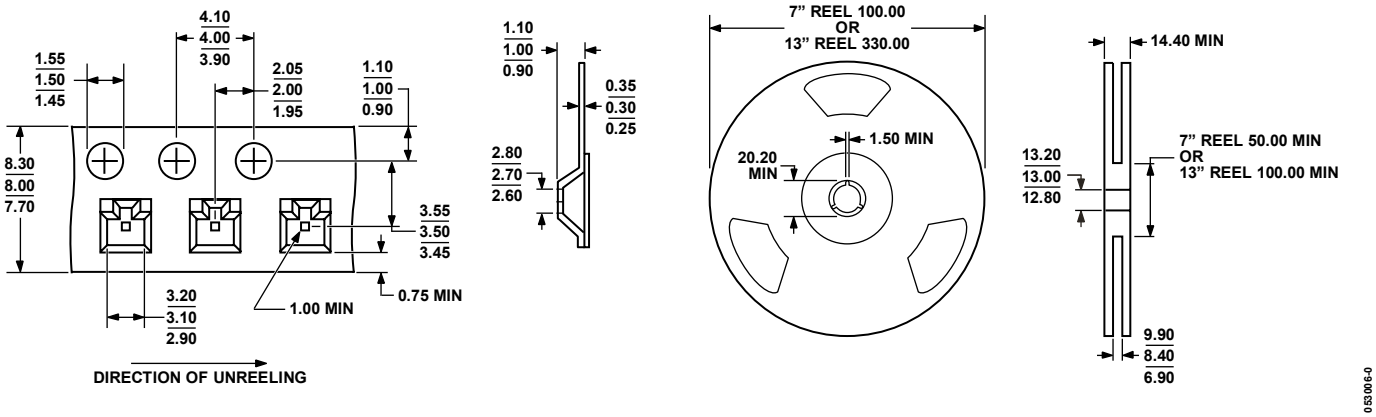

Figure 20. SOT-23-3 Tape and Reel Outline Dimensions
Dimensions shown in millimeters

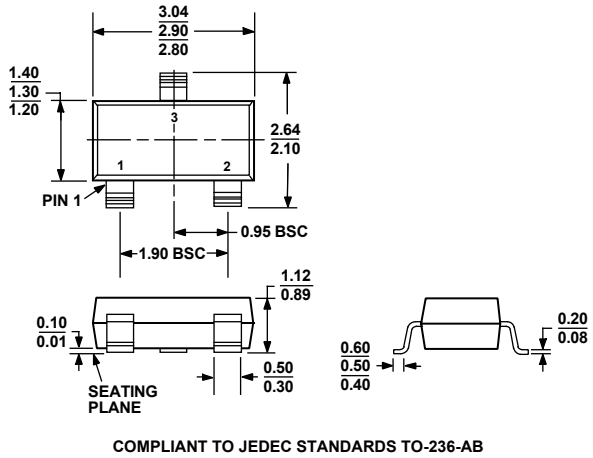

Figure 21. 3-Lead Small Outline Transistor Package [SOT-23-3]
(RT-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Output Voltage (V_O)	Initial Accuracy ± (mV)	Initial Accuracy ± (%)	Temperature Coefficient (ppm/°C)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADR370ART-R2	2.048	10	0.5	100	−40°C to +125°C	3-Lead SOT-23-3	RT-3	250	RPA
ADR370ART-REEL7	2.048	10	0.5	100	−40°C to +125°C	3-Lead SOT-23-3	RT-3	3,000	RPA
ADR370ARTZ-REEL7[1]	2.048	10	0.5	100	−40°C to +125°C	3-Lead SOT-23-3	RT-3	3,000	L26
ADR370BRT-R2	2.048	4	0.5	50	−40°C to +125°C	3-Lead SOT-23-3	RT-3	250	RPB
ADR370BRT-REEL7	2.048	4	0.2	50	−40°C to +125°C	3-Lead SOT-23-3	RT-3	3,000	RPB
ADR370BRTZ-R2[1]	2.048	4	0.5	50	−40°C to +125°C	3-Lead SOT-23-3	RT-3	250	L27
ADR370BRTZ-REEL7[1]	2.048	4	0.2	50	−40°C to +125°C	3-Lead SOT-23-3	RT-3	3,000	L27

[1] Z = RoHS Compliant Part.

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NOTES

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